Analytical threshold voltage model for strained silicon GAA-TFET*

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Tunnel field effect transistors (TFETs) are promising devices for low power applications. An analytical threshold voltage model, based on the channel surface potential and electric field obtained by solving the 2D Poisson's equation, for strained silicon gate all around TFETs is proposed. The variation of the threshold voltage with device parameters, such as the strain (Ge mole fraction x), gate oxide thickness, gate oxide permittivity, and channel length has also been investigated. The threshold voltage model is extracted using the peak transconductance method and is verified by good agreement with the results obtained from the TCAD simulation.

Keywords: tunnel field effect transistor, threshold voltage, strained silicon

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1. Introduction

Continuous scaling of traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) for high performance can result in a rapid increase of power, which blocks its applications in the low power domains.[1–3] Therefore, tunnel field effect transistors (TFETs) have been considered as one of the most promising candidates for MOSFETs beyond 45 nm for future ultra-low power applications due to their better immunity to short channel effects, higher I_{ON}/I_{OFF} ratio, and so on.[4–7] However, TFETs to date show a low drain current due to the low band-to-band tunneling (BTBT) efficiency.

To boost the tunneling currents, the biaxial strained silicon technology, which reduces the effective carrier transport mass (m^*) by lowering and splitting the band gap resulting from the exerted strain in the silicon layer, seems to be an effective way to enhance the tunnel efficiency.[8–10] Gate all around TFETs (GAA TFETs) with strained silicon can provide enhanced electrostatic performance and optimum scaling capability to improve the current. The gate threshold voltage is a key electrical parameter for designing the TFET. Additionally, to estimate the device current we must know the threshold voltage.[11,12] Although plenty of efforts have been made for the extraction of TFET threshold voltages and some models have been developed, reports on the models for strained silicon TFETs with a GAA architecture have been rare.

In this paper, an analytical threshold voltage model for strained silicon GAA TFETs is developed. Moreover, the effect of the device parameters like the strain (Ge mole fraction x), gate oxide thickness, gate oxide permittivity, and channel length on the threshold voltage have been discussed, which can provide an effective reference for designing the GAA TFET. The model threshold voltage is extracted using peak transconductance method and is in excellent agreement with the TCAD simulation results, giving the evidence for its validity.

2. Structure and analytical model

2.1. Structure of the strained silicon GAA TFET

Figure 1 shows a cross-sectional diagram of a GAA TFET. The proposed cylindrical TFET is constructed mainly by a PIN and surrounding gate, which provides better electrostatic control over the channel. The doping concentrations of the source and drain regions are N_s and N_d, respectively. The intermediate channel is moderately n-doped, with a doping concentration N_c. L_g is the length of the gate, R is the radius of the channel, and T_{ox} is the thickness of the gate oxide layer. Because of the strain (Ge mole fraction x) in $Si_{1-x}Ge_x$, the energy band gap of the strained silicon GAA TFET changes with the Ge mole fraction x, which is shown in Fig. 2 for $x = 0.1$ and $x = 0.3$. As the energy band gap narrows, the tunneling probability increases, and the drain current of a GAA TFET in the ON state improves.

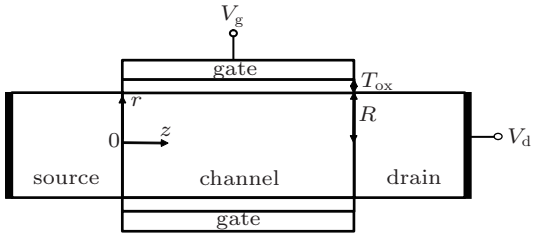


Fig. 1. Cross-sectional diagram of the n-TFET.

GAA TFET is basically a reverse biased PIN diode with the working principle of a quantum mechanical BTBT mechanism.[13] When a positive voltage is applied to the end

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of the gate and drain over the threshold voltage, the energy band at the source-channel junction is strongly bended, and valence and conduction band overlap occurs, as shown in Fig. 2. Simultaneously, the BTBT current occurs in the GAA TFET. Therefore, the threshold voltage is a key point in the analysis of the current.

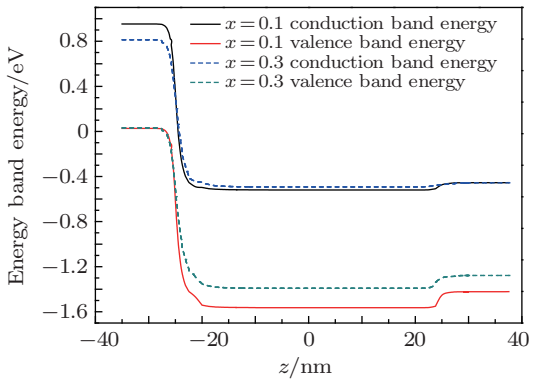


Fig. 2. (color online) Energy band of the strained-silicon.

2.2. Analytical threshold voltage model

To predict the channel surface potential characteristic of the GAA TFET in the subthreshold region, we assume that the mobile charges in this region are negligible and that source-channel and drain-channel junctions are abrupt. Therefore, the 2D Poisson's equation at the n-type strained silicon cylindrical channel can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi(r,z)}{\partial r}\right)+\frac{\partial^2\phi(r,z)}{\partial z^2}=-\frac{qN_c}{\varepsilon_{ssi}},$$
$$0\le r\le R,\quad 0\le z\le L_g, \tag{1}$$

where $\phi(r,z)$ is the electrostatic potential in the channel region, ε_{ssi} is the strained silicon region dielectric permittivity, and r varies from zero to R.

To obtain the solution of Eq. (1), a parabolic approximation of the channel potential distribution in the radial direction is applied, which can be written as[14]

$$\phi(r,z)=a_0(z)+a_1(z)r+a_2(z)r^2. \tag{2}$$

The coefficients $a_0(z)$, $a_1(z)$, and $a_2(z)$ are functions of z only, which can be determined by using the following boundary conditions:

i) At the interface between the gate oxide and the strained silicon, we assume an electrostatic potential as a surface potential,

$$\phi(r,z)|_{r=R}=\phi_s(z). \tag{3}$$

ii) At the central axis of the cylinder channel, the electric field is zero,

$$\left.\frac{\partial\phi(r,z)}{\partial r}\right|_{r=0}=0. \tag{4}$$

iii) At the interface between the gate oxide and the strained silicon, the electric field is continuous

$$\left.\frac{\partial\phi(r,z)}{\partial r}\right|_{r=R}=\frac{C'_{ox}}{\varepsilon_{ssi}}\left[V_{gs}-(V_{FB})_{ssi}-\phi_s(z)\right]. \tag{5}$$

Applying the boundary conditions from Eqs. (3)–(5) to Eq. (2), the coefficients can be obtained, and the solution of Eq. (2) can be expressed as

$$\phi(r,z)=\phi_s(z)-\frac{RC'_{ox}}{2\varepsilon_{ssi}}\left[V_{gs}-(V_{FB})_{ssi}-\phi_s(z)\right]+\frac{C'_{ox}}{2R\varepsilon_{ssi}}\left[V_{gs}-(V_{FB})_{ssi}-\phi_s(z)\right]r^2. \tag{6}$$

The electric field distribution along the r radius direction can be written as

$$E(r,z)=-\frac{d\phi(r,z)}{dr}=\frac{C'_{ox}r}{R\varepsilon_{ssi}}\phi_s(z), \tag{7}$$

where C'_{ox} is the capacitance of the gate oxide because the gate is all around the oxide. The capacitance $C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}$ can be modified into $C'_{ox}=\frac{\varepsilon_{ox}}{R\ln(1+t_{ox}/R)}$, V_{gs} is the voltage across the gate and the source, $\phi_s(z)$ is the surface potential of the interface between the gate and the oxide. ε_{ox} is the permittivity of the gate oxide. Because of the strain, $(V_{FB})_{ssi}$ is given by

$$(V_{FB})_{ssi}=(V_{FB})_{si}+\Delta V_{FB}, \tag{8}$$

where $(V_{FB})_{si}=\phi_M-\phi_{si}$,

$$\Delta V_{FB}=-\frac{(\Delta E_c)_{ssi}}{q}+\frac{(\Delta E_g)_{ssi}}{q}-V_T\ln\left(\frac{N_{vsi}}{N_{vssi}}\right),$$
$$\phi_{si}=\frac{\chi_{si}}{q}+\frac{(E_g)_{si}}{2q}+V_T\ln\left(\frac{N_c}{n_{isi}}\right),$$
$$V_T\ln\left(\frac{N_{vsi}}{N_{vssi}}\right)=V_T\ln\left(\frac{m^*_{hsi}}{m^*_{hssi}}\right)^{3/2}\approx 0.075x,$$
$$(\Delta E_c)_{ssi}=0.57x,\quad (E_g)_{ssi}=(E_g)_{si}-0.4x,$$

where $(V_{FB})_{ssi}$ and $(V_{FB})_{si}$ are the flat-band voltages of the strained silicon and silicon, respectively. ϕ_M is the metal gate work function. ϕ_{si} and ϕ_F are the work function and Fermi energy of the silicon, respectively. $V_T=kT/q$ is the thermal voltage, and n_{issi} is the intrinsic carrier concentration of the strained silicon. N_{vsi} and N_{vssi} are the effective density of states of the valence band of silicon and strained silicon, respectively. m^*_{hsi} and m^*_{hssi} are the hole effective mass of silicon and strained silicon, respectively. ΔE_c and ΔE_g are the conduction band offset and the band gap reduction of the strained silicon compared to the energy band of the silicon, respectively. x is the Ge mole fraction in $Si_{1-x}Ge_x$.

Substituting Eq. (6) into Eq. (1), we obtain the surface potential equation

$$\frac{\partial^2\phi_s(z)}{\partial z^2}-\alpha^2\phi_s(z)=\beta, \tag{9}$$

where

$$\alpha^2 = \frac{2C'_{\rm ox}}{R\varepsilon_{\rm ssi}}, \quad \beta = -\frac{qN_{\rm c}}{\varepsilon_{\rm ssi}} - \frac{2C'_{\rm ox}}{R\varepsilon_{\rm ssi}}\left[V_{\rm g} - (V_{\rm FB})_{\rm ssi}\right].$$

Equation (9) is a second-order differential equation, and the general solution can be written as

$$\phi_{\rm s}(z) = c_1 \exp(\alpha z) + c_2 \exp(-\alpha z) - \frac{\beta}{\alpha^2}. \tag{10}$$

The channel surface electric field along the z direction can be obtained as

$$E_{\rm s}(z) = -\frac{\partial \phi_{\rm s}(z)}{\partial z} = -c_1\alpha \exp(\alpha z) + c_2\alpha \exp(-\alpha z). \tag{11}$$

To calculate the coefficients c_1 and c_2, we use the following boundary conditions:

$$\phi_{\rm s}(z)|_{z=0} = \phi_{\rm s}(0) = -V_{\rm T}\ln\left(\frac{N_{\rm s}N_{\rm c}}{n_{\rm isi}^2}\right) + (\Delta V_{\rm bi})_{\rm ssi}, \tag{12}$$

$$\phi_{\rm s}(z)|_{z=L_{\rm g}} = \phi_{\rm s}(L_{\rm g}) = V_{\rm ds} + V_{\rm T}\ln\left(\frac{N_{\rm d}N_{\rm c}}{n_{\rm isi}^2}\right) + (\Delta V_{\rm bi})_{\rm ssi}, \tag{13}$$

where

$$(\Delta V_{\rm bi})_{\rm ssi} = -\frac{(\Delta E_{\rm g})_{\rm ssi}}{q} + V_{\rm T}\ln\left(\frac{N_{\rm vsi}}{N_{\rm vssi}}\right),$$

where $V_{\rm ds}$ is the drain voltage across the drain to source and $(\Delta V_{\rm bi})_{\rm ssi}$ is the variation of the built-in potential at the source-channel and drain-channel junctions.

By substituting Eqs. (12) and (13) into Eq. (10), the expressions of c_1 and c_2 are given by

$$c_1 = \left\{\frac{\left[-V_{\rm T}\ln\left(\frac{N_{\rm s}}{n_{\rm isi}^2}\right) + (\Delta V_{\rm bi})_{\rm ssi} + \frac{\beta}{\alpha^2}\right]\exp(\alpha L_{\rm g}) - \left[V_{\rm d} + V_{\rm T}\ln\left(\frac{N_{\rm d}}{n_{\rm isi}^2}\right) + (\Delta V_{\rm bi})_{\rm ssi} + \frac{\beta}{\alpha^2}\right]}{\exp(\alpha L_{\rm g}) - \exp(-\alpha L_{\rm g})}\right\}, \tag{14a}$$

$$c_2 = \left\{\frac{\left[V_{\rm ds} + V_{\rm T}\ln\left(\frac{N_{\rm d}}{n_{\rm isi}^2}\right) + (\Delta V_{\rm bi})_{\rm ssi} + \frac{\beta}{\alpha^2}\right] - \left[-V_{\rm T}\ln\left(\frac{N_{\rm s}}{n_{\rm isi}^2}\right) + (\Delta V_{\rm bi})_{\rm ssi} + \frac{\beta}{\alpha^2}\right]\exp(-\alpha L_{\rm g})}{\exp(\alpha L_{\rm g}) - \exp(-\alpha L_{\rm g})}\right\}. \tag{14b}$$

The threshold voltage is the gate voltage where the tunneling barrier width ($t_{\rm bw}$) from the valence band of the source region to the conduction band of the channel region starts to saturate with increasing applied gate bias. When $t_{\rm bw}$ is around 5–6 nm, significant electron tunneling occurs.[15] Thus, the threshold voltage is the gate voltage when the gate voltage at $z = t_{\rm bw}$ is equal to the surface potential $V_{\rm ds} + \phi_{\rm d}$, that is $V_{\rm th} = V_{\rm gs}$.

$$c_1 \exp(\alpha t_{\rm bw}) + c_2 \exp(-\alpha t_{\rm bw}) - \frac{\beta}{\alpha^2} = V_{\rm ds} + V_{\rm T}\ln\left(\frac{N_{\rm d}N_{\rm c}}{n_{\rm issi}^2}\right). \tag{15}$$

By substituting Eqs. (14a) and (14b) into Eq. (15), $V_{\rm th}$ can be obtained as

$$V_{\rm th} = V_{\rm gs} = -\frac{qR^2N_{\rm c}\ln\left(1+\frac{t_{\rm ox}}{R}\right)}{2\varepsilon_{\rm ox}} - \frac{\delta_2 Q + P\delta_3 - \delta_1 Q}{\delta_1 - \delta_2 - \delta_3} + (V_{\rm FB})_{\rm ssi}, \tag{16}$$

where

$$\delta_1 = \exp(\alpha L_{\rm g}) - \exp(-\alpha L_{\rm g}),$$
$$\delta_2 = \exp(\alpha t_{\rm bw}) - \exp(-\alpha t_{\rm bw}),$$
$$\delta_3 = \exp(\alpha L_{\rm g} - \alpha t_{\rm bw}) - \exp\left[-(\alpha L_{\rm g} - \alpha t_{\rm bw})\right],$$
$$P = -V_{\rm T}\ln\left(\frac{N_{\rm s}N_{\rm c}}{n_{\rm isi}^2}\right) + (\Delta V_{\rm bi})_{\rm ssi},$$
$$Q = V_{\rm ds} + V_{\rm T}\ln\left(\frac{N_{\rm d}N_{\rm c}}{n_{\rm isi}^2}\right) + (\Delta V_{\rm bi})_{\rm ssi}.$$

3. Result and discussion

The analytical model is verified by comparing the model results with Sentaurus TCAD simulation results. To obtain a more accurate simulation result, the nonlocal Kane's BTBT model, band gap narrowing model, and SRH recombination model are used in the Sentaurus TCAD tools. The doping concentrations of $N_{\rm s} = 10^{20}$ cm^{-3} in the p-type source region, $N_{\rm c} = 10^{17}$ cm^{-3}in the n-type channel, and $N_{\rm d} = 10^{19}$ cm^{-3} in the n-type drain region. The gate work function is $\Phi = 4.6$ eV, and the gate leakage current is neglected in all the Sentaurus TCAD simulations.

The analytical results of the channel surface potential distribution as well as comparison to the TCAD simulations results for the different gate voltages applied and the different Ge mole fractions of $x = 0.1$, $x = 0.2$, and $x = 0.3$ are shown in Figs. 3(a) and 3(b). It can be seen that, as x and the applied gate voltage increase, the channel surface potential increases at the source–channel or drain–channel junctions remain constant throughout the channel. However, there is a significant increase towards the source–channel junction where the electron tunneling occurs resulting in a steeper potential distribution. Good agreement between the analytical results and

TCAD simulation results is observed.

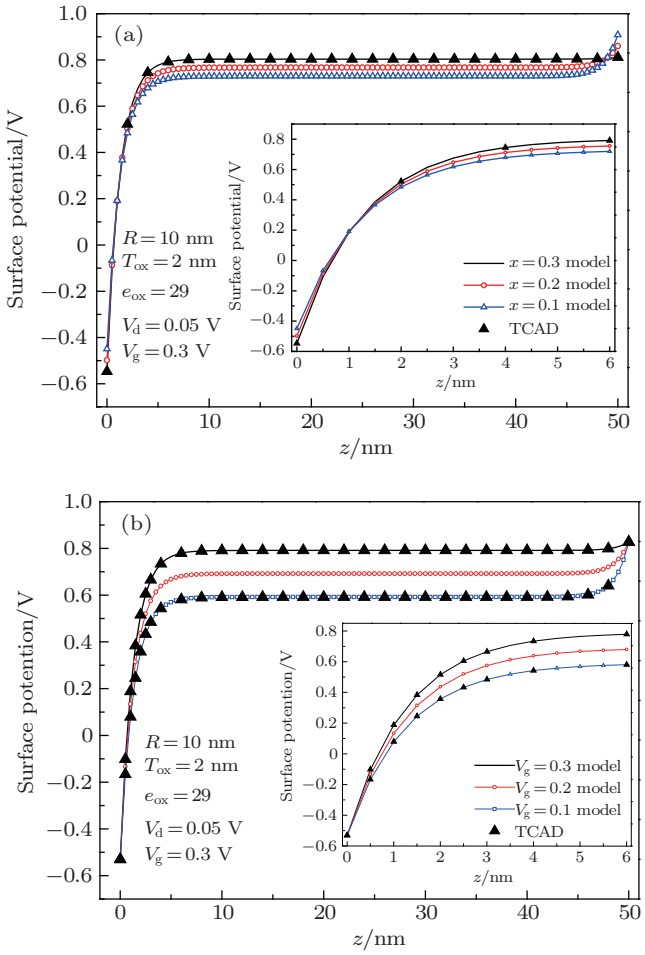


Fig. 3. (color online) (a) Surface potential distribution along with the channel for different Ge mole fractions x. (b) Surface potential distribution along with the channel for the different gate voltage.

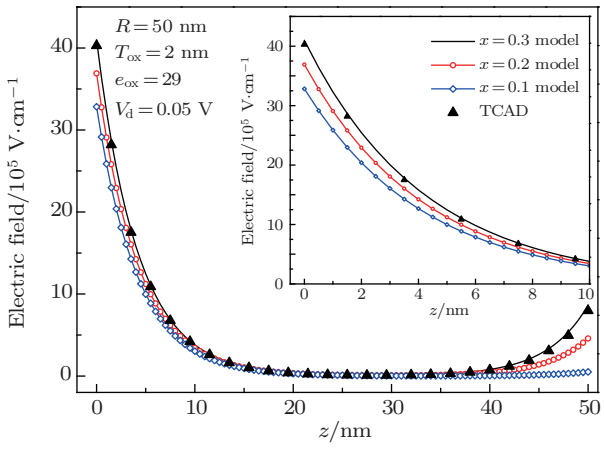


Fig. 4. (color online) Electric field distribution along the channel for the different Ge mole fractions x.

Figure 4 shows the electric field distribution along the channel for the different Ge mole fractions of $x=0.1$, $x=0.2$, and $x=0.3$. This figure describes that the electric field in the lightly doped channel increases as the Ge mole fraction x increases. The maximum point of the electric field is at the source–channel junction, which is attributed to the junction where the tunneling take place. The channel electric field between the source–channel and drain–channel junction remains constant and is approximately zero. Good agreements between the analytical and simulations results are observed.

To verify the threshold voltage analytical model, a TCAD simulation was used. The model threshold voltage is extracted using the peak transconductance method. In Figs. 5–8, the variation of the threshold voltage with the Ge mole fraction x, gate dielectric permittivity, gate oxide thickness, and gate length are shown.

Figure 5 illustrates the variation of the threshold voltage with the Ge mole fraction x. We can see that the threshold voltage decreases almost linearly with increasing Ge mole fraction x. This reduction can be attributed to a decrease of the flat-band voltage and the built-in potential barriers in the source-channel or drain-channel junctions, and an increasing tunneling probability of the electrons. The threshold voltage obtained from the analytical model tracks well with the TCAD results.

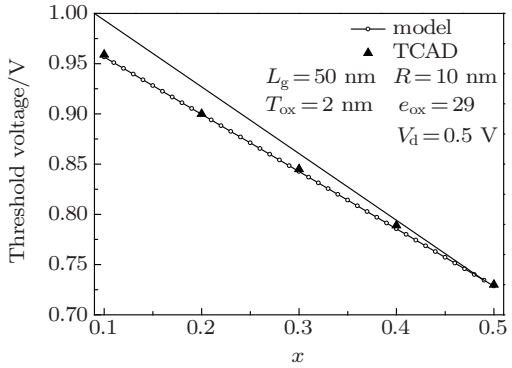


Fig. 5. Variation of threshold voltage with the Ge mole fraction x in $Si_{1-x}Ge_x$.

The variation of threshold voltage for different values of gate oxide permittivity and gate oxide thickness with the Ge mole fraction $x=0.1$, $x=0.2$, and $x=0.3$ are shown in Figs. 6 and 7, respectively. Both figures show that the threshold voltage decreases with increasing Ge mole fraction x, which is due to the strain.

In Fig. 6, when the gate oxide permittivity is scaled down from 30 nm to 3 nm, the threshold voltage increases. The reason is that a higher gate oxide permittivity increases the gate control of the tunnel junction, resulting in a decrease of the threshold voltage. Therefore, to achieve the lower threshold voltage in a GAA TFET, usually, a higher gate oxide permittivity is employed. In Fig. 7, the threshold voltage increases linearly as the gate oxide thickness increases. By decreasing the gate oxide thickness, the gate control of the barrier width is increased in the tunnel junction, and it helps to decrease the value of the threshold voltage.

Therefore, in order to obtain improved characteristics of the GAA TFET, a high k material and thinner oxide layer is chosen. The proposed model results coincide well to those of the TCAD simulation results.

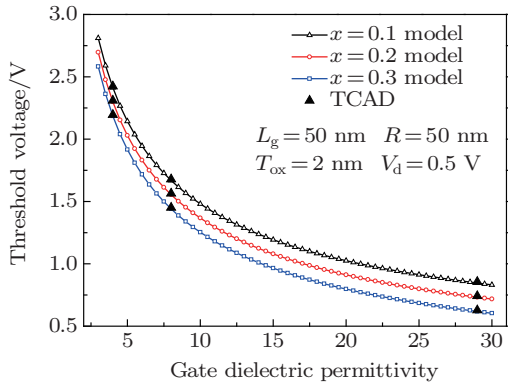


Fig. 6. (color online) Variation of the threshold voltage with the gate oxide permittivity.

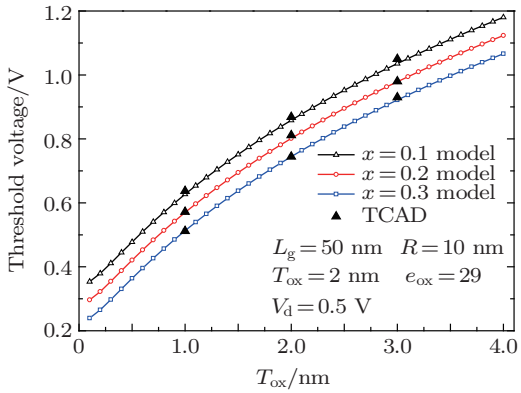


Fig. 7. (color online) Variation of the threshold voltage with the oxide thickness.

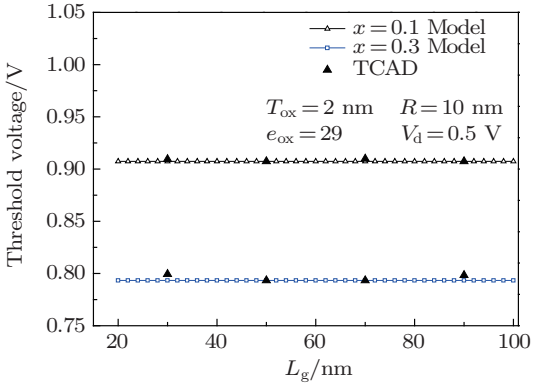


Fig. 8. (color online) Variation of the threshold voltage with the gate length.

The variation of the threshold voltage with the length of the gate at constant drain and gate voltages is shown in Fig. 8. The threshold voltage curve remains constant when the length of the gate increases. This is due to the fact that the electric field is maximum at the source-channel junction and is independent of the gate length. On the other hand, the channel acts like a resistance in the case of a TFET. If the length of the gate increases, then the channel resistance will increase. Therefore, to reduce the channel resistance, the length of the gate is set to 50 nm.

4. Conclusion and perspectives

In summary, an analytical threshold voltage model that is based on the surface potential and electric field models obtained by solving the 2D polar coordinate Poisson's equation in the channel for a strained silicon GAA TFET has been developed. Furthermore, it can be observed that the proposed model can predict the trend of the threshold voltage with the key TFET parameters. Our results show that the threshold voltage decreases with increasing Ge mole fraction x, and the gate dielectric permittivity increases with increasing gate oxide thickness. Superior to the MOSFET device, the threshold voltage of the TFET remains constant when the length of the gate increases. Therefore, to obtain improved characteristics of the GAA TFET, a high-k material, and thin oxide layer, and strain for $x = 0.3$ in $Si_{1-x}Ge_x$ can be chosen. The proposed models provide an effective reference for the design and application of the GAA TFET.

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