Parasitic effects of air-gap through-silicon vias in high-speed three-dimensional integrated circuits*

Xiaoxian Liu(刘晓贤), Zhangming Zhu(朱樟明)†, Yintang Yang(杨银堂), Ruixue Ding(丁瑞雪), and Yuejin Li(李跃进)

School of Microelectronics, Xidian University, Xi'an 710071, *China*

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In this paper, ground-signal-ground type through-silicon vias (TSVs) exploiting air gaps as insulation layers are designed, analyzed and simulated for applications in millimeter wave. The compact wideband equivalent-circuit model and passive elements (RLGC) parameters based on the physical parameters are presented with the frequency up to 100 GHz. The parasitic capacitance of TSVs can be approximated as the dielectric capacitance of air gaps when the thickness of air gaps is greater than 0.75 μm. Therefore, the applied voltage of TSVs only needs to achieve the flatband voltage, and there is no need to indicate the threshold voltage. This is due to the small permittivity of air gaps. The proposed model shows good agreement with the simulation results of ADS and Ansoft's HFSS over a wide frequency range.

Keywords: three-dimensional integrated circuits, through-silicon vias, air gaps, high frequency

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1. Introduction

Physical constraints and technological challenges beyond 22-nm node now set back the further development of Moore's Law of scaling the feature size of transistor.[1–7] The interconnect performance becomes a key challenge to achieving the overall performance of a chip. Compared with conventional circuits, through-silicon vias (TSVs) for vertical interconnection are able to achieve shorter wiring paths, higher interconnect densities, and smaller foot prints. Therefore, the technology of three-dimensional integrated circuits (3D ICs) has the potential to significantly improve the system functionality and performance.[1–7]

With the rapid development of silicon technologies, the operating frequency of 3D ICs has been progressively expanded into millimeter-wave (mmW) and terahertz (0.1–10 THz) regions.[8] The heterogeneous integration and high operating speed make the signal integrity (SI) and the coupling noise induced by massive TSVs be major concerns for 3D IC systems.[5] This is especially true for high frequency bands, in which the parasitic parameters of the TSV play more important roles in circuits. Therefore, the accurate extraction of parasitic effects of TSVs is vital for the design and assessment of 3D systems.[2,5,6] The parasitic effects of SiO_2-based TSVs in high-frequency 3D IC systems are put forward. The passive elements (RLGC) of TSV have been proposed as functions of the physical parameters and material characteristics, while the TSV is in GS-mode.[9–14] Up to now, few published works on TSV technology have been focused on the TSV transmission structure that is in GSG-mode.[15–19] Coplanar waveguide (CPW) passive elements in the GSG-mode are important technologies to realize low-cost millimeter-wave ICs,[20,21] which can also be applied to high-frequency 3D ICs. Therefore, the three-TSV system is needed to interconnect CPW on different 3D IC layers.[15] What is more, the *S*-parameters of GSG-mode TSVs show better characters than those of GS-mode TSVs, especially in the millimeter frequency range.[16] It is obvious that the S_{11} can be reduced remarkably by using GSG-type TSVs, due to the better shielding effects of the two ground TSVs around the signal TSV. Therefore, GSG-type TSVs for microwave applications are analyzed in this paper. The *S*-parameters of the GSG-type TSVs are measured, but the exact parasitic effects of TSVs are not abstracted. In Ref. [17], we have investigated the parasitic effects and schematic equivalent electrical model of the GSG-mode TSV pair. However, the simplified T- or π-model of the GS- or GSG-model TSVs are needed during the design of 3D IC systems and the equivalent electrical model in Ref. [17] is difficult to reduce into a T- or π-model. Therefore, we further study it and come up with another schematic equivalent electrical model, which can be simplified into a π-model in this paper.

The schematic equivalent electrical model and simplified π-model of the GSG-mode TSV pair are established for microwave 3D ICs with operating frequency up to 10 GHz, which is based on the design physical parameters and the operating frequency in this paper. The extractions of different parasitic effects of air-gap TSVs are introduced in Section 2. Due to the low dielectric constant of air gaps, the parasitic capacitance of the air-gap TSV shows different characteristics from the conventional SiO_2-based TSV structure. In Section 3, an

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†Corresponding author. E-mail: zmyh@263.net

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equivalent electrical model and lumped RLGC parameters of the GSG-type TSV pair are given, respectively. These are verified by the simulations including ADS and Ansoft's HFSS, which show good agreement and verify our analysis.

2. Parasitic effects of air-gap TSVs

The structure of GSG-type TSVs is shown in Fig. 1, including a signal TSV and two ground TSVs surrounded by air gaps. The equivalent circuit model using RLCG components is developed based on the geometric and material information up to 100 GHz. Since the length of TSV is short enough when compared with the wavelength of operating frequency, the lumped model is used. Parasitic effects of the inter-metal-dielectric (IMD) layer and the bottom oxide layer are also taken into account. Design parameters of TSV are listed in Table 1. The parasitic effects of TSVs, such as resistance, capacitance, and inductance, all function with materials and the geometry design. These are vital parameters assessing the performance of TSVs and 3D integration. Among these characteristics, the capacitance, determined by the dielectric constants of the insulation layer, has the most predominant influence. All propagation delay, power consumption, and crosstalk increase almost proportionally to the TSV capacitance. Low capacitance, using materials with low dielectric constants as insulation layers, is of great importance for high-performance of 3D systems.[19–22] Air ($\varepsilon_r = 1$ at $T = 273$ K)[19,20] and benzocyclobutene (BCB) polymer ($\varepsilon_r = 2.6$)[21] are used as insulation layers instead of the conventional silicon dioxide (SiO_2) ($\varepsilon_r = 4$). The integration of low-κ (2.8) liner reduces the TSV capacitance by 27.6%.[22] In this paper, we use the air as insulator layers of TSVs, and the oxide silicon and Cu are selected as the insulation and redistribution layers, respectively.

Table 1. Design parameters of the TSV.

Parameter	Symbol	Value/μm
TSV radius	r_{TSV}	5
TSV height	h_{TSV}	60
TSV-to-TSV pitch	p_{TSV}	40
air-gap thickness	t_{air}	1
IMD height	h_{IMD}	2
bottom SiO_2 thickness	h_{ox}	2

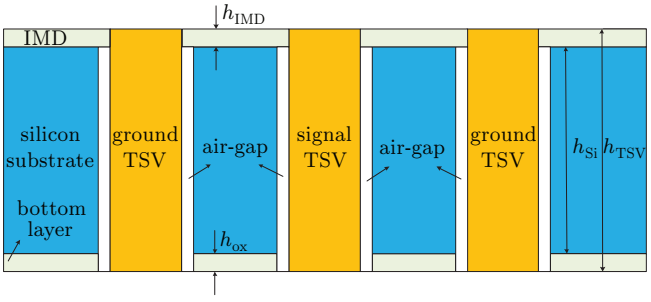


Fig. 1. (color online) Cross-sectional view of the GSG-type TSV structure with structural parameters.

2.1. The resistance of TSV plug

Since the resistance of TSVs represents a parasitic contribution to the signal delay in ICs, it is necessary to extract the resistance of the TSV metal plug. The analytical expression of the dc resistance R_{TSV_dc} is given by[9]

$$R_{TSV_dc} = \frac{h_{TSV}\rho_{TSV}}{\pi r_{TSV}^2}. \tag{1}$$

However, as the operating frequency goes up, the skin and proximity effects emerge, which cannot be ignored in the calculation of the TSV resistance. Therefore, the resistance of TSV, R_{TSV}, is given by[14]

$$R_{TSV} = \sqrt{R_{TSV_dc}^2 + R_{TSV_ac}^2}, \tag{2}$$

where R_{TSV_ac} is the ac resistance of the TSV, given by

$$R_{TSV_ac} = \frac{k_p h_{TSV}\rho_{TSV}}{2\pi r_{TSV}\delta}, \tag{3}$$

where $k_p = 1.5$ is a correction factor determined by the proximity effect and the ratio $p_{TSV}/2r_{TSV}$;[14,23] δ is the skin depth and is calculated by

$$\delta = \sqrt{\frac{\rho_{TSV}}{\pi f \mu_0 \mu_{rTSV}}}, \tag{4}$$

where ρ_{TSV} and μ_{rTSV} are the resistivity and relative permeability of the Cu plug, respectively, and $\mu_0 = 4\pi \times 10^{-7}$ H/m is the permeability of free space.

2.2. The inductance of TSVs

As the operating frequency increases, the influence of parasitic inductance becomes more and more remarkable. For the GSG-type TSV pair, the current flowing through the middle signal TSV separates into two ground TSVs. This forms two current loops among the three TSVs. Therefore, the current of the ground TSV is half of the signal TSV with an inverted phase. The concept of partial inductance is explored in this paper to model the inductive effect of TSVs in highspeed circuits.[24] As the current tends to move toward the surface of TSVs with increased frequency, the internal inductance goes to zero and is ignored in our calculations. Partial inductances, including self- and mutualinductances, are decided by TSV design parameters such as TSV pillar diameter, length, and pitch between two TSV pillars as[24]

$$L_{self} = a\left[\ln\left(b+\sqrt{b^2+1}\right) - \sqrt{1+1/b^2} + 1/b\right], \tag{5}$$

$$M_1 = a\left[\ln\left(c+\sqrt{c^2+1}\right) + 1/c - \sqrt{1/c^2+1}\right], \tag{6}$$

$$M_2 = a\left[\ln\left(c/2+\sqrt{c^2/4+1}\right) + 2/c - \sqrt{4/c^2+1}\right], \tag{7}$$

where L_{self} is the self-inductance; M_1 is the mutual inductance between signal TSV and ground TSV; M_2 is the mutual inductance between the two ground TSVs; $a = \mu_0\mu_{r,TSV}h_{TSV}/2\pi$;

$b = h_{\mathrm{TSV}}/r_{\mathrm{TSV}}$; $c = h_{\mathrm{TSV}}/(r_{\mathrm{TSV}} + p_{\mathrm{TSV}})$. The loop inductance of GSG-type TSVs with frequency up to gigscale[25] can then be acquired as

$$L_{\mathrm{Loop}} = 1.5L_{\mathrm{self}} - 2M_1 + 0.5M_2 + R_{\mathrm{TSV}}/2\pi f. \quad (8)$$

The inductance of every single TSV, $L_{\mathrm{TSV,signal}}$ and $L_{\mathrm{TSV,ground}}$ can be expressed as

$$L_{\mathrm{TSV,signal}} = L_{\mathrm{self}} - M_1 + R_{\mathrm{TSV}}/2\pi f, \quad (9)$$

$$L_{\mathrm{TSV,ground}} = 0.5L_{\mathrm{self}} - M_1 + 0.5M_2 + R_{\mathrm{TSV}}/2\pi f. \quad (10)$$

2.3. The capacitance of TSVs

A TSV assumes a metal–insulator-semiconductor (MIS) capacitance structure. The copper TSV is surrounded by a dielectric layer for dc isolation (air gaps in this paper). This isolation dielectric is surrounded by a depletion region when the TSV gate bias increases, as shown in Fig. 2. Parasitic capacitance of the TSV is investigated by the following analysis.

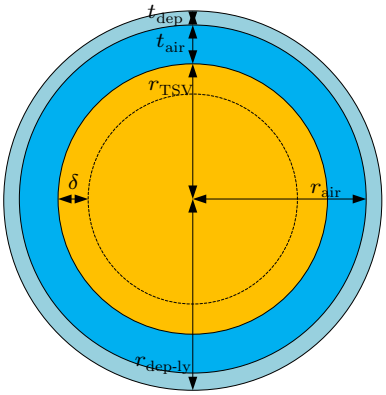


Fig. 2. (color online) Cross section view of a single TSV.

The capacitance of TSV, C_{TSV} is the series combination of the dielectric capacitance C_{die} and depletion capacitance C_{dep}. Analytical expression for C_{TSV} can be obtained by solving Poisson's equation in a cylindrical coordinate system. The MIS capacitance of TSV is in the accumulation region when $V_{\mathrm{TSV}} < V_{\mathrm{FB}}$, where V_{FB} denotes the flat-band voltage. The capacitance in this case is the cylindrical dielectric capacitance given by[6]

$$C_{\mathrm{TSV}} = C_{\mathrm{die}} = \frac{2\pi\varepsilon_0\varepsilon_{\mathrm{r,die}}h_{\mathrm{die}}}{\ln\left(r_{\mathrm{die}}/r_{\mathrm{TSV}}\right)}, \quad (11)$$

where $\varepsilon_{\mathrm{r,die}}$ and h_{die} are the relative permittivity and the height of the dielectric layer, respectively. As the TSV gate bias increases into the range of $V_{\mathrm{FB}} \le V_{\mathrm{TSV}} \le V_{\mathrm{Th}}$, the depletion region emerges, where V_{Th} is the threshold voltage. At high frequency and with a fast sweeping ramp in the direction toward strong inversion, the semiconductor does not have enough time to come to equilibrium even with the large-signal variation.[26] Thus the depletion width does not increase beyond $t_{\max}$, and the minimum depletion capacitance C_{dep} can be obtained by the maximum radius of depletion region as

$$C_{\mathrm{dep\,min}} = \frac{2\pi\varepsilon_0\varepsilon_{\mathrm{r,Si}}h_{\mathrm{Si}}}{\ln\left(r_{\max}/r_{\mathrm{die}}\right)}. \quad (12)$$

The total minimal capacitance of TSV C_{TSV} is the series combination of dielectric and depletion capacitance, which is given by

$$C_{\mathrm{TSV}} = \left(1/C_{\mathrm{die}} + 1/C_{\mathrm{dep\,min}}\right)^{-1}. \quad (13)$$

Figure 3 contrasts per-unit-length of dielectric capacitance, C_{die}, as a function of the thickness of dielectric layer. In order to better understand the advantage of air-gap structure TSV, values of C_{die} using SiO_2 as the dielectric layer are also shown in Fig. 3. We find that C_{die} of the air dielectric layer is much smaller compared with the one of SiO_2, especially when the thickness of the dielectric t_{die} is in the small range. It is due to that the dielectric constant of air is much smaller than that of SiO_2.

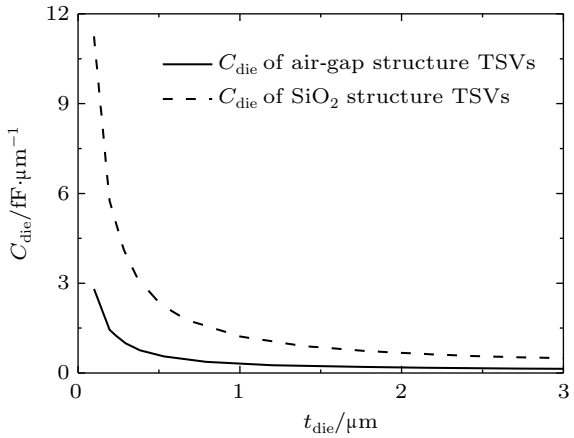


Fig. 3. Per-unit-length of C_{TSV} as a function of the thickness of the dielectric layer t_{die} of air-gap and SiO_2-based TSV.

The total capacitance of air-gap structure TSV, C_{TSV} as a function of the applied voltage $V_{\mathrm{TSV}}$is shown in Fig. 4(a). In order to have a better understanding of the merits of air-gap TSV, C_{TSV} of SiO_2-based TSV is also shown in Fig. 4(b) for comparison. Since the dielectric layer of SiO_2 is about 0.1–0.2 μm in the state-of-the-art TSV technology, we assume $t_{\mathrm{SiO_2}} = t_{\mathrm{air}} = 1$ μm for comparison. It is shown that the capacitance of air-gap TSV is much less than that of SiO_2-based TSV, which shows a 71% reduction when V_{TSV} achieves V_{TH}. Further, the C_{TSV} of air-gap TSV nearly equals to the dielectric layer capacitance C_{air}, which shows only 5% difference. This is due to the fact that C_{air} is much lower than the depletion layer capacitance C_{dep}; C_{TSV} is the series combination of C_{air} and C_{dep}. Therefore, C_{TSV} can be approximated to C_{air} when the applied voltage to the air-gap TSV reaches flatband voltage V_{FB}. There is no need to specify the threshold voltage V_{Th} and depletion capacitance in a certain error range. These phenomena are studied by further quantitative analysis.

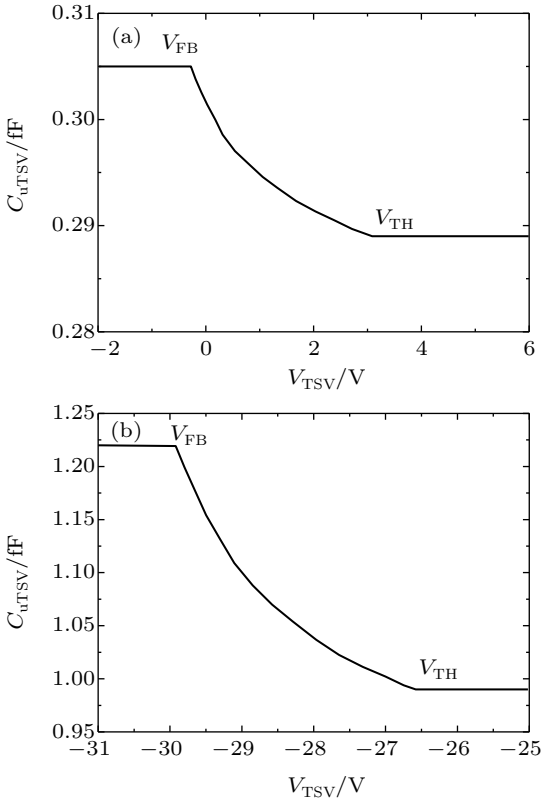


Fig. 4. Per-unit-length of C_{TSV} as a function of the applied voltage V_{TSV} for TSV: (a) air-gap TSV. (b) SiO_2-based TSV.

In our research, the difference of C_{TSV} and C_{die} is defined by Δ and given by

$$\Delta = \frac{C_{die} - C_{TSV}}{C_{die}}. \tag{14}$$

From Fig. 2, we know that $r_{die} = r_{TSV} + t_{die}$, $r_{dep} = r_{TSV} + t_{die} + t_{max}$, then C_{die} and C_{depmin} are calculated as

$$C_{die} = \frac{2\pi\varepsilon_0\varepsilon_{rdie}h_{die}}{\ln(1 + t_{die}/r_{TSV})}, \tag{15}$$

$$C_{depmin} = \frac{2\pi\varepsilon_0\varepsilon_{r,Si}h_{Si}}{\ln(1 + t_{dep}/(r_{TSV} + t_{die}))}. \tag{16}$$

Submitting Eqs. (15) and (16) into Eq. (14), we can obtain

$$\Delta = \frac{\ln\left(1 + \frac{t_{dep}}{r_{TSV}+t_{die}}\right)}{\ln\left(1 + \frac{t_{dep}}{r_{TSV}+t_{die}}\right) + \frac{\varepsilon_{r,Si}}{\varepsilon_{rdie}}\ln\left(1 + \frac{t_{die}}{r_{TSV}}\right)}, \tag{17}$$

from which, we can find that Δ is the function of the dielectric layer thickness t_{die}, the radius of TSVs r_{TSV}, and the thickness of depletion region t_{dep}. Values of Δ as a function of dielectric layer thickness at different radii of TSVs and depletion region thicknesses are shown in Fig. 5. To obtain a better understanding of the advantage of air-gap structure TSVs, Δ of SiO_2 based TSV is also shown in Fig. 5. We find that Δ rapidly drops with the increase of t_{die} due to that C_{die} goes up and C_{dep} goes down as the increase of t_{die} both for air-gap and SiO_2 structure TSVs, and Δ becomes small enough and can be ignored when t_{die} increases into a certain range. In addition, the influence of t_{dep} changes on Δ becomes significant when t_{die} is almost equal to t_{dep} and Δ also increases with the increase of t_{dep}. What is more, the variation of r_{TSV} has very finite influnece on Δ, which can be ignored.

Assume that the maximum value of Δ is 5% in this paper. For the air-gap structure TSV with $r_{TSV} = 5$ μm, Δ equals to 5% when the thickness of the air gap achieves 0.75 μm and continues to reduce as t_{air} increases. This also means that we can simplify the C_{TSV} of air-gap structure TSV to C_{air} as long as the thickness of air gap is greater than 0.75 μm and the applied voltage V_{TSV} achieves V_{FB}. There is no need to distinguish V_{Th}. However, for SiO_2 structure TSV, Δ reduces to 5% when the thickness of SiO_2 is 2.65 μm due to the large permittivity of SiO_2. While t_{SiO_2} is about 0.1 μm at the state-of-the art TSV technology, the difference of C_{TSV} and C_{SiO_2} is 63%. This also means that it is necessary to calculate both V_{Th} and V_{FB} to determine the total capacitance for SiO_2 structure TSV.

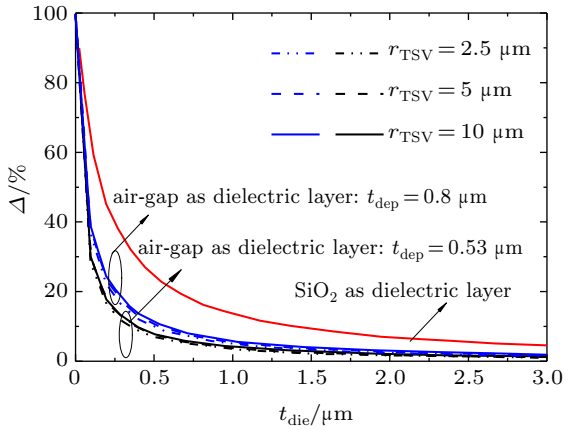


Fig. 5. (color online) Values of Δ as a function of dielectric layer thickness at different radii of TSV and different thicknesses of depletion regions.

2.4. The capacitance and conductance of the silicon substrate

The capacitance and conductance of the silicon substrate between TSVs, C_{Si} and G_{Si} are respectively modeled as[27]

$$C_{Si} = \frac{\pi\varepsilon_0\varepsilon_{r,Si}h_{Si}}{\ln\left[p_{TSV}/(2r_{TSV}) + \sqrt{\left(p_{TSV}/(2r_{TSV})\right)^2 - 1}\right]}, \tag{18}$$

$$G_{Si} = (\sigma_{Si}/\varepsilon_{Si} + \omega\tan\delta_{c,Si})C_{Si}, \tag{19}$$

where $\tan\delta_{c,Si} = 0.004$ is the loss tangent used to characterize the loss in dielectrics. The minimum G_{Si} equals to 6.3545×10^{-4} with $f = 0$, and the maximum G_{Si} is 6.5225×10^{-4} when the frequency is up to 100 GHz. There is only a 2.6% increase with the frequency increasing from zero to 100 GHz, which is due to $\omega\tan\delta_{c,Si}C_{Si}$ being much smaller than $C_{Si}\sigma_{Si}/\varepsilon_{Si}$. Therefore, the effect of operating frequency on the conductivity of silicon substrate can be ignored, and equation (19) can by simplified to

$$G_{Si} = \sigma_{Si}C_{Si}/\varepsilon_{Si}. \tag{20}$$

There are other parasitic capacitances which are formed between TSVs and the silicon substrate in the IMD and bottom oxide layer, $C_{\rm IMD}$ and $C_{\rm ox}$. They are given respectively as[14]

$$C_{\rm IMD} = \frac{\pi\varepsilon_0\varepsilon_{\rm r,ox}h_{\rm IMD}}{\cosh^{-1}(p_{\rm TSV}/(2r_{\rm TSV}))}, \tag{21}$$

$$C_{\rm ox} = \frac{\pi\varepsilon_0\varepsilon_{\rm r,ox}h_{\rm ox}}{\cosh^{-1}\left(p_{\rm TSV}/(2r_{\rm TSV})\right)}. \tag{22}$$

3. RLGC parameters

The schematic equivalent electrical model of GSG-type TSVs can reduce to a simplified π-type transmission-line model, as shown in Fig. 6, which is simulated by advanced digital system (ADS) software. The RLGC parameters of the π-type model in this paper are given by

$$R = R_{\rm TSV}, \tag{23}$$

$$L = L_{\rm Loop}, \tag{24}$$

$$G = \frac{\omega^2 mp + nq}{(\omega m)^2 + n^2}, \tag{25}$$

$$C = \frac{np - mq}{(\omega m)^2 + n^2}, \tag{26}$$

where m, n, p, and q are given by

$$m = C_{\rm TSV} + 3C_{\rm Si}, \quad n = 6G_{\rm Si},$$

$$p = 12C_{\rm IMD}G_{\rm Si} + 2C_{\rm TSV}G_{\rm Si},$$

$$q = -\omega^2(C_{\rm TSV}C_{\rm Si} + C_{\rm TSV}C_{\rm IMD} + 6C_{\rm IMD}C_{\rm Si}).$$

Ansoft's HFSS is employed as a 3D EM field solver, which is based on the finite element method (FEM).[28] The lumped components of RLGC in HFSS can be obtained by

$$R = {\rm Re}\left(Z_0\frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}}\right), \tag{27}$$

$$L = \frac{\rm Im}{\omega}\left(Z_0\frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}}\right), \tag{28}$$

$$G = {\rm Re}\left(\frac{1}{Z_0}\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}\right), \tag{29}$$

$$C = \frac{\rm Im}{\omega}\left(\frac{1}{Z_0}\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}\right), \tag{30}$$

where $\omega = 2\pi f$ is the angular frequency; Z_0 is the port impedance assumed to be 50 Ω.

The S_{11} and S_{21} of GSG-type TSV using air gaps as the dielectric layer are shown in Fig. 7. The solid lines are S_{11} and S_{21} of schematic equivalent electrical model obtained by ADS simulation. The scatter lines are S_{11} and S_{21} of the 3D model obtained by HFSS simulation. The solid lines accord well with the scatter ones, which verify the accuracy of our proposed schematic equivalent electrical model of GSG-type TSV. Per-unit-length of RLGC parameters of the proposed model and HFSS simulation results as a function of frequency are shown in Fig. 8. Curves of the proposed model coincide well with the HFSS simulation. The error between these is less than 5% with the operating frequency up to 100 GHz.

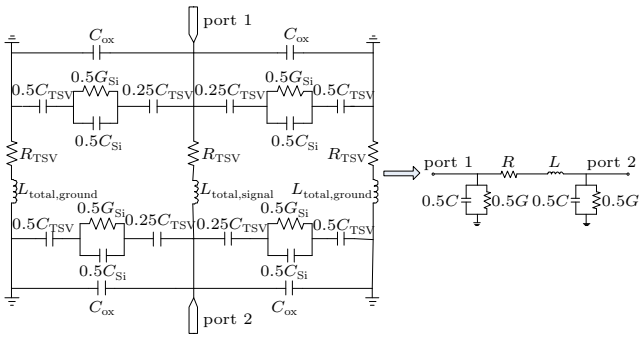


Fig. 6. Schematic equivalent electrical model and the π-type model of GSG TSV pair with air gaps as insulator layers.

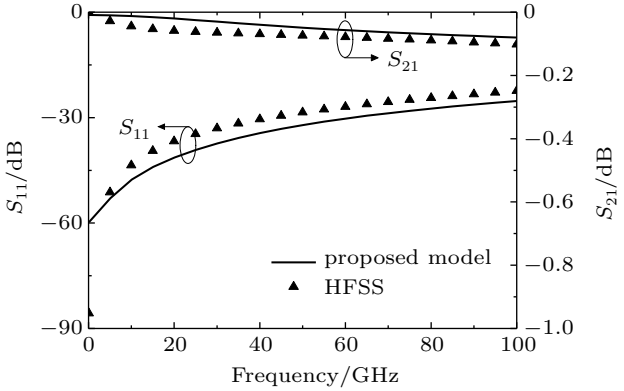


Fig. 7. S_{11} and S_{21} of GSG-type TSV.

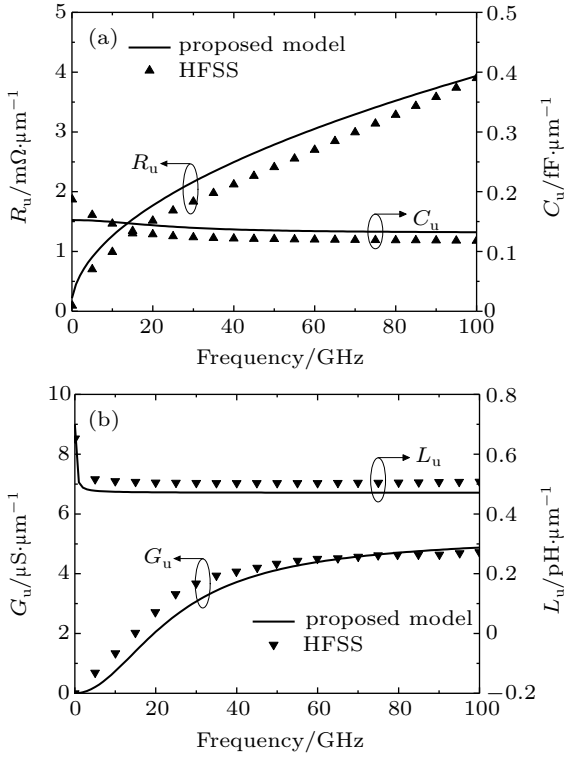


Fig. 8. The per-unit-length of RLGC parameters of GSG-type TSV: (a) $R_{\rm u}$ and $C_{\rm u}$; (b) $G_{\rm u}$ and $L_{\rm u}$.

4. Conclusion

Compared with SiO_2, air gaps were chosen as insulator layers of TSVs due to the low permittivity in this paper. Since the electrical characteristics of GSG-type TSVs used in high-speed circuits are still obscure, the investigation of GSG-type TSVs surrounded by air gaps are performed. Precise electrical models of parasitic effects are given in this paper. The parasitic capacitance of TSV can be approximated as the dielectric capacitance of air gaps when the thickness of air gaps is greater than 0.75 μm and the applied voltage to the TSV achieves flatband voltage. There is no need to indicate the threshold voltage. The per-unit-length of RLGC parameters of the GSG-type TSV is modeled and verified by the measurements and simulation of Ansoft's HFSS and ADS in a wideband frequency range, which shows good accuracy of the proposed model.

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