Threshold resistance switching in silicon-rich SiO_x thin films*

Da Chen(陈达) and Shi-Hua Huang(黄仕华)†

Physics Department, Zhejiang Normal University, Zhejiang 321004, *China*

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Si-rich SiO_x and amorphous Si clusters embedded in SiO_x films were prepared by the radio-frequency magnetron cosputtering method and high-temperature annealing treatment. The threshold resistance switching behavior was achieved from the memory mode by continuous bias sweeping in all films, which was caused by the formation of clusters due to the local overheating under a large electric field. Besides, the *I–V* characteristics of the threshold switching showed a dependence on the annealing temperature and the SiO_x thickness. In particular, formation and rupture of conduction paths is considered to be the switching mechanism for the 39 nm-SiO_x film, while for the 78 nm-SiO_x film, adjusting of the Schottky barrier height between insulator and semiconductor is more reasonable. This study demonstrates the importance of investigation of both switching modes in resistance random access memory.

Keywords: threshold resistance switching, silicon-rich SiO_x thin film, annealing

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1. Introduction

The first report about the reversible resistance switching (RS) effect in binary metal oxides was published about fifty years ago. With the decrease of the gate oxide thickness, the traditional flash memory is facing challenges in large storage, low power consumption, fast speed, long retention, best endurance, and three-dimensional integration due to its larger leakage current.[1] Therefore, the technique based on the reversible memory RS effect has attracted wide attention all over the world, which is one of the most possible candidates applied in the next generation nonvolatile memory because of its above features.[2] However, there is another RS effect called threshold RS, which has not been observed widely in materials. The difference between the two kinds of RS effects is whether they have two stable resistance states without external applied bias.[3–7] Furthermore, investigating the RS mechanism of different RS methods is significant to clarify the RS behaviors.

Several materials, such as NiO,[3,4,8] amorphous Ta_2O_5 film,[9] SiO_2,[10] and amorphous NbO_x film,[11] have been reported to show the coexistence of bi-stable memory RS and mono-stable threshold RS in one device by changing some fabricating or testing conditions. Silicon-rich oxide (SRO) films, also known as semi-insulating polysilicon films doped with oxygen atoms, have been reported in the using of passivating material for silicon electronic devices and integral part of nonvolatile.[12–18] Some researchers have found that SRO films are composed mostly of amorphous Si and SiO_x in a two-phase network, which means that there exist a number of Si–O–Si bonds and some Si–Si bonds.[19] If a bias is applied to the film, the formation and modification of silicon nanocrystal in the SiO_x matrix will take place through breaking Si–O bonds and gathering Si atoms to form Si clusters.[17] At the same time, a lot of Si atoms cannot bond with other atoms and, as a result, the films contain a high concentration of silicon dangling bonds (Si-DBs).[15] Therefore, RS based on the SRO films is mostly ascribed to the formation and rupture of nonmetallic conduction filaments consisted of Si nanocrystals or Si-DBs.[15–17] On the other hand, if SRO is firstly annealed at high temperature, the atoms will permute and combine again. The silicon clusters or particles will form, and the degree of silicon crystallization is depend on the annealing temperature and time.[20–22] The leakage current will be smaller due to the lower concentration of defects, which is beneficial for improving the resistance and the on/off ratio for the application in RRAM. Therefore, SRO films are employed to form metal/insulation/Si structures to study their RS effects. Moreover, the threshold resistance switching effect was firstly found in the SRO films in the electrical measurement. And the threshold voltage and current are smaller than those of the other reported materials.[3,10–12]

In this paper, we reported the threshold RS effect in silicon-rich SiO_x and annealed SiO_x. Firstly, we demonstrated the evolutionary process of the transformation from the memory to the threshold effect. Then, the effects of the film thickness and annealing temperature on the threshold RS behaviors were investigated. Finally, the conduction mechanism was employed to analyze the switching mechanism through fitting the current–voltage curves and combining with the previous researches about silicon-rich SiO_x films. Furthermore, the trans-

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†Corresponding author. E-mail: huangshihua@zjnu.cn

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formation process from memory mode to threshold mode was also investigated.

2. Experimental details

Silicon-rich SiO_x films were deposited by using the radio-frequency magnetron co-sputtering method. A sector piece of a Si wafer with a resistivity of $\sim 2\ \Omega$·cm was tightly stuck to a SiO_2 (99.99%) target with a diameter of 60 mm, and it was used as the co-sputtering target. A boron heavily-doped p-type Si wafer with a resistivity of $\sim 0.001\ \Omega$·cm was used as the substrate and bottom electrode (BE). Before deposition, the Si wafer and the substrate were processed by standard RCA cleaning. After drying by nitrogen gas, they were inserted immediately into the pretreatment chamber and the sputtering chamber of the magnetron sputtering deposition system, respectively. When the background pressure was better than 4.0×10^{-3} Pa, 10-min presputtering was carried out to clean the surface of the target and stabilize the glow discharge of argon gas (99.999%) under a power density of 3.5 W/cm^2 for each new deposition. During the deposition, the substrate temperature and the base pressure were maintained at 573 K and 0.5 Pa, respectively. Silicon-rich SiO_x thin films with different thicknesses were obtained. A part of the deposited films were thermally annealed for 60 min in high-purity argon atmosphere at various temperatures. Finally, Cu, the top electrode (TE, 500 nm, 1 mm in diameter), was defined by depositing Cu film using a thermal evaporator system to complete the full device structure. Figure 1 shows a schematic diagram of the Cu/SRO/Si device.

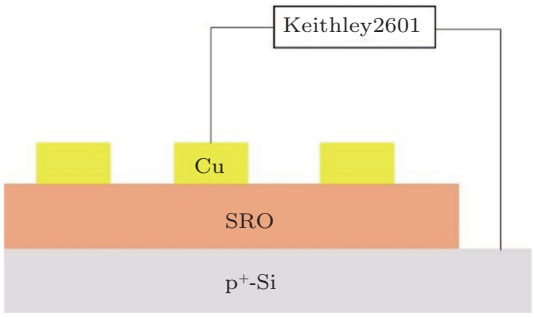


Fig. 1. (color online) Schematic diagram of the Cu/SRO/Si device.

The electrical characteristics of the Cu/SRO/Si devices were measured by a digital sources tester (Keithley 2601) at room temperature (RT). During the electrical measurement, the bias voltage was applied on the Cu electrode (TE) with the Si substrate (BE) grounded.

3. Results and discussion

First, we illustrate the transformation process of the transition from the memory mode to the threshold mode for the Cu/SRO/Si device with 39-nm thickness SRO film annealed at 1073 K, as shown in Fig. 2. For the first DC voltage sweeping, the bias voltage is swept in the sequence of $0 \to 10 \to 0 \to -10 \to 0$ V, as shown in Fig. 2(a). The current fluctuates at the level of nA, and this state is called the high resistance state (HRS). The current then has an abrupt increase to a compliance current of 10 nA when the voltage reaches ~ 7 V. The switching process is called the SET process. The device keeps in the low resistance state (LRS) when the voltage sweeps back from 10 V to 0 V. During the negative voltage sweeping, the device turns from LRS into HRS at the voltage about -5 V, and this process is called the RESET process. When the voltage sweeps from the negative voltage to 0 V, the device is still in the HRS. From the above description, we ascribe this behavior to the bipolar resistance memory mode due to the coexistence of a HRS and a LRS at zero voltage. Following the first *I*–*V* measurement, the second measurement is carried out immediately, and the *I*–*V* curve is similar to that of the first measurement. The threshold voltage is different, while the sequence of resistance states with the voltage sweeping has no change. There is an interesting phenomenon happened during the negative voltage sweeping process in the third measurement, which is retained in the fourth. In this *I*–*V* measurement, the bias voltage is swept in the sequence of $0 \to 0.1 \to 0 \to -0.1 \to 0$ V. Observing from Fig. 2(b), when

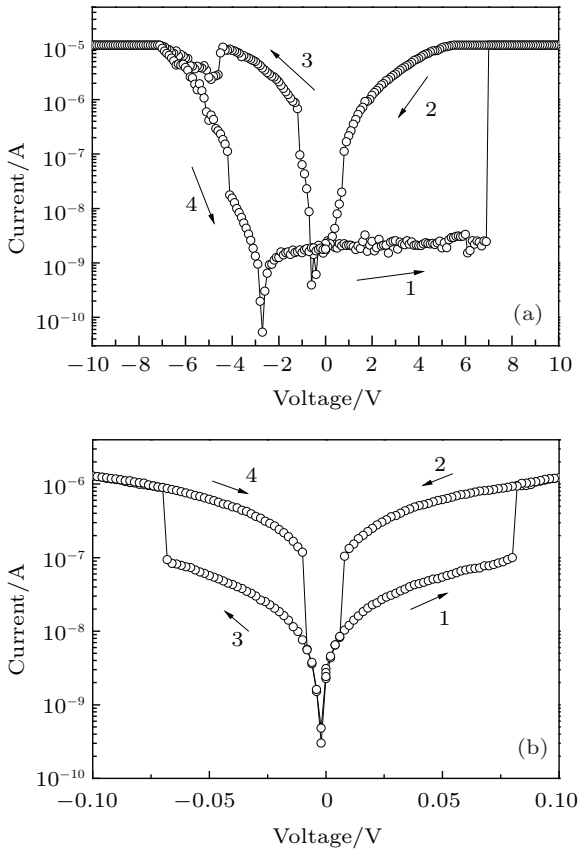


Fig. 2. Transformation process from memory switching to threshold switching of the Cu/SRO/Si device with as-deposited SRO film: (a) first three voltage sweepings, (b) after four voltage sweeping.

the voltage reaches 0.08 V, the device switches from HRS to LRS. Then, the device has a RESET process at the voltage about 0.008 V during the voltage sweeping back from 0.1 V to 0 V. And the *I*–*V* curves in the negative bias are symmetrical to those in the positive bias. The difference between the *I*–*V* curves in different voltage polarities is that the SET and RESET voltages are −0.068 V and −0.08 V, respectively. This phenomenon should be called threshold RS.[3,11] The details about the *I*–*V* curves in small scale are shown in Fig. 3, which will be carefully discussed later in this paper. The conversion from the memory to the threshold switching will also be clarified.

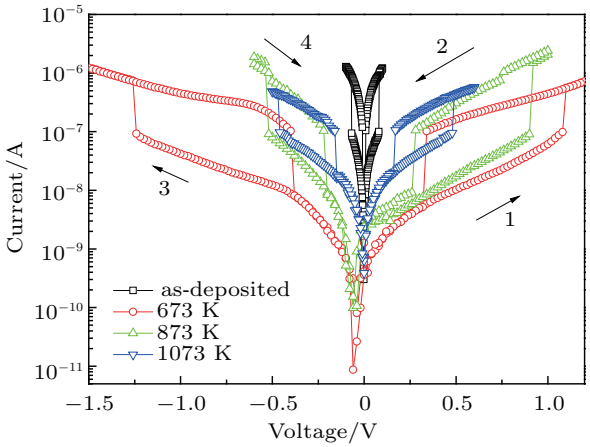


Fig. 3. (color online) Typical *I*–*V* curves of the threshold RS behavior for Cu/SRO/Si devices without annealing and annealed at 673 K, 873 K, and 1073 K, respectively. The thickness of these SRO thin films is 39 nm.

New *I*–*V* curves with higher measuring accuracy for the devices annealed at various temperatures are shown in Fig. 3. It is clear that the as-deposited device has a set process at a voltage of about 0.1 V and a reset process at a voltage of about 0.01 V. Compared to the as-deposited device, the other devices annealed at various temperatures have larger threshold voltages and smaller currents in both resistance states. With the annealing temperature decreasing from 1073 K to 673 K, $V_{\rm SET}$ and $V_{\rm RESET}$ increase from 0.48 V to 1.08 V and from 0.17 V to 0.34 V, respectively. However, the leakage current increases with the decrease of the annealing temperature, which is opposite to the fact that we know.[23] It should be pointed out that all devices can keep the reversible threshold RS behavior for more than 100 cycles and 10^5 s. The retention characteristics of the Cu/SRO/Si device with 39 nm interlayer annealed at 1073 K are shown in Fig. 4. The resistance states and switching processes of every device are quite stable.

The thickness of the interlayer is changed to investigate the thickness dependence of the *I*–*V* characteristic of the Cu/SRO/Si devices annealed at 1073 K, as shown in Fig. 5. With the increase of the interlayer thickness, the currents in HRS and LRS are kept in a lower magnitude and the buck resistance is larger. On the other hand, $V_{\rm SET}$ increases from 0.48 V to 3.72 V and $V_{\rm RESET}$ increases from 0.17 V to 0.84 V. Besides, the *I*–*V* curve turns from symmetry to asymmetry with the interlayer thickness increasing from 39 nm to 78 nm. On other hand, the lowest point of the *I*–*V* curve shifts from the zero voltage to negative bias, which means that the Schottky junction is dominate or the Schottky barrier height is high enough to show up.[24] Characteristics of Si clusters formed in SiO_x have been successively studied by Kanzawa *et al.*,[25] Furukawa *et al.*,[26] and Yi *et al.*,[27] including the infrared absorption, photoluminescence spectra, component, and structural characterization.

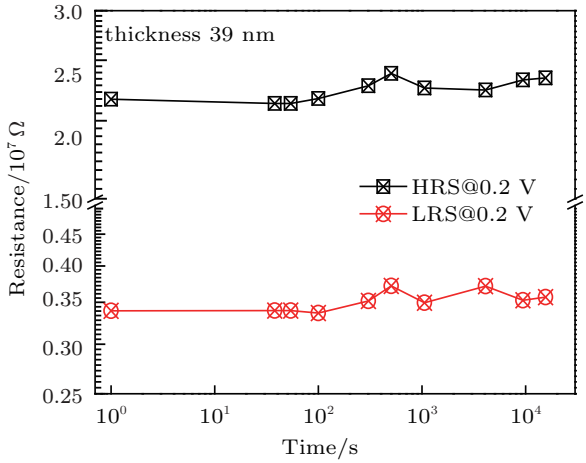


Fig. 4. (color online) Retention characteristics of the Cu/SRO/Si device with 39 nm interlayer annealed at 1073 K.

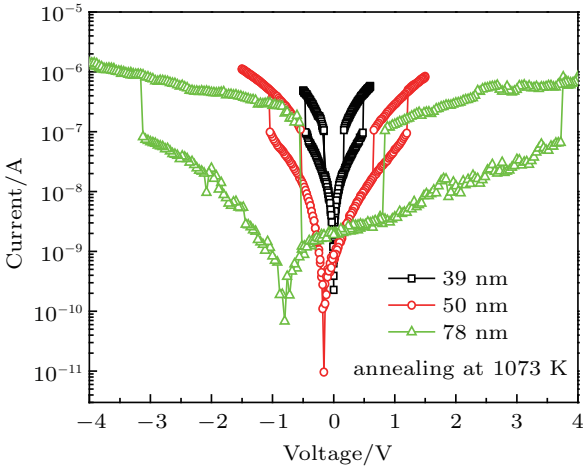


Fig. 5. (color online) The *I*–*V* characteristics of Cu/SRO/Si devices with different thicknesses of interlayers annealed at 1073 K.

With increasing annealing temperature from 673 K, the phase separation process of SiO_x can be divided into three states due to the following two reactions:

$$(SiO_x) \rightarrow SiO(g), \tag{1}$$

$$2SiO(g) \leftrightarrow Si + SiO_2, \tag{2}$$

where (SiO_x) and SiO(g) represent a nonstoichiometric SiO_x monomer at the void perimeter and a gas-phase SiO molecule,

respectively. Stage 1, for annealing at 673 K in Ar atmosphere, Ar atoms can diffuse into the film, which results in the decrease of the distortion for the bonding network in the film and the deviation from stoichiometry in the local structure. However, the Ar atoms will be removed when annealing at around 773 K, which was observed by Furukawa *et al.*[26] in the transmitted infrared (IR) absorption and x-ray photoelectron spectroscopy (XPS). Stage 2, for annealing at 873 K, reaction (1) may occur in the thin film and gaseous SiO molecules will generate. Stage 3, the SiO_x species separate into SiO_2 and Si phases on the basis of reaction (2) when the annealing temperature reaches 1073 K. However, the Si clusters are amorphous in this stage. If the annealing temperature is higher than 1073 K, the crystallization of the amorphous Si clusters will take place. The three devices annealed at the three temperatures correspond to the three states, respectively. The decreases of V_{SET} and V_{RESET} with the increase of the annealing temperature shown in Fig. 3 can be ascribed to the better regular crystal structure, which is good for the formation of the conduction channel in the grain boundaries.[28]

Comparing the Raman spectra of the samples annealed at various temperatures with those of the samples with different Si concentrations, Kanzawa *et al.*[25] noted that the spectral changes caused by annealing were very similar to those caused by the increase in the excess Si concentration. Therefore, it is believed that amorphous Si clusters have formed in the film annealed at 1073 K.

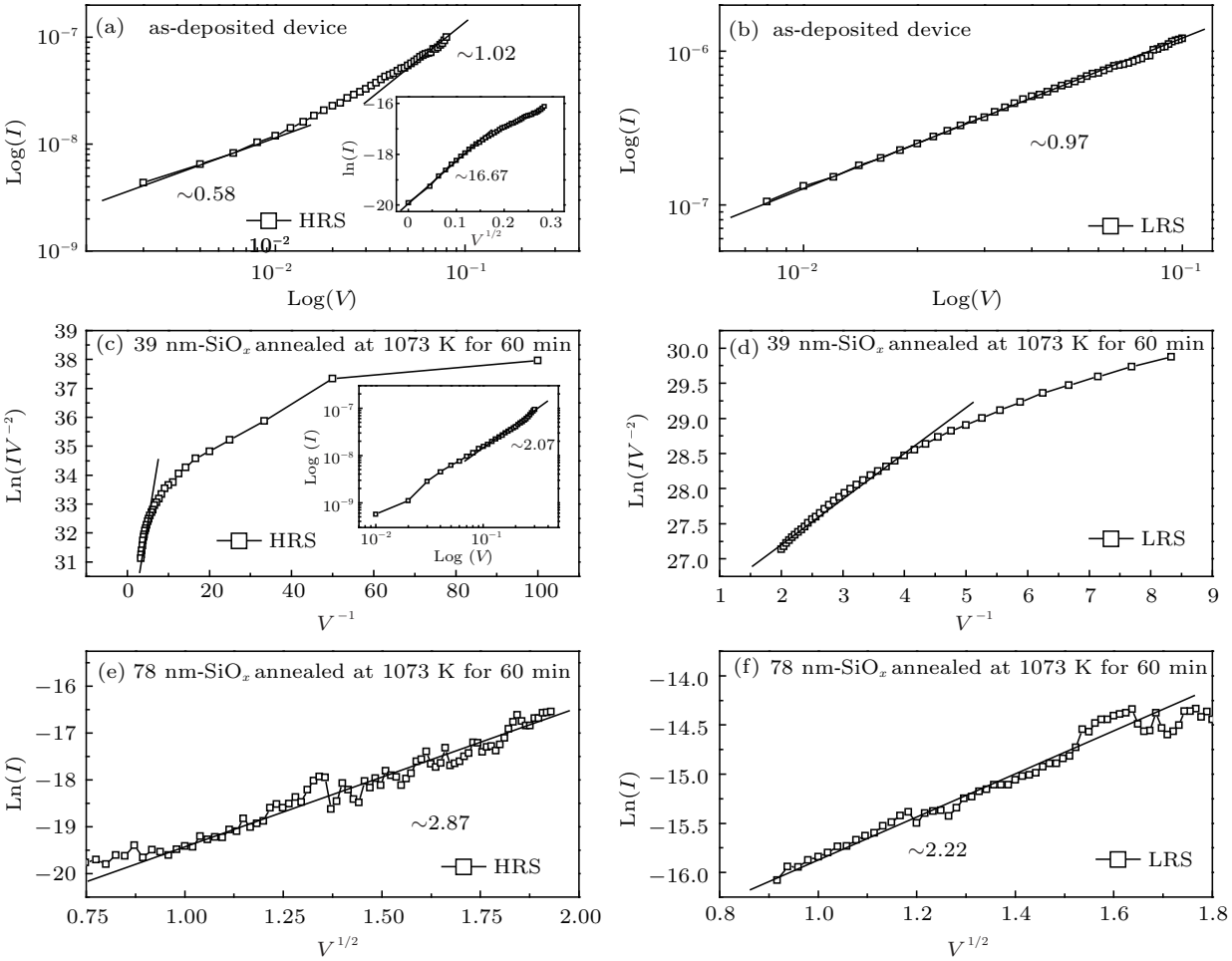


Fig. 6. Fitting analysis of the *I*–*V* curves. (a) Double-logarithmic plot of the as-deposited device in HRS. The inset of panel (a) is a Schottky emission plot. (b) Double-logarithmic plot of the as-deposited device in LRS. (c) and (d) The positive bias *I*–*V* characteristic of the 39 nm-SiO_x film annealed at 1073 K in coordinates corresponding to Fowler–Nordheim tunneling in HRS and LRS, respectively. (e) and (f) Schottky emission presentations of the *I*–*V* curves of the 78 nm-SiO_x film annealed at 1073 K in HRS and LRS, respectively.

In order to better understand the origins of the threshold RS effect, fittings to the *I*–*V* characteristics are carried out to study the conduction mechanism. For the as-deposited device, a double-logarithmic plot for HRS in the positive bias is shown in Fig. 6(a). In the low voltage region, the Schottky emission mechanism is dominant. In the high voltage region, as indicated by the slope ~1.02, the ohmic conduction is dominant. In addition, the ohmic conduction is still dominant in Fig. 6(b) as shown by the near 1.00 slope in the log–log plot. This means that in the two stages, the conduction theory of the variable rang hopping between uncontinuously trapping centers can well explain the phenomenon. For the device an-

nealed at 1073 K, owing to the decrease of the defect density, such as silicon dangling bonds and oxygen vacancies, the process of injected electrons trapping by a-Si clusters will be obvious in LRS, which can be confirmed by the liner fitting about Fowler–Nordheim tunneling for the voltage < 0.5 V. However, as seen from Fig. 6(c) and the inset of Fig. 6(c), F–N tunneling and traps-filled space controlled limited conduction (SCLC) are dominated in the low and the high bias voltage regions, respectively. Moreover, both HRS and LRS are dominated by the Schottky emission for the 78 nm-SiO_x film annealed at 1073 K, as shown in Figs. 6(e) and 6(f). In conclusion, a possible switching mechanism for the 39 nm-SiO_x films can come from the same origin, i.e., formation and rupture of conduction paths. Note that different types of paths are formed in the films, for the as-deposited sample, electron trapping and detrapping by defects in high concentration is dominated; while for the 1073 K-annealed sample, tunneling between a-Si clusters plays an important role in the threshold RS behavior. On the other hand, for the 78 nm-SiO_x film, adjusting of the Schottky barrier height between insulator and semiconductor is more reasonable to describe the switching behavior. In contrast from the mechanism reported by Jiang *et al.*,[29] formation of a-Si clusters by annealing is random and the distribution of a-Si clusters is uniform. When the electrons are injected from a cathode, a number of a-Si clusters trap electrons, but the possibility of electrons transported to the neighbor cluster is limited. Therefore, the way that electrons are collected by the anode is similar to a funnel.

We also measure the temperature dependence of $R_{\rm LRS}$ at 0.4 V for the Cu/SRO/Si device with 39-nm thickness SRO film annealed at 1073 K, as shown in Fig. 7. It is clear that the resistance increases as the temperature decreases from 295 K to 230 K. This implies that the electronic transport in the LRS of the device is semiconduction rather than the metallic conduction. Therefore, it is reasonable for us to exclude the effect of the Cu electrode.

The switching from the memory mode to the threshold mode of SRO can be explained well by soft breakdown models for SiO_2 thin films.[30,31] As sweeping with a large electric field for the initial time, local overheating occurs, which means that the balance between Joule heating and thermal dissipation is broken. This can induce local crystalline structural changes because the atoms will move to the local lattice point with the lowest energy. In addition, the Si–O bonds will be broken to form Si–Si bonds, which then aggregate into clusters. Abundant clusters will present in the SiO_x film by increasing the sweeping times and different conduction behaviors will happen between neighboring clusters because of their different morphologies. Therefore, we need a large bias voltage of about 8 V to active the reaction as shown in Fig. 2. In addition, the local overheating will facilitate the atoms to recombine again and the process is similar to current annealing, which is similar to the results reported by other groups; i.e., using compliance current,[10,11] bottom electrode with different thicknesses,[8] or controlling by temperature.[3]

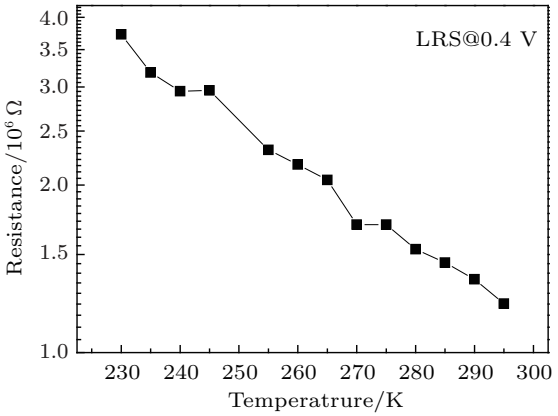


Fig. 7. Temperature dependence of $R_{\rm LRS}$ at 0.4 V for the Cu/SRO/Si device with 39-nm thickness SRO film annealed at 1073 K. The measurement was carried out about one year after completing the device.

4. Conclusion

We find that the threshold switching can be obtained from the memory switching by continuous high voltage sweeping in all fabricated devices. In addition, the *I–V* characteristics show a dependence on the annealing temperature and the interlayer thickness of the Si-rich SiO_x films. Fittings to the *I–V* characteristics and features of Si clusters embedded in SiO_x prove that different conduction channels are formed in the 39 nm-SiO_x films. For the unannealed and 1073 K-annealed devices, electron trapping and detrapping by defects and tunneling between amorphous Si clusters dominate, respectively. On the other hand, the 78 nm-SiO_x film annealed at 1073 K is caused by adjusting the Schottky barrier height between insulator and semiconductor. Above all, the conversion between the memory switching and the threshold switching is determined by the formation of clusters due to the local overheating under a large electric field. Our investigation provides a guide to control the two switching modes and to improve the performance of resistance random access memory.

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