A two-dimensional analytical modeling for channel potential and threshold voltage of short channel triple material symmetrical gate Stack (TMGS) DG-MOSFET

Shweta Tripathi†

Department of Electronics & Communication Engineering, Motilal Nehru National Institute of Technology, Allahabad-211004, India

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In the present work, a two-dimensional (2D) analytical framework of triple material symmetrical gate stack (TMGS) DG-MOSFET is presented in order to subdue the short channel effects. A lightly doped channel along with triple material gate having different work functions and symmetrical gate stack structure, showcases substantial betterment in quashing short channel effects to a good extent. The device functioning amends in terms of improved exemption to threshold voltage roll-off, thereby suppressing the short channel effects. The encroachments of respective device arguments on the threshold voltage of the proposed structure are examined in detail. The significant outcomes are compared with the numerical simulation data obtained by using 2D ATLAS^{TM} device simulator to affirm and formalize the proposed device structure.

Keywords: triple material symmetrical gate stack (TMGS) DG MOSFET, gate stack, short channel effect, drain induced barrier lowering, threshold voltage

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1. Introduction

During the last five decades since the invention of the MOSFETs, we have seen rapid and stiff advancement in the evolution of integrated circuit engineering.[1–3] The principal driving force behind this tremendous development has been the downscaling of the dimensions of the MOSFET.[3,4] The greater the downscale of MOSFET, the higher its packing density becomes, the faster its operation and the lower its power dissipation is.[5] The perennial downscaling slipstream of MOSFETs has steered eminent execution and low power functioning as prescribed by ITRS, however some newfangled effects in the device performance have also arisen.[4–6] In particular, a gathering of undesirable sources of difficulties springs up, which are jointly called short channel effects (SCEs) that hinder further advancement in transistor downscaling.[6] In order to sustain the rate of advancement in device performance with uninterrupted downscaling, alterations to device design and fabrication are the essential requirements. In connection to this, a number of new extended device structures already have been reported in the literature to handle the severe challenges associated with SCEs as well as device efficiency.[7–15] One of the predominant anticipated solutions in the nanoscale regime to inhibit these SCEs is DG-MOSFET.[16] However to cope with the device downscaling and quashing the SCEs, there arises the need to allow some relatively thicker gate oxide along with high-k effectuation to exert the electrostatic integrity of the DG MOSFET device.[7,15] Due to this progression, DG-MOSFET is anticipated to be further investigated to subdue the SCEs.

A multimaterial-based gate structure is anticipated to provide further improvement in the performance of DG MOSFET since it may create a step potential profile to screen the effect of the drain on the channel.[12,13] Another possible solution to suppress SCEs is by using gate stack. If aforementioned solutions are combined in order to improve the performance of DG MOSFET then it may prove to be an effective option over the existing technology. There exist several reports that establish the superiority of the performance of TM DG MOSFET and gate stack structures.[12–15] Razavi and Orouji[12] proposed TM-DG MOSFET structure and through numerical simulation results they showed that SCEs such as drain-induced barrier lowering (DIBL) and hot carrier effect are reduced significantly in comparison with conventional DG MOSFET. They also demonstrated that TM-DG MOSFET leads simultaneously to the enhancement of transconductance and the reduction of drain conductance which itself leads to higher DC gain than the classical DG MOSFET. Pradhan *et al.*[13] reported a simulation-based study for the performance differences among six dissimilar gate stacked device structures by utilizing gate and channel engineering. They also considered the gate stack TM DG MOSFET for the simulation purpose and established that TM DG MOSFET with gate stack structures improves DIBL significantly. Alamgir *et al.*[14] investigated the performance of DG-MOSFET with high-k stack on both the top and bottom gates using numerical simulation results. They observed that higher drain current in the low and high drain voltage regions, as well as lower threshold voltage and improved subthreshold swing can be yielded by considering their proposed structure. Jin *et al.*[15] presented an analytical-model-based study for surface potential, threshold

†Corresponding author. E-mail: shtri@mnnit.ac.in

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voltage, subthreshold current and subthreshold swing of symmetrical gate stack dual gate strained silicon MOSFETs. They showed that the high-k region on the oxide layer exhibits reduced SCE.

Therefore, based on the literature it can be concluded that pertaining to the scaling down of the device thickness, triple material gate stack structure is anticipated to be a more effective option over existing DG MOSFET device. To the best of my knowledge, so far in the literature analytical modeling and simulation-based study of TM DG MOSFET with gate stack have not been done. Hence in the present paper, combining the advantages of high-k gate stack and triple material structure, a new compact analytical model for triple material symmetrical gate stack (TMGS)-DG MOSFET is presented. In this proposed device structure, the front and back gate electrode each comprising three materials with different work functions and symmetrical high-k gate stack are considered for developing the compact analytical model and numerical simulation. Moreover, the channel of the simulated model is adopted to be lightly doped in order to increase the mobility of the charge carriers and stave off the problem of threshold voltage variation due to random fluctuation of dopant atoms. The result analysis is based on the solution of two dimensional (2D) Poisson's equation with the appropriate limit specifications employing 2D ATLAS^{TM} device simulation tool.[17]

2. Device structure

The schematic device structure of TMGS-DG MOSFET used for analysis and simulation is shown in Fig. 1, where L ($L = L_1 + L_2 + L_3$), t_{si}, t_{ox}, and t_k are gate length, channel thickness, thickness of gate oxide and thickness of material with large dielectric constant, respectively. The x and y axes of the schematic structure are considered to be along the channel length and channel thickness, respectively.

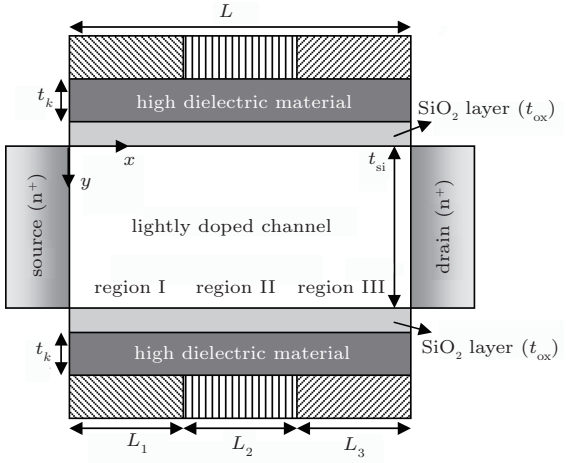


Fig. 1. Schematic diagram of TMGS DG MOSFET, where L ($L = L_1 + L_2 + L_3$), t_{si}, t_{ox}, and t_k are gate length, thickness of silicon channel, thickness of gate oxide, and thickness of high dielectric constant material, respectively.

The gate electrode of the DG MOSFET is considered to be made up of three materials having different work functions ϕ_{m1}, ϕ_{m2}, and ϕ_{m3} (such that $\phi_{m1} > \phi_{m2} > \phi_{m3}$) and deposited over the respective lengths L_1, L_2, and L_3 on the gate oxide layer. The gate material placed at the source end with the highest work-function i.e., ϕ_{m1} forms a control gate, the middle material with intermediate work-function value ϕ_{m2} forms a first screen gate, and the remaining material with the lowest work function ϕ_{m3} placed at the drain side of the gate forms a second screen gate. In the present work tungsten disilicide (WSi_2, $\phi_{m1} = 4.8$ eV), $Hf_{0.27}Ta_{0.58}N_{0.15}$ ($\phi_{m2} = 4.6$ eV), and $Hf_{0.40}Ta_{0.46}N_{0.14}$ ($\phi_{m3} = 4.4$ eV) are used as the materials for control gate, first and second screen gates, respectively. The gate terminal of the TMGS-DG MOSFET device is made by tying together control and screen gates in order to feed the device with the same gate voltage V_{gs}. In the proposed structure, high-k gate stack is used in order to combat the SCEs therefore in place of t_{ox} effective gate oxide thickness (t_{eff}) is used. t_{eff} can be given as[15]

$$t_{eff} = \frac{\varepsilon_k t_{ox} + \varepsilon_{ox} t_k}{\varepsilon_k}, \tag{1}$$

where t_k is the high dielectric material thickness and ε_k is dielectric constant of the high-k material.

3. Model derivation

3.1. 2D potential modeling

The 2D Poisson's equation for potential distribution in the lightly doped channel region can be given as[15]

$$\frac{\partial^2 \phi_n(x,y)}{\partial x^2} + \frac{\partial^2 \phi_n(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{si}}, \quad n = 1,2,3, \tag{2}$$

where $n = 1$, 2, and 3 correspond to the regions under metal M_1, M_2, and M_3, respectively. $\phi_n(x,y)$ is the electrostatic potential in the channel region, q is the electronic charge on electron, N_a is the acceptor concentration of channel, and ε_{si} is the permittivity of silicon.

The Poisson's equation can be solved using the following boundary conditions.

(i) Electric fluxes (displacement) at the gate-oxide/substrate-Si layer interface of top and bottom gate are continuous therefore boundary conditions for the front and back surface can be expressed, respectively, as[17]

$$\left.\frac{\partial \phi_n(x,y)}{\partial y}\right|_{y=0} = \frac{\varepsilon_{ox}\left[\phi_{Sn}(x) - V_{gs} + V_{fbn}\right]}{\varepsilon_{si} t_{eff}}, \tag{3}$$

$$\left.\frac{\partial \phi_n(x,y)}{\partial y}\right|_{y=t_{si}} = -\frac{\varepsilon_{ox}\left[\phi_{Sn}(x) - V_{gs} + V_{fbn}\right]}{\varepsilon_{si} t_{eff}}, \tag{4}$$

where $\phi_{si}(x)$ are the surface potentials related to channel regions I, II, and III, respectively, V_{gs} is the gate-to-source voltage, V_{fbn} is the flat band voltages corresponding to regions I, II, and III, and can be given as

$$V_{fbn} = \phi_{mn} - \left[\chi_{si} + \frac{E_g}{2q} + V_T \ln\left(\frac{N_a}{n_i}\right)\right]. \tag{5}$$

Here, ϕ_{mn} are the work functions of the gate material in regions I, II, and III of the top and bottom gate respectively, χ_{si} is the electron affinity of the silicon material, E_g is the silicon energy band gap, V_T is the thermal voltage, and n_i is the intrinsic carrier concentration.

(ii) The potential distribution must be a continuous function for the entire channel region, therefore boundary conditions for interfacing regions (Regions I–II and Regions II–III) can be as given as follows:[17]

$$\phi_1(L_1,0) = \phi_2(L_1,0), \tag{6}$$
$$\phi_1(L_1,t_{si}) = \phi_2(L_1,t_{si}), \tag{7}$$
$$\phi_2(L_1+L_2,0) = \phi_3(L_1+L_2,0), \tag{8}$$
$$\phi_2(L_1+L_2,t_{si}) = \phi_3(L_1+L_2,t_{si}). \tag{9}$$

(iii) The electric flux at channel region interfaces (Regions I–II and Regions II–III) will also be continuous. Thus, boundary conditions for electric flux at these interfaces can also be given as

$$\left.\frac{\partial\phi_1(x,y)}{\partial x}\right|_{x=L_1} = \left.\frac{\partial\phi_2(x,y)}{\partial x}\right|_{x=L_1}, \tag{10}$$
$$\left.\frac{\partial\phi_2(x,y)}{\partial x}\right|_{x=L_1+L_2} = \left.\frac{\partial\phi_3(x,y)}{\partial x}\right|_{x=L_1+L_2}. \tag{11}$$

(iv) The potentials at the source-channel and channel-drain interface can be written as[17]

$$\phi_1(0,0) = \phi_{S1}(0) = V_{bi}, \tag{12}$$
$$\phi_3(L,0) = \phi_3(L_1+L_2+L_3,0) = \phi_{S3}(L_1+L_2+L_3) = V_{bi}+V_{ds}, \tag{13}$$

where V_{ds} is the drain-to-source voltage and V_{bi} is the built-in potential of the source–channel and channel–drain junctions given as

$$V_{bi} = \left[V_T \ln\left(\frac{N_a N_{ds}}{n_i^2}\right)\right], \tag{14}$$

where N_{ds} represent the drain and source doping concentrations respectively.

The potential distribution in the channel is assumed to be parabolic third order polynomial and can be expressed as[18]

$$\phi_i(x,y) = \phi_{Sn}(x) + c_{n1}(x)\,y + c_{n2}(x)\,y^2, \tag{15}$$

where c_{n1} and c_{n2} each are an arbitrary function of x. The Poisson's equation is solved separately under the three metal gates by using the boundary conditions from Eqs. (3)–(13), to obtain the coefficients $\phi_{Sn}(x)$, $c_{n1}(x)$, and $c_{n2}(x)$ of Eq. (15) and the values obtained can be written as

$$c_{n1}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{eff}}\left[\phi_{si}(x) - V_{gs} + V_{fbn}\right], \tag{16}$$
$$c_{n2}(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{eff}t_{si}}\left[\phi_{si}(x) - V_{gs} + V_{fbn}\right]. \tag{17}$$

Now, substituting $y = t_{si}/2$ into Eq. (15) and utilizing Eqs. (16) and (17), we can obtain $\phi_{Sn}(x)$ as

$$\phi_{Sn}(x) = \frac{4\varepsilon_{si}t_{eff}}{4\varepsilon_{si}t_{eff}+\varepsilon_{ox}t_{si}} \times \left[\phi_{Cn}(x) + \frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{eff}}\left(V_{gs}-V_{fbn}\right)\right], \tag{18}$$

where $\phi_{Cn}(x)$ is the mid channel potential of the device given by

$$\phi_{Cn}(x) = \phi_n(x,y)|_{y=t_{si}/2}. \tag{19}$$

The characteristic length associated with mid channel potential of the channel is significant in determining SCEs of the DG MOSFET.[19] Therefore, characteristic length can be determined by solving Poisson's equation in the middle of the silicon channel.[19] Now, following this argument Eq. (2) can be solved at the center of the silicon channel as,[20]

$$\frac{\partial^2\phi_{Ci}(x)}{\partial x^2} + \frac{\phi_{Ci}(x)}{\lambda^2} = \frac{qN_a}{\varepsilon_{si}} - \frac{V_{gs}-V_{fbi}}{\lambda^2}, \tag{20}$$

where λ is the characteristic length associated with the center channel potential given as[17]

$$\lambda = \sqrt{\frac{t_{si}\left(4\varepsilon_{si}t_{eff}+\varepsilon_{ox}t_{si}\right)}{8\varepsilon_{ox}}}. \tag{21}$$

The generalized solution of Eq. (20) can be written as[17]

$$\phi_{Cn}(x) = A_n \exp\left(\frac{x}{\lambda}\right) + B_n \exp\left(\frac{-x}{\lambda}\right) - \frac{\beta_n}{\alpha} \tag{22}$$

where $\lambda = \sqrt{\alpha}$, $\eta = 1/\sqrt{\alpha}$ and

$$\beta_i = \frac{1}{\alpha\varepsilon_{si}}\left[q\alpha N_a - \varepsilon_{si}\left(V_{gs}-V_{fbi}\right)\right]. \tag{23}$$

The coefficients A_n's and B_n's of the generalized solution Eq. (22) corresponding to the channel regions I, II, and III can be obtained by solving Eq. (20) in conjunction with the boundary conditions of Eqs. (6)–(13) and can be given by

$$A_1 = \frac{1}{2\sinh\left[\eta\left(L_1+L_2+L_3\right)\right]}\left[V_{bi}+V_{ds}+\frac{\beta_3}{\alpha} - \left(V_{bi}+\frac{\beta_1}{\alpha}\right)\exp\left[-\eta\left(L_1+L_2+L_3\right)\right] + \frac{(\beta_1-\beta_2)}{\alpha}\cosh\left[\eta\left(L_2+L_3\right)\right] + \frac{(\beta_2-\beta_3)}{\alpha}\cosh\left(\eta L_3\right)\right], \tag{24}$$

$$B_1 = \frac{1}{\alpha}\left(\alpha V_{bi} + \beta_1 - \alpha A_1\right), \tag{25}$$

$$A_2 = \frac{2A_1\alpha\exp(\eta L_1) - (\beta_1 - \beta_2)}{2\alpha}, \tag{26}$$

$$B_2 = \frac{2\alpha\exp(-\eta L_1)\left(V_{\rm bi} + \frac{\beta_1}{\alpha} - A_1\right) - (\beta_1 - \beta_2)}{2\alpha}, \tag{27}$$

$$A_3 = \frac{2A_1\alpha\exp[\eta(L_1 + L_2)] - (\beta_1 - \beta_2)\exp[\eta L_2] - (\beta_2 - \beta_3)}{2\alpha}, \tag{28}$$

$$B_3 = \frac{2\left(V_{\rm bi} + \frac{\beta_1}{\alpha} - A_1\right)\alpha\exp[-\eta(L_1 + L_2)] - (\beta_1 - \beta_2)\exp(-\eta L_2) - (\beta_2 - \beta_3)}{2\alpha}. \tag{29}$$

Now using Eqs. (15), (18), (22), and Eqs. (24)–(29), the 2D channel potentials for the three regions of the channel can be obtained as

$$\phi_n(x,y) = \left[A_n\exp(\eta x) + B_n\exp(-\eta x) - \frac{\beta_n}{\alpha} + \frac{\varepsilon_{\rm ox}t_{\rm si}}{4\varepsilon_{\rm si}t_{\rm eff}}\left(V_{\rm gs} - V_{{\rm fb}n}\right)\right]\left[1 + \frac{\varepsilon_{\rm ox}t_{\rm si}}{4\varepsilon_{\rm si}t_{\rm eff}}\right]^{-1}$$
$$\times\left[1 + \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}t_{\rm eff}}y - \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}t_{\rm eff}t_{\rm si}}y^2\right] - \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}t_{\rm eff}}\left(V_{\rm gs} - V_{{\rm fb}n}\right)y + \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}t_{\rm eff}t_{\rm si}}\left(V_{\rm gs} - V_{{\rm fb}n}\right)y^2, \tag{30}$$

where $n = 1, 2, 3$.

3.2. Threshold voltage modeling

Under threshold condition, the channel under the control gate will not conduct until channels under both the screen gates are turned on. The conduction from source to drain will take place only when all the three gates are turned on. This suggests that threshold voltage of the device under consideration will systematically be governed by control gate region of length L_1 with highest work function ϕ_{m1}. The effect of drain-to-source voltage on the subthreshold behavior of the device can be monitored by position and value of minimum channel potential. The position of minimum channel potential $x_{\rm min}$ can be evaluated by solving equation

$$\left.\frac{{\rm d}\phi_{C1}(x)}{{\rm d}x}\right|_{x=x_{\rm min}} = 0$$

and given as,

$$x_{\rm min} = \frac{\lambda}{2}\ln\left(\frac{B_1}{A_1}\right). \tag{31}$$

Now, minimum value of channel potential $\phi_{C1}(x) = \phi_{C1}(x_{\rm min}) = \phi_{C1\,\rm min}$, i.e., minimum channel potential can be obtained by using Eq. (22), and equation (31) can be written as

$$\phi_{C1\,\rm min} = \frac{1}{\varepsilon_{\rm si}}\left[\left(2\sqrt{A_1B_1} + V_{\rm gs} - V_{\rm fb1}\right)\varepsilon_{\rm si} - \lambda^2 qN_{\rm a}\right]. \tag{32}$$

Now, the virtual cathode potential $\phi_{\rm vc}(y)$ can be given as[21]

$$\phi_{\rm vc}(y) = \left[1 + \frac{\varepsilon_{\rm ox}t_{\rm si}}{4\varepsilon_{\rm si}t_{\rm eff}}\right]^{-1}\left[\phi_{C1\,\rm min} + \frac{\varepsilon_{\rm ox}t_{\rm si}}{4\varepsilon_{\rm si}t_{\rm eff}}\left(V_{\rm gs} - V_{\rm fb1}\right)\right]\left[1 + \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}t_{\rm eff}}y - \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}t_{\rm eff}t_{\rm si}}y^2\right] - \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}t_{\rm eff}}\left(V_{\rm gs} - V_{\rm fb1}\right)y + \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}t_{\rm eff}t_{\rm si}}\left(V_{\rm gs} - V_{\rm fb1}\right)y^2. \tag{33}$$

The inversion charge density ($Q_{\rm inv}$) depends exponentially on the surface potential. Now the inversion carrier charge sheet density at $\phi_{\rm vc}(y)$ can be given as[22]

$$Q_{\rm inv} = n_{\rm i}\int_0^{t_{\rm si}}\exp\left(\frac{q}{kT}\phi_{\rm vc}(y)\right){\rm d}y. \tag{34}$$

In order to obtain the analytical expression of $Q_{\rm inv}$ we may use the property of undoped DG MOSFET that the effective conduction path is located at $y = t_{\rm si}/4$ from the silicon surface. Thus, $Q_{\rm inv}$ can be approximated as

$$Q_{\rm inv} = n_{\rm i}\int_0^{t_{\rm si}}\exp\left(\frac{q}{kT}\phi_{\rm vc1}(y)\Big|_{y=\frac{t_{\rm si}}{4}}\right){\rm d}y. \tag{35}$$

Now using the value of $\phi_{\rm vc}(y)$ from Eq. (33), in Eq. (35), $Q_{\rm inv}$ can be given as

$$Q_{\rm inv} = n_{\rm i}t_{\rm si}\exp\left(\frac{q}{kT}\left[V_{\rm gs} - V_{\rm fb1} + \left(\frac{4\varepsilon_{\rm si}t_{\rm eff}}{4\varepsilon_{\rm si}t_{\rm eff} + \varepsilon_{\rm ox}t_{\rm si}}\right)\left(2\sqrt{A_1B_1} - \frac{\lambda^2 qN_{\rm a}}{\varepsilon_{\rm si}}\right)\left(1 + \frac{3\varepsilon_{\rm ox}t_{\rm si}}{16\varepsilon_{\rm si}t_{\rm eff}}\right)\right]\right). \tag{36}$$

Now assuming $Q_{\rm in} = Q_{\rm TH}$ under threshold condition Eq. (36)[22,23] becomes

$$V_{\rm TH} - V_{\rm fb1} + \left(\frac{4\varepsilon_{\rm si}t_{\rm eff}}{4\varepsilon_{\rm si}t_{\rm eff} + \varepsilon_{\rm ox}t_{\rm si}}\right)\left(2\sqrt{A_1'B_1'} - \frac{\lambda^2 qN_{\rm a}}{\varepsilon_{\rm si}}\right)\left(1 + \frac{3\varepsilon_{\rm ox}t_{\rm si}}{16\varepsilon_{\rm si}t_{\rm eff}}\right) = \frac{KT}{q}\ln\left(\frac{Q_{\rm TH}}{n_{\rm i}t_{\rm si}}\right), \tag{37}$$

where

$$A_1' = A_1\left(V_{gs} = V_{TH}\right) \text{ and } B_1' = B_1\left(V_{gs} = V_{TH}\right).$$

To obtain the threshold voltage of long channel device, the limiting condition of $L \to \infty$ in Eq. (37) yields

$$V_{THL} = V_{fb1} + \frac{16\varepsilon_{si}t_{eff} + 3\varepsilon_{ox}t_{si}}{4\left(4\varepsilon_{si}t_{eff} + \varepsilon_{ox}t_{si}\right)}\frac{\lambda^2 qN_a}{\varepsilon_{si}} + \frac{KT}{q}\ln\left(\frac{Q_{TH}}{n_i t_{si}}\right). \tag{38}$$

Now using Eq. (37), equation (38) can be solved to obtain short channel threshold voltage of the device under consideration as follows:

$$V_{TH} = V_{THL} - \frac{16\varepsilon_{si}t_{eff} + 3\varepsilon_{ox}t_{si}}{4\left(4\varepsilon_{si}t_{eff} + \varepsilon_{ox}t_{si}\right)}\frac{\lambda^2 qN_a}{\varepsilon_{si}} + \left(\frac{4\varepsilon_{si}t_{eff}}{4\varepsilon_{si}t_{eff} + \varepsilon_{ox}t_{si}}\right)\left(2\sqrt{A_1'B_1'} - \frac{\lambda^2 qN_a}{\varepsilon_{si}}\right) \times \left(1 + \frac{3\varepsilon_{ox}t_{si}}{16\varepsilon_{si}t_{eff}}\right). \tag{39}$$

4. Results and discussion

In this section, we present some theoretical results obtained by the proposed model that is validated by comparing the theoretical results with the numerical simulation data obtained by using the ATLAS^{TM} device simulator. The drift-diffusion model has been used for carrier transport, and classical Fermi–Dirac statistics model is used for the numerical simulation.[24] To integrate the effect of high electric field in the device channel, the field dependent mobility model has been implemented in the ATLAS^{TM} simulation.[25,26] Further, the ratio of lengths of regions I, II, and III is taken to be $L_1 : L_2 : L_3 : 1 : 1 : 1$ for all the computations. The p-type substrate concentration is taken to be uniformly doped with a doping concentration of $N_a = 1 \times 10^{16}$ cm^{-3} in all the three regions under different gate metal contacts. The source and drain regions are both assumed to be heavily doped with doping concentration of $N_{S/D} = 1 \times 10^{20}$ cm^{-3}. The dielectric constant value of high-k material is taken to be 20. The typical values of t_{si}, t_{ox}, and t_k are taken to be 20 nm, 2 nm, and 4 nm respectively.

Figure 2 shows the variations of surface potential of TMGS-DG MOSFET along the gate length for different values of drain-to-source voltage (V_{ds}). It can be clearly seen from the figure that the area under the control gate is effectively screened from the variations in V_{ds}, thereby giving rise to negligible DIBL effect in the device due to the presence of the two screening gates. Further, it may also be observed from the figure that the position of minimum channel potential lies under the control gate, which justifies the assumption that we have made for modeling the threshold voltage. The variations of threshold voltage with gate length for different values of V_{ds} are plotted in Fig. 3. It can be seen from the figure that for longer gate length devices, threshold voltage varies little with the drain bias compared with the corresponding shift of threshold voltage for shorter gate length devices.

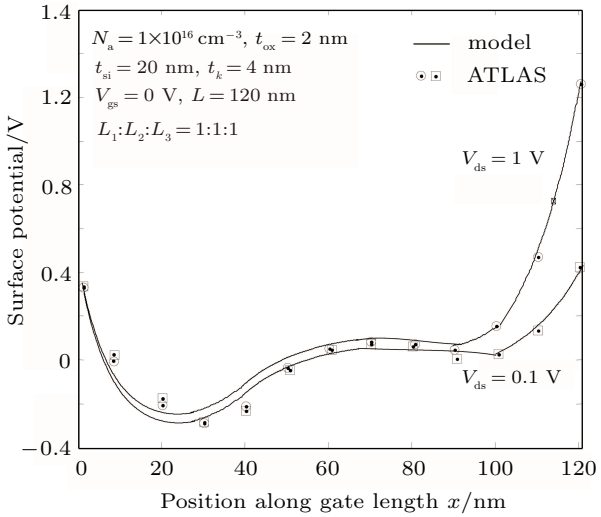


Fig. 2. Variations of channel potential with position along the channel length for different values of drain-to-source voltage (V_{ds}).

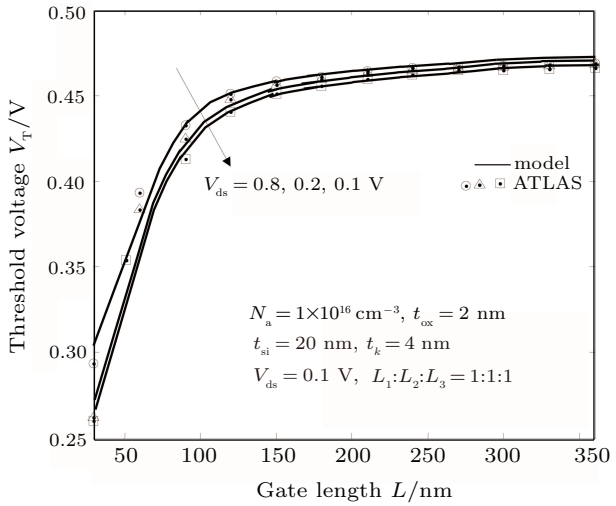


Fig. 3. Variations of threshold voltage with gate length (L) for different values of drain-to-source voltage (V_{ds}).

Figure 4 demonstrates the variations of threshold voltage with gate length for different values of silicon thickness (t_{si}). It is noteworthy here that for the lower values of t_{si}, the roll-off in the threshold voltage is relatively low in comparison with that for the higher channel thickness. It may be due to the improvement in the gate electrostatics on the channel with the decrease in t_{si}.

Figure 5 shows the variations of the threshold voltage with channel lengths for different values of gate-oxide thickness (t_{ox}). It can be observed from the figure that the device with lower t_{ox} shows better suppression of SCEs.

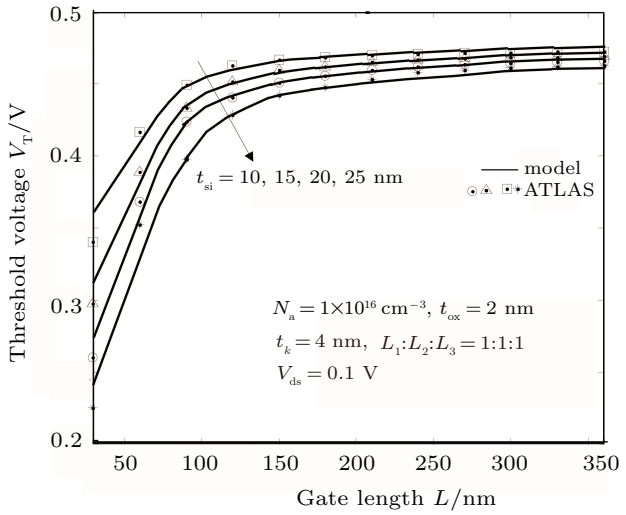


Fig. 4. Variations of threshold voltage with gate length (L) for different values of silicon film thickness t_{si}.

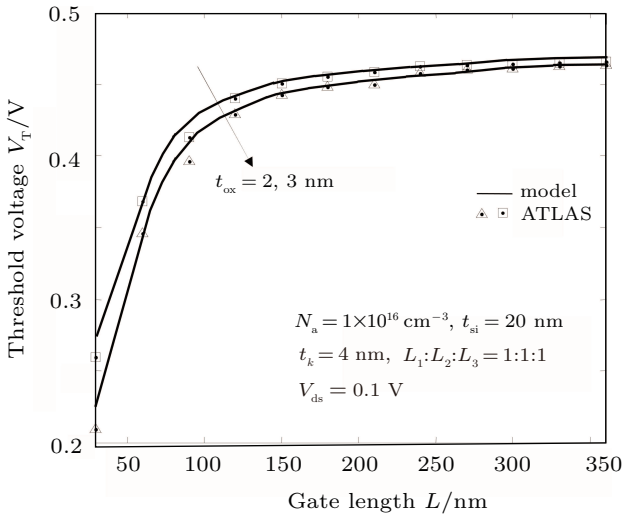


Fig. 5. Variations of threshold voltage with gate length (L) for different values of gate-oxide thickness (t_{ox}).

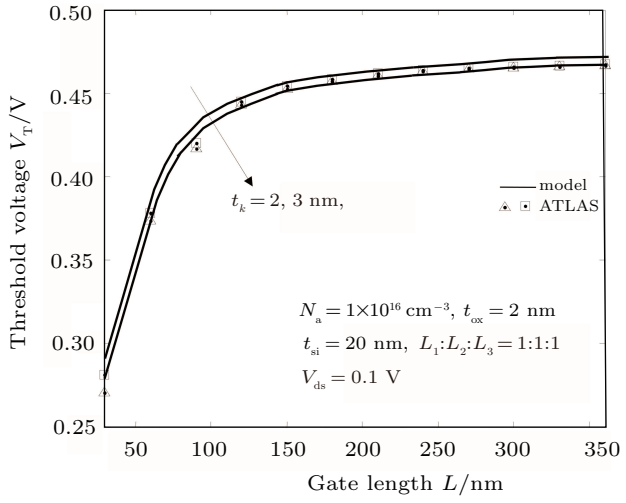


Fig. 6. Variations of threshold voltage with the gate length (L) for different values of stack layer thickness (t_k).

Figure 6 shows the variations of threshold voltage with channel length (L) for different values of stack layer thickness (t_k). The threshold voltage roll-off is higher for large value of t_k. It may further be noted that if we compare Fig. 5 with Fig. 6, then it may be observed that the effect of t_k oversees the effect of t_{ox} on the threshold voltage variation. Even the threshold voltage roll-off is improved in the case of larger value of t_k therefore in the case of TMGS-DG MOSFET gate stack oxide acts as a controlling gate oxide.

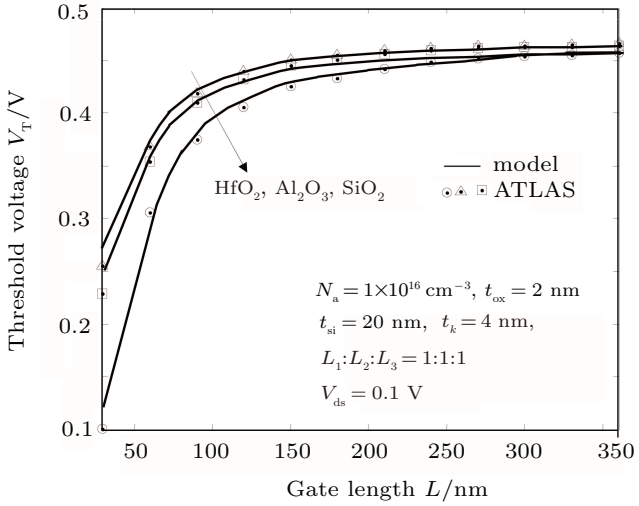


Fig. 7. Variations of threshold voltage with gate length (L) for different stack materials HfO_2, Al_2O_3, and SiO_2.

Figure 7 shows the effects of change of high-k stack material on the threshold voltage of the device with different gate lengths. Three different dielectric materials are considered i.e., HfO_2, Al_2O_3, and SiO_2 with largest value of dielectric constant for HfO_2 and least value for SiO_2. It can be observed from the figure that for the material with high dielectric constant threshold voltage, the roll-off is considerably reduced. It may be due to the fact that increasing dielectric constant of the stack material can lead to a decrease in the effective gate oxide thickness t_{eff} (Eq. (1)), which may result in an efficient suppression of SCEs. This implies that the improved gate controllability can be achieved by using material with high dielectric constant to establish the suitability of TMGS-DG MOSFET over conventional DG MOSFET.

5. Conclusions

In the present paper, channel potential and threshold voltage of DG-MOSFET is modeled analytically. A detailed study to see the effects of gate stack on the threshold voltage of TMGS DG-MOSFET and other important parameters is performed in detail. The model results are found to be well matched with the ATLAS numerical simulation results for different values of drain bias, silicon film thickness, gate-oxide thickness, stack layer thickness and stack materials.

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