Characteristics of cylindrical surrounding-gate $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ heterojunction tunneling field-effect transistors*

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(Received 30 December 2015; revised manuscript received 24 May 2016; published online 25 August 2016)

A III–V heterojunction tunneling field-effect transistor (TFET) can enhance the on-state current effectively, and $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ heterojunction exhibits better performance with the adjustable band alignment by modulating the alloy composition. In this paper, the performance of the cylindrical surrounding-gate $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ heterojunction TFET with gate–drain underlap is investigated by numerical simulation. We validate that reducing drain doping concentration and increasing gate–drain underlap could be effective ways to reduce the off-state current and subthreshold swing (SS), while increasing source doping concentration and adjusting the composition of $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ can improve the on-state current. In addition, the resonant TFET based on $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ is also studied, and the result shows that the minimum and average of SS reach 11 mV/decade and 20 mV/decade for five decades of drain current, respectively, and is much superior to the conventional TFET.

Keywords: tunneling field-effect transistor, surrounding-gate, subthreshold swing, resonant tunneling

PACS: 85.30.Mn, 81.05.Ea, 85.30.Tv **DOI:** 10.1088/1674-1056/25/10/108502

1. Introduction

With the continuous scaling down of the feature size of metal–oxide–semiconductor field-effect transistor (MOSFET), the switching speed, density and functionality of integrated circuits have been improved greatly. But further reducing the device dimensions will increase the leakage current, which results in increased power consumption. The higher power consumption under low supply voltage results from the not so steep subthreshold swing (SS) of MOSFET, with a 60 mV/decade limit at room temperature. In order to solve this problem, new devices such as tunneling FET (TFET)[1–4] and impact ionization FET[5] have been proposed. TFET benefits from the quantum mechanical band-to-band tunneling, which is different from the thermal injection of carriers in MOSFET, and can obtain SS beyond the 60 mV/decade limitation.[6,7]

The on-state current I_{ON} of TFET is determined by the tunneling probability, and is much lower than that of MOSFET. The Wentzel–Kramer–Brillouin approximation provides a way to calculate the tunneling probability T_{WKB}:

$$T_{WKB} \approx \exp\left[-\frac{4\lambda\sqrt{2m^*}E_g^{3/2}}{3q\hbar\left(E_g+\Delta\Phi\right)}\right], \tag{1}$$

where E_g is the bandgap, λ represents the tunneling length, m^* is the effective carrier mass, q is electronic charge, h is the Dirac constant, and $\Delta\Phi$ denotes the energetic difference between the valence band in the source and the conduction band in the channel in the n-type TFET.[6] Equation (1) implies some methods to boost I_{ON}. So various material TFETs with different structures have been studied, including carbon nanotube,[8] PNPN,[9] and heterojunction (Si/InAs, group III–V materials)[10,11] TFETs. Compared with the homojunction TFET, the heterojunction TFET shows superior performance.[12] $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ heterojunction TFETs allows various band alignments through changing the alloy compositions of the source and channel material, which makes it more convenient to design and optimize TFET, such as increasing I_{ON} without deteriorating off-state current I_{OFF} and SS. The I_{ON} can be improved even to the MOSFET level by reducing the effective tunneling barrier height (E_{beff}),[13] so the TFET based on $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ heterojunction possesses great potential applications in the low-power and energy-efficient logical circuits. In order to alleviate short-channel effects, surrounding-gate (SG) structure which has the superior gate-controllability and higher scalability is widely adopted. Previous work focused on the planar $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ heterojunction TFETs.[13,14] Research on the performance of the SG mixed-As/Sb heterojunction TFET with cylindrical cross-section, which can eliminate the corner effect,[15] has not been found so far in the literature.

*Project supported by the National Natural Science Foundation of China (Grant Nos. 61176038 and 61474093), the Science and Technology Planning Project of Guangdong Province, China (Grant No. 2015A010103002), and the Technology Development Program of Shaanxi Province, China (Grant No. 2016GY-075).

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Moreover, gate–drain underlap can be efficient to suppress the I_{OFF} in TFET.

In this paper, we study the cylindrical surrounding-gate $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ heterojunction TFET with gate-drain underlap by numerical simulation. The effects of device parameters and resonant tunneling on the performance of the device are investigated.

2. Device structure

The designed structure is a lateral n-type cylindrical SG-TFET which is shown in Fig. 1. The P^+ source region is $GaAs_xSb_{1-x}$ with carbon-doped concentration N_A, the channel is undoped $In_yGa_{1-y}As$, the N^+ drain region is $In_yGa_{1-y}As$ with silicon-doped concentration N_D, and the dielectric material used as gate oxide layer is HfO_2. R is the channel radius, L_g is gate length, and $L_{underlap}$ represents the underlap length between the gate and the drain. Unless otherwise specified, the channel length L_{ch} is 20 nm, the oxide thickness t_{ox} is 2 nm, $L_{underlap}$ is equal to 10 nm, R is 7 nm, and x and y are equal to 0.35 and 0.7, respectively. The three-dimensional (3D) device simulator Sentaurus[16] is used for simulation, and the dynamic non-local band-to-band tunneling model is activated for current calculation. Besides, under the assumption of high doping concentration in the source and drain, the band-gap narrowing model is enabled and Shockley–Read–Hall recombination model is also included. In order to consider the effect of interface trap on band-to-band tunneling in TFET, the trap-assisted tunneling model is also activated.

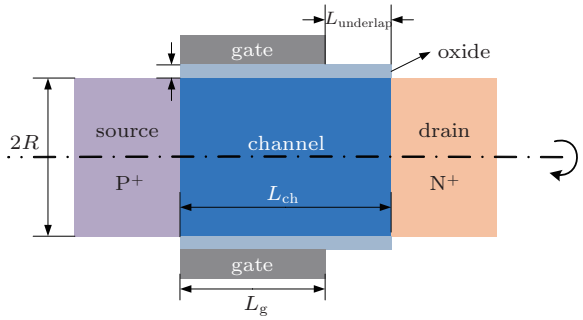


Fig. 1. (color online) Schematic of SG-TFET with gate–drain underlap.

3. Results and discussion

Figure 2 shows the influence of source doping concentration on the characteristics of the heterojunction SG-TFETs. From Fig. 2, it can be observed that, by increasing N_A, there is enhancement in I_{ON} which results from the fact that a higher N_A will make the band steeper and enhance the electric field between the source and channel as shown in Fig. 3, thus tunneling probability increases. However, at $V_{DS} = 0.5$ V and $V_{GS} - V_{OFF} = 0.5$ V, where V_{OFF} is the gate voltage corresponding to $I_{OFF} = 10$ pA/μm, I_{ON} increases more than 30 times when N_A varies from 10^{19} cm^{-3} to 5×10^{19} cm^{-3}, much larger than the two-fold enhancement when N_A varies from 5×10^{19} cm^{-3} to 10^{20} cm^{-3}. The smaller increase in I_{ON} in the latter case results from the higher degeneration of the source region at higher doping concentration, which makes the Fermi level E_{FS} fall below the valence band maximum E_V in the source region and electrons partially occupy the states in the valence band between E_V and E_{FS}, resulting in reduced paired-tunneling states and thus smaller increase in I_{ON}.[17] Figure 4 shows the dependences of transfer characteristics on N_D. It can be seen that N_D hardly influences the on-state performance, since I_{ON} is primarily controlled by the tunneling junction between the source and channel. Nevertheless, I_{OFF} increases with increasing N_D because of the ambipolar behavior.[18] From Figs. 2 and 4, in contrast to MOSFETs, the current of TFET does not change linearly with gate voltage on a semi-logarithmic scale, which results from the band-to-band tunneling mechanism leading to the complex dependences of the tunneling current on energy band profile and available quantum states. The dependence of SS on N_D is plotted in Fig. 5. SS is lower than 60 mV/decade for a drain current range of more than 5 orders of magnitude, and achieves a minimum of 30 mV/decade when N_D is equal to 10^{18} cm^{-3}. It is evident that SS degrades as N_D increases.

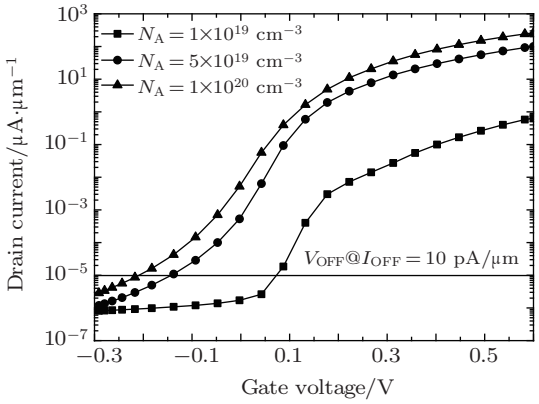


Fig. 2. Plots of drain current versus gate voltage for different values of carbon-doped concentration N_A at $V_{DS} = 0.5$ V and $N_D = 5\times10^{18}$ cm^{-3}.

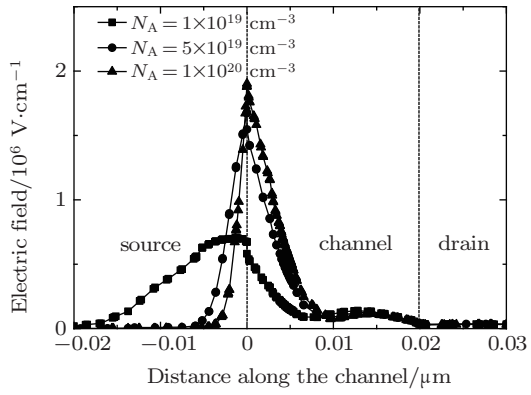


Fig. 3. Plots of electric field versus distance along the channel for different values of carbon-doped concentration N_A at $V_{GS} - V_{OFF} = 0.5$ V, $V_{DS} = 0.5$ V, and $N_D = 5\times10^{18}$ cm^{-3}.

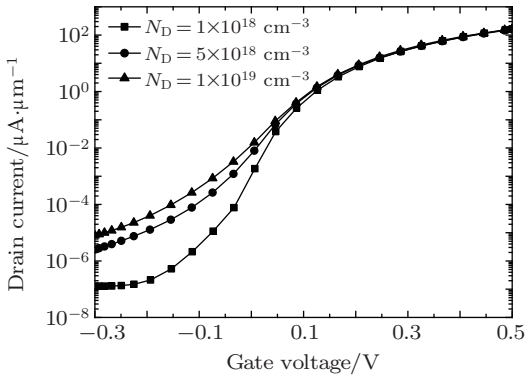


Fig. 4. Variations of drain current with gate voltage for different values of silicon-doped concentration N_D at $V_{DS} = 0.5$ V and $N_A = 10^{20}$ cm^{-3}.

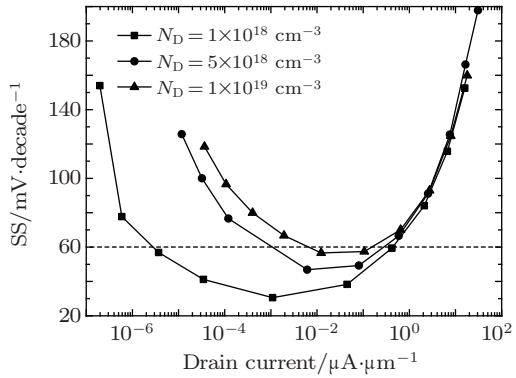


Fig. 5. Plots of SS versus drain current for different values of silicon-doped concentration N_D at $V_{DS} = 0.5$ V and $N_A = 10^{20}$ cm^{-3}.

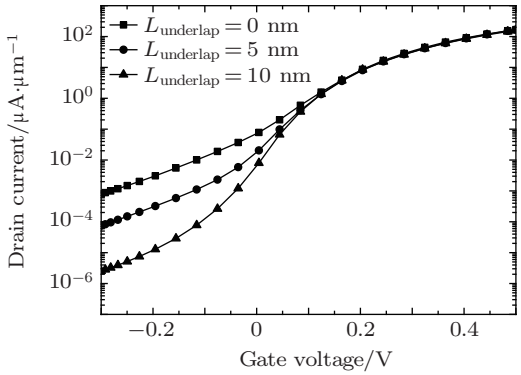


Fig. 6. Curves of drain current versus gate voltage for different values of $L_{underlap}$ at $V_{DS} = 0.5$ V, $L_g = 10$ nm, $N_A = 10^{20}$ cm^{-3}, and $N_D = 5\times10^{18}$ cm^{-3}.

The influences of the gate–drain underlap $L_{underlap}$ on the characteristics of SG-TFET are given in Fig. 6. It can be seen that I_{ON} is scarcely affected by $L_{underlap}$, but I_{OFF} decreases with increasing $L_{underlap}$. When $V_{DS} = 0.5$ V and $V_{GS} = -0.3$ V, I_{OFF} decreases about 300 times as $L_{underlap}$ varies from 0 nm to 10 nm. In the TFET with gate–drain underlap, there is a high-resistance region in the non-gated channel region which makes the electrical field reduced at the channel–drain junction. As a result, the ambipolar behavior which makes the main contribution to I_{OFF} is mitigated, thus I_{OFF} is reduced. Because the high-resistance region is near the drain, the electric field in the source–channel tunneling junction is not influenced by $L_{underlap}$. I_{ON} is controlled by the source–channel tunneling junction, so I_{ON} is insensitive to $L_{underlap}$. Figure 7 gives the dependences of SS on $L_{underlap}$. The advantage of the gate–drain underlap is more evident. When $L_{underlap}$ is 10 nm, SS is lower than the thermal limitation 60 mV/decade of MOSFET for more than 2-decade drain current. Besides, the gate–drain underlap also reduces the area of gate capacity, thus reducing the gate delay.[19]

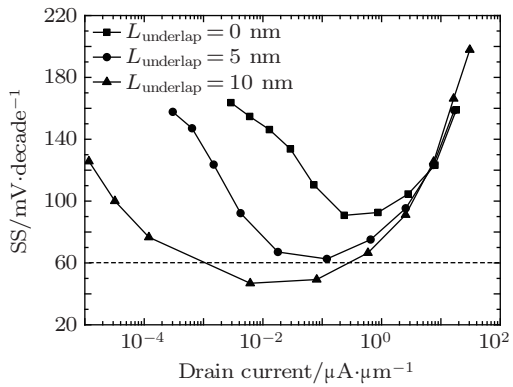


Fig. 7. SS versus drain current for different values of $L_{underlap}$ at $V_{DS} = 0.5$ V, $L_g = 10$ nm, $N_A = 10^{20}$ cm^{-3}, and $N_D = 5\times10^{18}$ cm^{-3}.

Figure 8 presents the transfer characteristics of SG-TFETs at different values of L_g, in which there is no gate–drain underlap. The plot indicates that increasing gate length results in the diminution of I_{OFF}, but unnoticeable change of I_{ON}. When L_g is reduced from 15 nm to 10 nm, due to the direct tunneling from the source to the drain, I_{OFF} increases more than 2 orders of magnitude at $V_{DS} = 0.5$ V and $V_{GS} = -0.3$ V, which is much larger than the increment when L_g is changed from 20 nm to 15 nm. The weak dependence of I_{ON} on L_g is due to the fact that the current in TFET results from the quantum tunneling at the source–channel junction. Figure 9 shows the variations of SS with drain current at different gate lengths. SS decreases with increasing L_g and reaches a minimum value of 27.7 mV/decade when L_g is 20 nm. The current range for SS below 60 mV/decade almost reaches 6 decades.

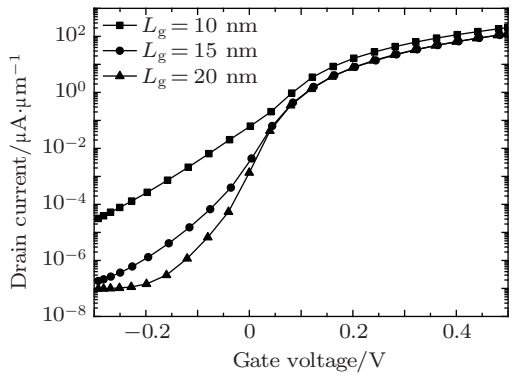


Fig. 8. Variations of drain current with gate voltage for different values of gate length L_g at $V_{DS} = 0.5$ V, $N_A = 10^{20}$ cm^{-3}, and $N_D = 10^{18}$ cm^{-3}.

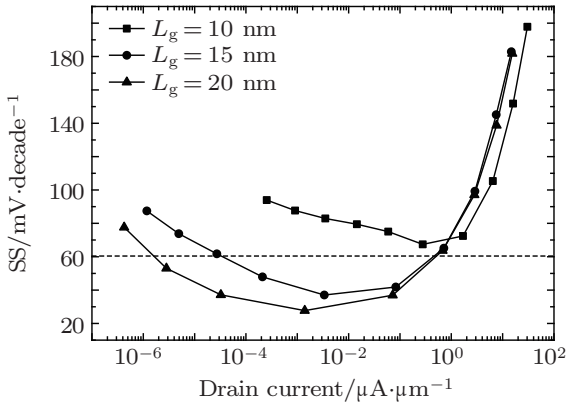


Fig. 9. Variations of SS with drain current for different values of gate length L_g at $V_{DS} = 0.5$ V, $N_A = 10^{20}$ cm^{-3}, and $N_D = 10^{18}$ cm^{-3}.

The band alignment can be designed through modulating the alloy compositions of $GaAs_xSb_{1-x}$ and $In_yGa_{1-y}As$ to easily obtain better device performances. Figures 10 and 11 depict the transfer and SS characteristics of SG-TFETs with different alloy compositions ($x = 0.5$, $y = 0.53$ and $x = 0.4$, $y = 0.65$), at which $GaAs_xSb_{1-x}$ and $In_yGa_{1-y}As$ are lattice-matched, and Eb_{eff} values are 0.5 eV and 0.31 eV, respectively.[13,20] Here, I_{ON} is determined at $V_{DS} = 0.5$ V and V_{GS}–V_{OFF} (at $I_{OFF} = 1$ nA/μm) = 0.5 V. I_{ON} increases from 33 μA/μm to 103 μA/μm, more than 3 times, when Eb_{eff} varies from 0.5 eV to 0.31 eV as shown in Fig. 10. Reducing Eb_{eff} is an effective way to enhance I_{ON}, because smaller Eb_{eff} makes it much easier for electrons to tunnel in the n-type TFET. The simulation shown in Fig. 11 demonstrates that SS becomes better with the scaling down of Eb_{eff}. We can obtain higher drain current and smaller SS at the same time due to the various band alignments in $GaAs_xSb_{1-x}$/$In_yGa_{1-y}As$ system, so the mixed-As/Sb material system is attractive for low-power applications.

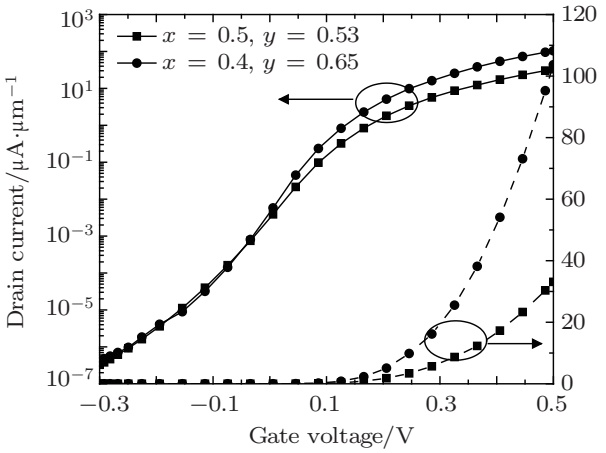


Fig. 10. Curves of drain current versus gate voltage for different material compositions ($x = 0.5$, $y = 0.53$, $Eb_{eff} = 0.5$ eV and $x = 0.4$, $y = 0.65$, $Eb_{eff} = 0.31$ eV) in (dashed) linear and (solid) log scales at $V_{DS} = 0.5$ V, $N_A = 10^{20}$ cm^{-3}, and $N_D = 10^{18}$ cm^{-3}.

Next, the effect of the resonant tunneling is investigated. Compared with the conventional TFET, the resonant TFET (R-TFET) only exchanges the materials between the source region and channel (drain) region.[21] Here, the materials used in the source region and channel (drain) region of the R-TFET are $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$, respectively. Figure 12 shows the lateral band diagrams of the conventional TFET and the R-TFET. In the R-TFET, there is a narrow triangle quantum well between the source and channel due to the larger electron affinity of $In_{0.7}Ga_{0.3}As$ ($\chi = 4.651$ eV) than that of $GaAs_{0.35}Sb_{0.65}$ ($\chi = 4.07$ eV),[22] which creates a double-barrier band structure[21] as shown in Fig. 12(b). According to quantum mechanism, there are discrete energy levels in a quantum well. The way of tunneling through the double-barrier via discrete energy levels is resonant tunneling.[23] The tunneling probability, as a function of tunneling carrier energy, is like Breit–Wigner-type distribution, and can achieve maximum when the energy of tunneling carriers is equal to a quantized energy level. In Fig. 13, the transfer characteristics of the conventional TFET and the R-TFET are plotted. It is obvious that the transfer curve of the R-TFET in the sub-threshold region is much steeper than that of the conventional TFET, which results from the fact that when the energy level of tunneling carriers in the R-TFET aligns with the quantized energy level, the tunneling probability and thus the drain current increases abruptly. The drain current of the R-TFET increases from 10^{-8} μA/μm to 10^{-2} μA/μm with a gate voltage increase of 110 mV. The minimum SS of the R-TFET is 11 mV/decade and SS is below 20 mV/decade over 2.5 decades of drain current as shown in Fig. 14. The average SS of the R-TFET calculated in a drain current range from 10^{-7} μA/μm to 10^{-2} μA/μm, is merely 20 mV/decade, 30 mV/decade lower than the conventional TFET. Because of its excellent sub-threshold performance, the R-TFET may have greater potential applications in very low-voltage and low-power though its on-state current is lower than that of the conventional TFET.

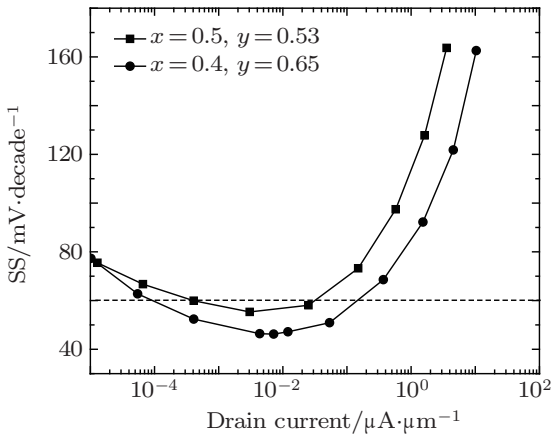


Fig. 11. Curves of SS versus drain current for different material compositions at $V_{DS} = 0.5$ V, $N_A = 10^{20}$ cm^{-3}, and $N_D = 10^{18}$ cm^{-3}.

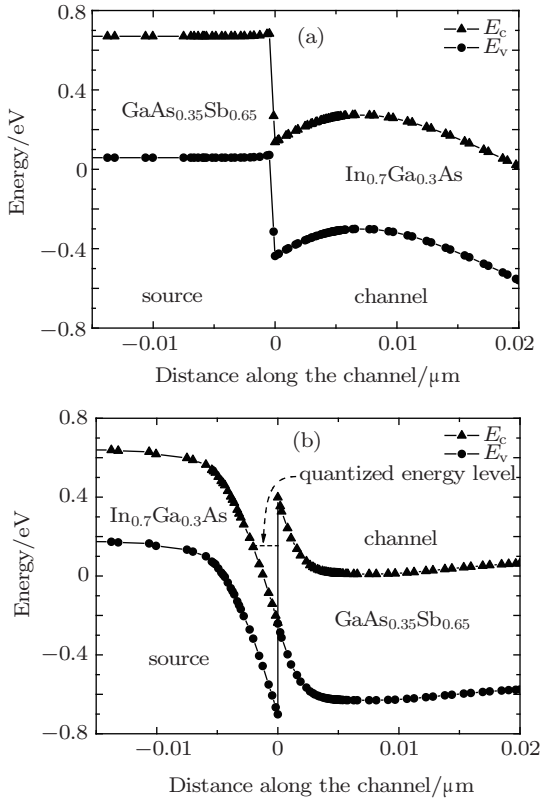


Fig. 12. Energy band diagrams of (a) the conventional TFET and (b) the R-TFET with $L_g = 10$ nm at $V_{GS} = 0$ V.

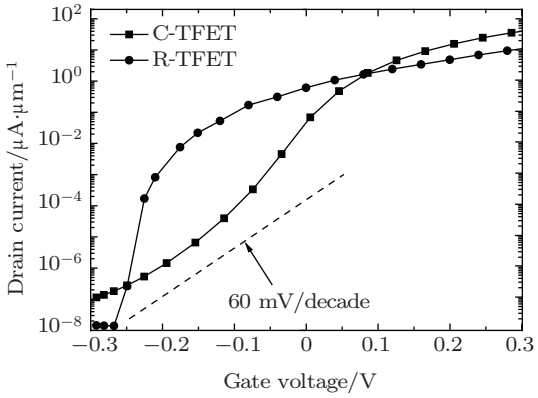


Fig. 13. Transfer curves of the conventional TFET (C-TFET) and the R-TFET, where $V_{DS} = 0.5$ V, $R = 3$ nm, $N_A = 10^{20}$ cm^{-3}, and $N_D = 5 \times 10^{18}$ cm^{-3}.

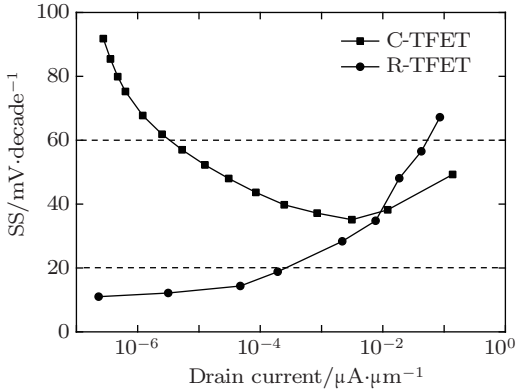


Fig. 14. Curves of SS versus drain current of the C-TFET and R-TFET, where $V_{DS} = 0.5$ V, $R = 3$ nm, $N_A = 10^{20}$ cm^{-3}, and $N_D = 5 \times 10^{18}$ cm^{-3}.

4. Conclusions

The characteristics of cylindrical SG $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ heterojunction TFET with gate–drain underlap are investigated. The effects of doping concentration, gate–drain underlap, gate length, and the compositions of $GaAs_xSb_{1-x}$ and $In_yGa_{1-y}As$ on the performance are analyzed. It turns out that better SS can be obtained through lower drain doping concentration and longer gate–drain underlap, and the drain current can be enhanced by modulating the alloy composition or increasing source doping concentration. In addition, a novel TFET called R-TFET is studied based on $GaAs_xSb_{1-x}/In_yGa_{1-y}As$ staggered-gap heterojunction, and the result shows that the sub-threshold performance is superior to that of the conventional TFET due to its resonant tunneling mechanism. The minimum SS of the R-TEFT is only 11 mV/decade, and its average SS is 20 mV/decade for 5 decades of drain current, 30 mV/decade lower than those of the conventional TFET.

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