# Atomic-layer-deposited $Al_2O_3$ and $HfO_2$ on InAlAs: A comparative study of interfacial and electrical characteristics*

Li-Fan Wu(武利翻)[1,2], Yu-Ming Zhang (张玉明)[1], Hong-Liang Lv (吕红亮)[1,†], and Yi-Men Zhang(张义门)[1]

[1] School of Microelectronics, Xidian University, Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices of China, Xi'an 710071, China

[2] School of Electronic Engineering, Xi'an University of Posts and Telecommunications, Xi'an 710121, China

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$Al_2O_3$ and $HfO_2$ thin films are separately deposited on n-type InAlAs epitaxial layers by using atomic layer deposition (ALD). The interfacial properties are revealed by angle-resolved x-ray photoelectron spectroscopy (AR-XPS). It is demonstrated that the $Al_2O_3$ layer can reduce interfacial oxidation and trap charge formation. The gate leakage current densities are $1.37\times10^{-6}$ A/cm$^2$ and $3.22\times10^{-6}$ A/cm$^2$ at +1 V for the $Al_2O_3$/InAlAs and $HfO_2$/InAlAs MOS capacitors respectively. Compared with the $HfO_2$/InAlAs metal–oxide–semiconductor (MOS) capacitor, the $Al_2O_3$/InAlAs MOS capacitor exhibits good electrical properties in reducing gate leakage current, narrowing down the hysteresis loop, shrinking stretch-out of the $C$–$V$ characteristics, and significantly reducing the oxide trapped charge ($Q_{ot}$) value and the interface state density ($D_{it}$).

**Keywords:** high-$k$ dielectric, atomic layer deposition, InAlAs, characteristics

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## 1. Introduction

The InGaAs-based high electron mobility transistor (HEMT) has been widely studied for the applications in high-speed, low-power and high-frequency circuits due to its low effective electron mass and high electron mobility.[1,2] Its current flow is controlled by a Schottky metal gate. However, the Schottky gate brings a high leakage current. Recently, the InGaAs-based metal–oxide–semiconductor field-effect transistors (MOSFETs) have received much attention because of their relatively low gate leakage currents and large voltage swings compared with those of the Schottky-gate devices.[3] Each of these MOSFET and HEMT architectures typically has a higher band gap barrier layer, such as InAlAs, as a surface material, on which high-$\kappa$ dielectrics will be deposited. Compared with the InP barrier layer, InAlAs provides not only good lattice matching with InGaAs, but also a large conduction band offset with InGaAs, thereby improving the confinement of electrons in the channel. Using *in-situ* epitaxial growth, a high-quality interface between InGaAs and InAlAs can be obtained. However, the interface between the barrier layer InAlAs and high-$k$ oxide still plays an important role in device operation, affecting the subthreshold swing and the threshold voltage.[4] So, it is necessary to investigate interfacial and electrical characteristics between the barrier layer InAlAs and high-$k$ oxide.

$SiO_2$ has been replaced by the high-$k$ dielectric because of its high leakage current when scaling down the device.[5] Research focuses on high-$k$ dielectrics, including $Al_2O_3$,[6] $HfO_2$,[7] and so on. Among these high-$k$ dielectrics, the $HfO_2$ gate dielectric has a high dielectric constant (18–20). However, $HfO_2$ has a smaller bandgap of 5.45 eV than other high-$k$ dielectrics.[8] In comparison, $Al_2O_3$ has a larger band gap of 9 eV, stronger adhesion to many surfaces of material, and serves as a protection layer due to its stabilities against moisture. In recent studies, an $HfO_2$/InAlAs gate stack has been reported in relation to the surface passivation chemistries of InAlAs.[9–13] However, interfacial and electrical characteristics of $HfO_2$/InAlAs MOS have been rarely reported.

In this work, we investigate the interfacial and electrical properties of the ALD-$Al_2O_3$ and ALD-$HfO_2$ gate dielectrics on the InAlAs epitaxial layer. Compared with that of the $HfO_2$/InAlAs capacitor, the capacitance–voltage ($C$–$V$) characteristic of the $Al_2O_3$/InAlAs capacitor is significantly improved, and in particular, the stretch-out of $C$–$V$ curve for the $Al_2O_3$/InAlAs capacitor is considerably shrunk. The interface study is done by angle-resolved x-ray photoelectron spectroscopy (AR-XPS) and the electrical characterizations based on the $C$–$V$ hysteresis, current density–voltage ($J$–$V$), and charge-trapping behavior of $Al_2O_3$ gate stacks on InAlAs are performed to evaluate its potential as an alternative gate dielectric for the InAlAs MOS capacitor.

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†Corresponding author. E-mail: hllv@mail.xidian.edu.cn

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## 2. Experiments

In this work, a 1.5-μm n-type $In_{0.5}Al_{0.5}As$ layer (Si doped to $\sim 1\times10^{17}$ cm$^{-3}$) was epitaxially grown on a semi-insulating n-type GaAs substrate. Prior to deposition, the samples were first rinsed by using acetone and deionized (DI) water, then soaked in HCl (37%) for 1 min for native oxide removal, and finally dipped in $(NH4)_2S$ (10%) for 15 min to remove elemental As and In, cleaned in deionized water for 3 min and dried in $N_2$. Two types of ALD dielectrics, i.e., (I) $Al_2O_3$ (10 nm) and (II) $HfO_2$ (10 nm) film (sample I: $Al_2O_3$/InAlAs MOS capacitor, and sample II: $HfO_2$/InAlAs MOS capacitor), were used for fabricating the high-$k$/InAlAs MOS capacitors. The ALD-$Al_2O_3$ film was deposited at 245 °C by using tri(methyl)aluminum (TMA-Al) and $H_2O$ as the precursors. The ALD-$HfO_2$ film was deposited at 245 °C including an alternating pulse of tetrakis-(ethyl-methyl-amino)-hafnium (TEMA-Hf) and $H_2O$ used as the precursors. Post deposition annealing (PDA) was carried out at 380 °C for 1 min under $N_2$ ambient by rapid thermal annealing (RTA). Finally, an MOS capacitor structure was produced by sputtering Ti/Pt/Au (20 nm/20 nm/200 nm) to form the gate electrode with an area of $1\times10^{-4}$ cm$^2$.

All the $C$–$V$ hysteresis measurements were carried out at a high frequency of 1 MHz at room temperature (295 K). AR-XPS was performed by using a monochromated Al–K$\alpha$ x-ray source (1486.6 eV). The C 1 s line with a bonding energy of 284.6 eV was used as a reference to eliminate the charge effect during the analysis. AR-XPS is a useful tool for profiling depth in a substrate or a hetero-structure. If necessary, the photoelectron take-off angle, $\theta$ (defined as the elevation angle according to the sample surface), was changed by tilting the sample to change the photoelectron escape depth, $t$, in accordance with

$$t = \lambda \times \sin\theta, \tag{1}$$

where $\lambda$ is the inelastic mean free path of photoelectrons.

## 3. Results and discussion

To quantify the density of interfacial trapped charge in high-$k$ oxides on III–V surfaces, the $C$–$V$ hysteresis measurements are executed at a high frequency (1 MHz) and room temperature (295 K), and the results are shown in Fig. 1.

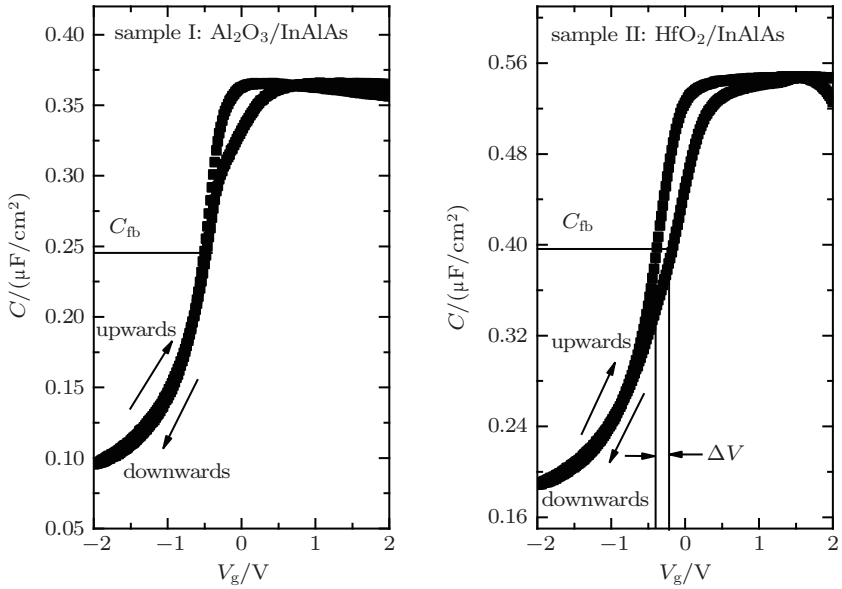



**Fig. 1.** $C$–$V$ characteristics of samples (I) $Al_2O_3$/n-InAlAs and (II) $HfO_2$/n-InAlAs, measured at a frequency of 1 MHz.

The upwards line represents the $C$–$V$ curve measured by the gate voltage swept from −2.0 V to 2.0 V for the $Al_2O_3$/InAlAs capacitor and from −2.0 V to 2.0 V for $HfO_2$/InAlAs capacitor respectively, and the downwards line shows the $C$–$V$ curve contained by the gate voltage swept in the opposite direction. There are obvious accumulation and depletion regions for both MOS capacitors. The hysteresis is likely to be caused by charges trapped at the high-$\kappa$/InAlAs interface as well as in the high-$\kappa$ layer. The $C$–$V$ curves for sample I show reducing stretch-out compared with those for sample II, which implies that the interfacial trapped charge densities for sample I are lower than those for sample II. In addition, as can be seen from Fig. 1, the difference in the flat-band voltage ($\Delta V$) of $C$–$V$ hysteresis for sample I is 0.02 V, which is smaller than the ΔV of 0.16 V for sample II. The value of $Q_{ot}$ (cm$^{-2}$) can be calculated from the following formula through using the $C$–$V$ measurements:

$$Q_{ot} = \frac{C_{ox}\cdot\Delta V}{q}, \tag{2}$$

where $Q_{ot}$ is the oxide trapped charge density, $\Delta V$ is the dif-

ference in the flat-band voltage of $C$–$V$ hysteresis, $q$ is the elementary charge, and $C_{ox}$ is the oxide capacitance. According to $\Delta V$ estimated from the $C$–$V$ hysteresis sweep, the oxide trapped charge densities are $8.7648\times10^{11}$ cm$^{-2}$ for sample II and $7.1980\times10^{10}$ cm$^{-2}$ for sample I, respectively, using an oxide capacitance ($C_{ox}$) $C_{ox} = 0.3599$ μF·cm$^{-2}$ for the $Al_2O_3$ layer and $C_{ox} = 0.5478$ μF/cm$^2$ for the single $HfO_2$ layer. Thus, sample I shows much smaller $Q_{ot}$. This is attributed to the good interface between the InAlAs material and $Al_2O_3$, which prevents interfacial oxide and trap charge from forming. The electrical characterizations of the MOS capacitors are summarized in Table 1 for the $Al_2O_3$ and $HfO_2$ layers as the dielectrics, respectively.

**Table 1.** Electrical properties of MOS capacitors with an area of 100 μm×100 μm for the $Al_2O_3$ and $HfO_2$ layers.

| Dielectric material | $V_{hys}$/V | $C_{ox}/(\mu F/cm^2)$ | $Q_{ot}$/cm$^{-2}$ |
|---|---|---|---|
| $Al_2O_3$ layer | 0.02 | 0.3599 | $7.1980\times10^{10}$ |
| $HfO_2$ layer | 0.16 | 0.5478 | $8.7648\times10^{11}$ |

In order to further study the interface quality of the two samples, the interface state density $D_{it}$ is analyzed. $D_{it}$ can be extracted from the $C$–$V$ curves by the Terman method [14] as follows:

$$C(V_s) = \frac{1}{1/C_{ox} + 1/C_s(V_s)}, \tag{3}$$

$$V_s = \frac{\varepsilon_s q N_a}{2C_s^2}, \tag{4}$$

$$C_{it}(V_s) = C_{ox}\left[\left(\frac{dV_s}{dV_g}\right)^{-1} - 1\right] - C_s(V_s), \tag{5}$$

$$D_{it}(V_s) = \frac{C_{it}(V_s)}{q}, \tag{6}$$

$$E_t - E_i = qV_B - qV_s, \tag{7}$$

where $C_{ox}$ is the insulator capacitance, $V_s$ the surface potential of InAlAs, $V_g$ the gate voltage, $C_s$ the substrate capacitance, $\varepsilon_s$ the relative dielectric constant of the substrate, $E_t$ the energy level of the interface trap state, $E_i$ the intrinsic Fermi level, $qV_B$ the doping-induced Fermi level in the bulk InAlAs, $q$ the unit charge, and $N$ the doping concentration of the substrate. According to the experimental $C$–$V$ curves, we can extract the values of $C_s$ from Eq. (3). Then the relationship between $V_s$ and $V_g$ can be extracted from Eq. (4). Fitting the experimental data, an approximate functional relationship between $V_s$ and $V_g$ can be developed. According to Eqs. (5)–(7), we can obtain the curves of $D_{it}$ versus $E_t$–$E_i$ in Fig. 2.

The midgap $D_{it}$ for sample I is $2.5\times10^{11}$ cm$^{-2}$·eV$^{-1}$, while the value of $D_{it}$ for sample II is $3\times10^{12}$ cm$^{-2}$·eV$^{-1}$. It is found that the interface trap density for sample I is lower than that for sample II, which means that the $Al_2O_3$ layer can effectively reduce the interface trap density, and thus improve the interfacial characteristics on the InAlAs layer. Moreover, $Al_2O_3$ has better lattice matching with the InAlAs epitaxial layer, which may contribute to the low dangling bonds, such as In–, As–, O–. The $Al_2O_3$ is known for its high-temperature stability against recrystallization. But $HfO_2$ forms polycrystalline after annealing 600 °C from the amorphous film. Thus $HfO_2$ is much weaker especially in the temperature stability. This indicates that a thermally stable and reliable $Al_2O_3$/InAlAs capacitor has been obtained.

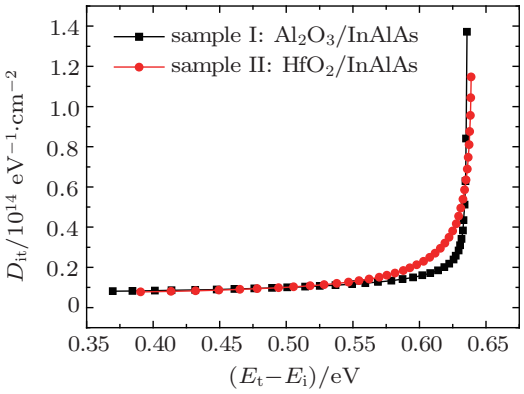



**Fig. 2.** (color online) Curves of $D_{it}$ versus $E_t$–$E_i$ for sample I: $Al_2O_3$/InAlAs and sample II: $HfO_2$/InAlAs.

To investigate the interfacial properties of the $HfO_2$ and $Al_2O_3$ stack films on InAlAs, the chemical states are analyzed by AR-XPS, and the spectra are fitted to Gaussian–Lorentzian functions. Figure 3(a) shows the Al 2p XPS photoelectron spectra obtained from 380 °C annealing for sample I at different take-off angle $\theta$. For sample I, the Al 2p spectrum shows the peak at 74.2 eV, which indicates the formation of $Al_2O_3$ at $\theta = 90°$. It is shown that there is no obvious change in the peak of Al 2p at $\theta = 10°$ and 30°, which suggests that there is no detectable chemical reaction in the $Al_2O_3$ layer. This is also confirmed by the O1s XPS photoelectron spectra shown in Fig. 5, which shows that no other aluminum compounds are formed in the $Al_2O_3$ layer. The XPS probing on the Hf 4f of sample II is shown in Fig. 3(b). For sample II, the Hf 4f spectrum shows two components $4f_{5/2}$ at 18.18 eV and $4f_{7/2}$ at 16.48 eV with a spin–orbital splitting of 1.86 eV at $\theta = 10°$, indicating the formation of $HfO_2$.[15] Figure 3(b) shows that the peaks shift to higher binding energies of 18.41 eV and 16.76 eV in the case of $\theta$=30° and 90° uniformly. The binding energies of Hf $4f_{7/2}$ and $4f_{5/2}$ in the HfAlO film are 16.76 eV and 18.41 eV respectively,[16] therefore it is concluded that a thin Hf–O–Al mixture layer is formed at the interface of samples II. This is nicely consistent with the changes in the O 1s spectra in Fig. 5.

To further investigate the interfaces of sample I and sample II, XPS analyses are performed on elements O and As in the gate dielectric structures. Figure 4 gives the information about the As 3d core level spectra for $HfO_2$ and $Al_2O_3$ on the n-InAlAs at the different values of take-off angle $\theta$.

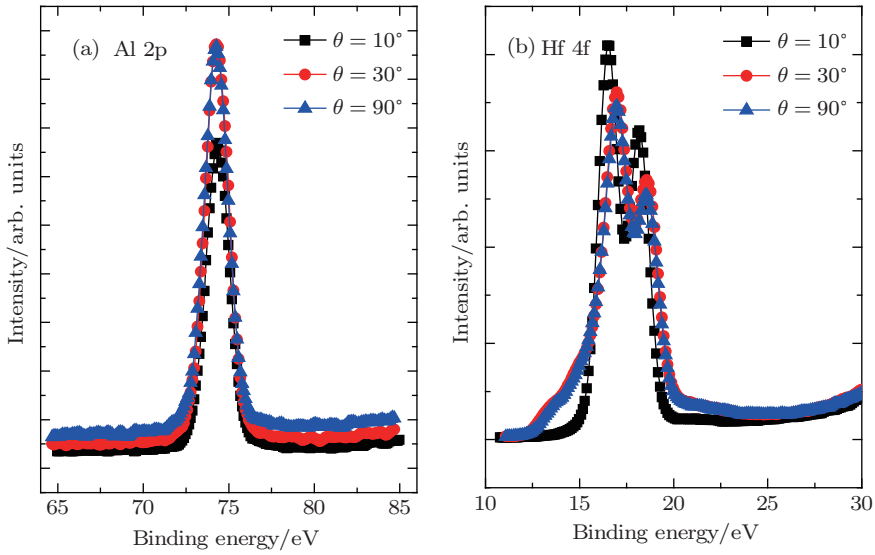



**Fig. 3.** (color online) XPS spectra of (a) Al 2p in sample I and (b) Hf 4f in sample II at different take-off angle $\theta$ (10°, 30°, and 90°).

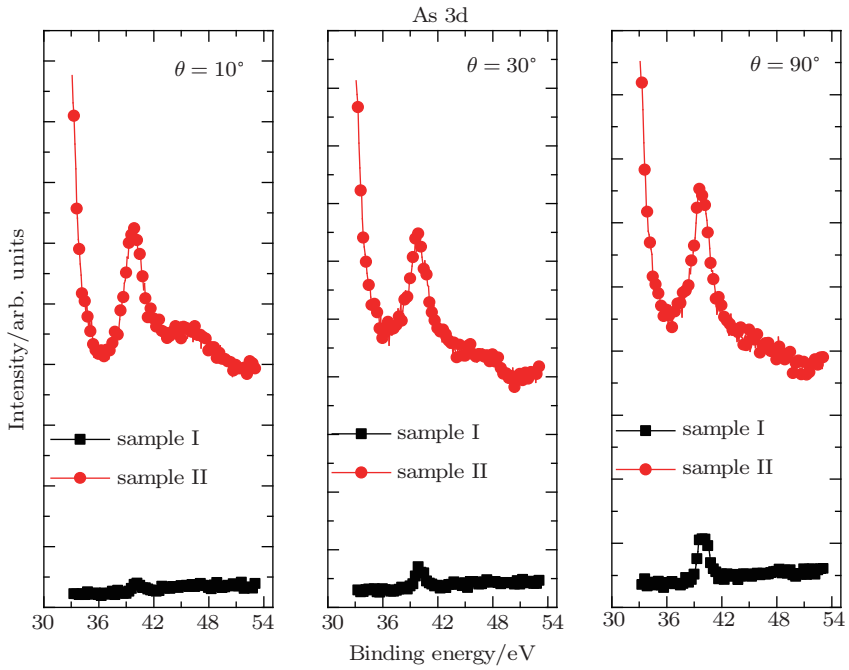



**Fig. 4.** (color online) As 3d photoelectron spectra of sample I and sample II at the different values of take-off angle $\theta$ (10°, 30°, and 90°).

Figure 5 shows the O 1s core level spectra for sample I and sample II at $\theta = 90°$. In Fig. 4, neither As– nor As–O is detected at $\theta = 10°$, and only a little As–O is detected at $\theta = 30°$ for sample I, which reveals that $Al_2O_3$ can be effective in lowering the diffusion of As for sample I. Meanwhile for sample II, a great amount of $As_2O_3$ is seen at $\theta = 10°$ and 30°, which suggests that As has great ability to diffuse in the $HfO_2$ gate dielectric. Figure 5 reveals that a certain number of O dangling bonds are shown in the $HfO_2$ sample, and it is the reason for forming interface trap density.[17,18]

The gate leakage currents of sample I and sample II can be seen in Fig. 6. At a gate voltage of +1 V, the gate leakages of the $Al_2O_3$ and $HfO_2$ samples are $1.37\times10^{-6}$ A/cm$^2$ and $3.22\times10^{-6}$ A/cm$^2$, respectively. The result indicates that sample I shows an appreciably lower gate leakage current than sample II. The gate leakage line is well fitted by the Fowler–Nordheim (FN) tunneling model (data not shown), thus the FN tunneling is the dominant current-conduction mechanism for sample I. The FN tunneling conduction demands a low density of oxide traps and a big band offset, which are required by the large bandgap and the high-quality oxide film of $Al_2O_3$. The decrease of leakage current density of sample I may be attributed to high-thermodynamic stability, high quality, robustness and large conduction band offset between $Al_2O_3$ and InAlAs. The $Al_2O_3$ is known for its high temperature stability against recrystallization and its large measured

conduction band offset with many semiconductor materials; while the higher gate leakage current of sample II may be explained by the smaller band-gap of $HfO_2$ and the change from amorphous $HfO_2$ films to polycrystalline after 600 °C annealing. $HfO_2$ is much weaker especially in the temperature stability. Moreover, the poor lattice-matching and interfacial quality between $HfO_2$ and InAlAs assist the carriers in tunneling the gate dielectric to form the high leakage current.

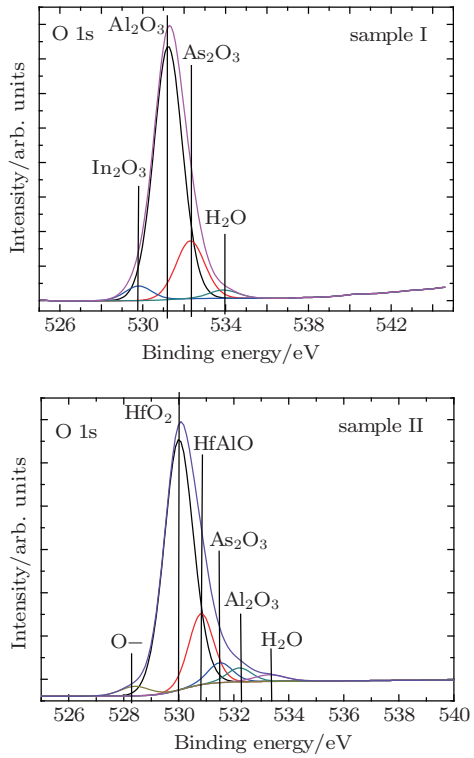



**Fig. 5.** (color online) O1s photoelectron spectra at the take-off angle $\theta = 90°$ for sample (I) $Al_2O_3$/InAlAs capacitor, and sample (II) $HfO_2$/InAlAs capacitor.

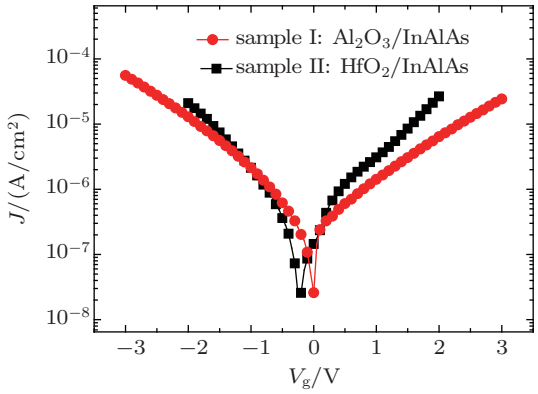



**Fig. 6.** (color online) *J*–*V* characteristics for sample I: $Al_2O_3$/InAlAs and sample II: $HfO_2$/InAlAs.

## 4. Conclusions

In this work, the characteristics of the ALD-$Al_2O_3$/InAlAs and ALD-$HfO_2$/InAlAs MOS capacitors are investigated by AR-XPS. It is found that the $Al_2O_3$ layer can prevent the As 3d from diffusing, and the interfacial oxidation and trap charge from forming. Moreover, the *C*–*V* hysteresis measurements are carried out at a high frequency (1 MHz) and room temperature (295 K). Compared with the $HfO_2$/InAlAs MOS capacitor, the $Al_2O_3$/InAlAs MOS capacitor exhibits good electrical properties in narrowing down the hysteresis loop, shrinking stretch-out of *C*–*V* characteristics, and significantly reducing the oxide trapped charge density ($Q_{ot}$) and the interface state density ($D_{it}$). Additionally, the gate leakage current densities of $1.37\times10^{-6}$ A/cm$^2$ and $3.22\times10^{-6}$ A/cm$^2$ at +1 V for the $Al_2O_3$/InAlAs and $HfO_2$/InAlAs capacitors respectively also prove that there are better electrical properties for the $Al_2O_3$/InAlAs capacitor. Therefore, the $Al_2O_3$/InAlAs MOS capacitor can make the device achieve good performances.

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