Self-compliance multilevel storage characteristic in HfO_2-based device*

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In this paper, the self-compliance bipolar resistive switching characteristic of an HfO_2-based memory device with Ag/HfO_2/Au structure for multilevel storage is investigated. By applying a positive voltage, the dual-step set processes corresponding to three stable resistance states are observed in the device. The multilevel switching characteristics can still be observed after 48 hours. In addition, the resistance values of all the three states show negligible degradation over 10^4 s, which may be useful for the applications in nonvolatile multilevel storage.

Keywords: resistive switching, resistive random access memory, multilevel, self-compliance

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1. Introduction

To solve the scaling limitation of conventional flash memory, various new types of nonvolatile memory (NVM) such as ferroelectric random access memory (FRAM), magnetic random access memory (MRAM), and resistive random access memory (RRAM) have been proposed. Among all these choices, the RRAM device, which is based on resistance change modulated by electrical stimulus, is considered as one of the most promising candidates for next-generation NVM due to its excellent scalability, simple structure, fast switching speed, low power consumption, and nondestructive readout.[1] In view of these excellent characteristics for RRAM devices, a large variety of candidate materials with resistive switching characteristics, such as GeTe,[2] $SrZrO_3$,[3] WO_3,[4] ZrO_2,[5] Cu_2O,[6] and HfO_2[7–9] have been proposed. In recent years, multilevel storage started to arouse the research community's interest due to the achievement of the multilevel storage on a single memory cell that demonstrates the capability of high density storage of RRAM devices.[9–13] So far, several efforts have been devoted to achieving multilevel storage, such as adopting Al/CeO_x/Pt structure to form multiple filament paths in CeO_x films,[13] controlling different voltage values in the reset process,[10,11] and setting different compliance currents in the set process.[11,12]

In this paper, an HfO_2-based RRAM device with a silver top and a gold bottom electrode is fabricated. The device can achieve self-compliance multilevel storage capability. In the set process, dual-step set processes with three stable resistance states can be obtained in the device. These results suggest that the Ag/HfO_2/Au device is potentially suitable for multilevel memory applications without controlling different voltage values or compliance currents.

2. Experimental details

The HfO_2-based RRAM devices in this study were fabricated as follows. A 20-nm thick Cr layer was deposited on the SiO_2/Si substrate followed by a 50-nm thick Au bottom electrode by electron beam evaporation. In this case, the Cr layer was used to improve the adhesion between the SiO_2 and Au bottom electrode. After that, a 40-nm thick HfO_2 film was then deposited on the Au bottom electrode via electron beam evaporation at room temperature. Finally, 50-nm thick square-shaped Ag top electrodes each with an area of 100 μm×100 μm were deposited and determined by photolithography and lift-off process to form an Ag/HfO_2/Au structure device. The current–voltage (I–V) characteristics of the fabricated devices were measured at room temperature, and the bias voltage was applied to the top electrode with the bottom electrode grounded.

3. Results and discussion

Figure 1 shows the typical bipolar I–V characteristics of the Ag/HfO_2/Au device. No initial electrical forming process is needed for our fresh devices to achieve the reversible resistive switching. When the voltage is swept from 0 V to a positive voltage, the current increases abruptly at the set volt-

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age (V_{set}), and the device switches from high resistance state (HRS) to low resistance state (LRS), which is denoted as the set process. Afterwards, by sweeping from 0 V to a negative voltage, a sudden drop in current happens at reset voltage (V_{reset}), and the device switches back from LRS to HRS (denoted as the reset process). Compared with those of other reported HfO_2-based RRAM devices,[7–9] the general trends of *I–V* curves from the structure with Ag/HfO_2/Au are found to be rather different, in which two 'current leaps' occur in each of the *I–V* curves when a positive sweeping voltage is applied, confirming the multilevel set process. Whereas, a multilevel reset process is seldom observed. In the multilevel set process, the device is first set from the HRS to an intermediate resistance state (IRS) and then to the LRS. These 'current leaps' can be observed repeatedly over 30 cycles without any degradation, confirming the reproducibility and stability of the device.

In addition, the 'current leaps' can still be observed even after two days for the same device cell as shown in Fig. 1(b), implying that it is an intrinsic property of this device. It also guarantees that the device is potentially suitable for multilevel storage, and thus suggesting a feasibility to achieve high density memory by means of multilevel storage in future applications.

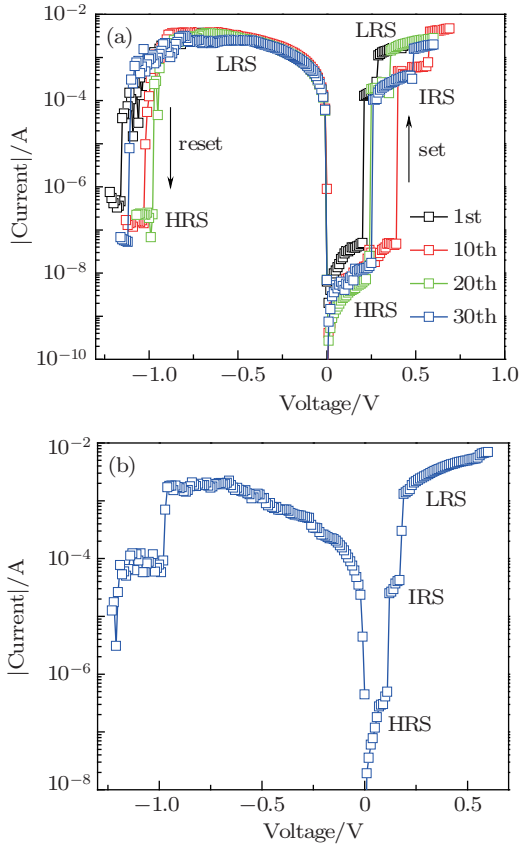


Fig. 1. (color online) *I–V* characteristics of the Ag/HfO_2/Au device (a) for 1st, 10th, 20th, and 30th cycles, (b) after two days. All the measurements are performed at room temperature and under dc sweeping mode.

The distributions of the HRS resistance (R_{HRS}), IRS resistance (R_{IRS}), and LRS resistance (R_{LRS}) during 30 successive resistive switching cycles in the Ag/HfO_2/Au device are presented in Fig. 2. The mean values (standard deviations) of R_{HRS}, R_{IRS}, and R_{LRS} for the Ag/HfO_2/Au device are 8.39×10^7 (1.25×10^8) Ω, 1255 (470) Ω, and 162 (22) Ω, respectively. The values of the coefficient of variation (σ/μ, σ is the standard deviation, μ is the mean value) of R_{HRS}, R_{IRS}, and R_{LRS} are 150.0%, 37.5%, 13.6%, respectively. Compared with R_{IRS} and R_{LRS}, the R_{HRS} shows a larger variation, which have the same tendencies as those reported in other work.[7–9] According to the experimental observations, it is sure that the fluctuant distributions of the R_{HRS}, R_{IRS}, and R_{LRS} make the stability of the resistance ratio reduced. Even though the decrease in the resistance ratio for our Ag/HfO_2/Au device, the average resistance ratio R_{HRS} : R_{IRS} : R_{LRS} of the three resistance states is still about 5×10^5:8:1, which provides a sufficient margin of resistance ratio for the periphery circuit to distinguish different resistance states, and thus guarantees multilevel storage possibility. To further confirm the potential in multilevel storage application, the retention characteristics of the three resistance states are investigated at room temperature, as shown in Fig. 3. After switching, a continuous 0.1-V voltage stress is applied, and the resistance is sampled every 100 s. The resistance values of the HRS, IRS, and LRS of the device are stable and show negligible degradation over 10^4 s, confirming the nonvolatile nature and the nondestructive readout characteristics of the device, thereby guaranteeing its good stability for RRAM applications.

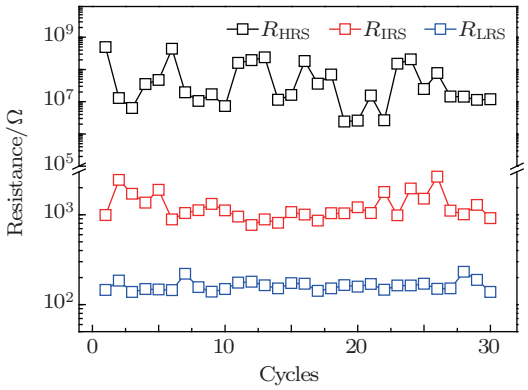


Fig. 2. (color online) Distributions of the R_{HRS}, R_{IRS}, and R_{LRS} during 30 successive resistive switching cycles in the Ag/HfO_2/Au device.

So far, several mechanisms and hypothetical models have been proposed to explain resistive switching phenomena, such as trap charging and discharging,[14] Schottky contact,[6] motion of oxygen vacancies in the insulating oxide film,[7] and the forming and rupture of conductive filaments (CFs).[9,12,13,15] However, the possible underlying mechanisms of the resistive switching phenomenon are surprisingly divergent and not yet clearly understood. To understand the switching mechanisms of the Ag/HfO_2/Au memory devices, the log–log plot of the *I–V* characteristic at

LRS is shown in the inset of Fig. 4. Through this fitting curve, it should be noticed that the slope of the LRS curve is very close to unity (slope = 1.01), which shows ohmic conduction with a slope of one. This result indicates that the resistive switching of the Ag/HfO_2/Au memory device is believed to be related to the formation and dissolution of metallic CFs inside the HfO_2 layer.[4,5,9,15] For the fabricated Ag/HfO_2/Au memory device, when a positive voltage is applied to the top electrode, a multilevel set process occurs. This result, we believe, may be related to the formation of multiple CFs in the set process, which is similar to the behavior of the Al/CeO_x/Pt memory device.[13] For the reset process, when it comes to the rupture of CFs, there is a general debate nowadays. Some reported results showed that the thermal dissolution of the CFs was the mechanism for the reset process.[16–18] But others believed that the rupture of CFs was due to an electrochemical effect.[4,15] To understand the dominant mechanism of the Ag/HfO_2/Au device in the reset process, further analysis identifies the correlation between R_{LRS} and reset current (I_{reset}) as shown in Fig. 4. The I_{reset} is closely correlated with its R_{LRS}. High I_{reset} is needed for small R_{LRS}, which is in accordance with the thermal dissolution model.[16,17] However, no distinct correlation is found between R_{LRS} and the reset voltage, which suggests that electrochemical reactions may not play a dominant role in the reset process of the Ag/HfO_2/Au device even if they exist. Instead, the reset process is very likely to be mediated by Joule heating.

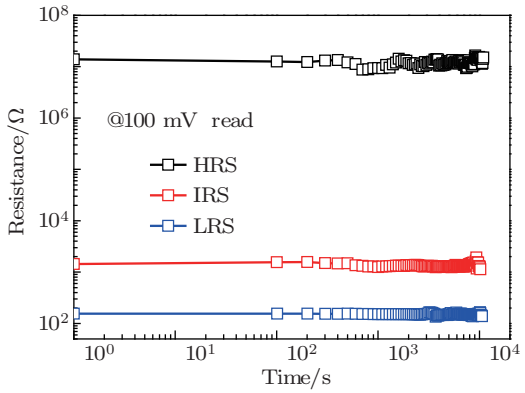


Fig. 3. (color online) Retention characteristics of the HRS, IRS, and LRS resistances for the Ag/HfO_2/Au device under a continuous 0.1-V read voltage.

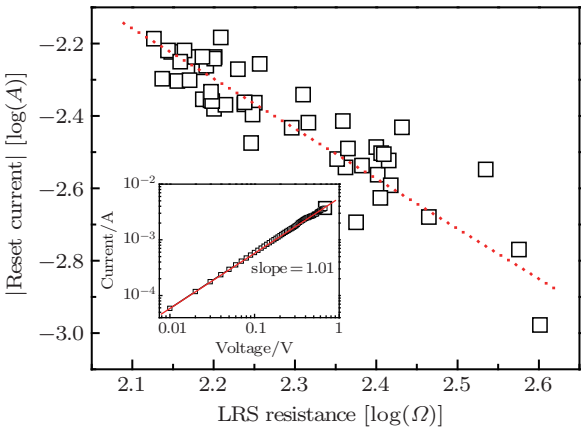


Fig. 4. (color online) LRS resistance dependence of reset current of the Ag/HfO_2/Au device. The inset shows *I*–*V* characteristic at the LRS in a double-logarithmic scale.

4. Conclusions

The resistive switching characteristics of Ag/HfO_2/Au RRAM devices are demonstrated. These devices exhibit their self-compliance multilevel storage characteristics without controlling different voltage values or compliance currents. The conduction mechanism of the set process is very likely to be mediated by forming multiple CFs, and the correlation between LRS resistance and reset current suggests that Joule heating is a dominant effect in the reset process. Self-compliance multilevel storage, enough resistance ratios between different resistance states, and good data retention demonstrate suitability for future memory applications.

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