Improved double-gate armchair silicene nanoribbon field-effect-transistor at large transport bandgap

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The electrical characteristics of a double-gate armchair silicene nanoribbon field-effect-transistor (DG ASiNR FET) are thoroughly investigated by using a ballistic quantum transport model based on non-equilibrium Green's function (NEGF) approach self-consistently coupled with a three-dimensional (3D) Poisson equation. We evaluate the influence of variation in uniaxial tensile strain, ribbon temperature and oxide thickness on the on-off current ratio, subthreshold swing, transconductance and the delay time of a 12-nm-length ultranarrow ASiNR FET. A novel two-parameter strain magnitude and temperature-dependent model is presented for designing an optimized device possessing balanced amelioration of all the electrical parameters. We demonstrate that employing HfO_2 as the gate insulator can be a favorable choice and simultaneous use of it with proper combination of temperature and strain magnitude can achieve better device performance. Furthermore, a general model power (GMP) is derived which explicitly provides the electron effective mass as a function of the bandgap of a hydrogen passivated ASiNR under strain.

Keywords: silicene, double-gate field-effect-transistor, non-equilibrium Green's function, tight binding

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1. Introduction

The monolayer honeycomb structure of silicon, silicene,[1] has appeared as an attractive one-atom thick material that might be highly compatible with the current silicon nanoelectronic technology. Similar to graphene,[2] silicene is also a gapless semimetal with linearly crossing bands near the Fermi level. Carriers in a silicene sheet are projected to face massless behavior in the vicinity of the Dirac point that would lead to a quite large mobility. Silicene stabilizes to form an unprecedented low-buckled (LB) geometry.[3] The height difference between the two nearest neighboring atoms in silicene, provides a tunable bandgap and makes this silicon allotrope a good candidate for switching and modulation applications. Exhibiting many characteristics of topological-insulators,[4] a quantum spin Hall effect[5] and attractive optoelectronic properties[6] are some of the distinguished aspects of silicene. Beside the aforementioned properties, high mechanical strength and elasticity[7,8] and low temperature synthesis,[9] altogether facilitate the conditions for the integration of silicene-based devices.

Scaling down the channel length of the field-effect-transistor (FET) makes the device suffer from short channel effects.[10] In order to enable continued FET scaling, an alternative channel geometry/material can be employed. Among the different classes of channel materials under study, the two-dimensional (2D) material silicene is of great importance due to the fact that it would be easier to adjust next-generation FETs to the silicene process technology. Meanwhile, the single layer material provides extremely good gate control over the channel. In this sense, silicene-based FETs are expected to greatly suppress short channel effects and provide better scalability of the device. Most recent, encapsulated silicene FET fabrication provided the first proof of concept for the silicene devices. Nevertheless, research on the application of silicene nanoribbons as the channel material of FETs is in their infancy and requires more comprehensive investigations.[9]

According to the International Technology Roadmap for Semiconductors (ITRS),[11] at 12-nm technology node where current FETs reach their physical scaling limits,[12] for silicene-based FETs to be an ideal alternative, a minimum gap of about 0.4 eV is required. A suitable bandgap for electronic applications can be achieved by patterning silicene into a narrow ribbon.[13] Independent of different shapes of the ribbon, armchair silicene nanoribbon (ASiNR) with 4 dimer lines along the width, 4-ASiNR, has great potential to be used in the electronics due to its large transport bandgap. In this paper, main electrical parameters of 4-ASiNR double-gate (DG) FET which play an important role in assessing the performance of the transistor, i.e., on–off current ratio, subthreshold swing, on-state saturation current, transconductance, and the delay time are calculated under different physical constraints and varying design parameters including the ribbon temperature, gate insulator thickness/material and uniaxial tensile strain. A new model is also proposed which determines appropriate values of temperature and strain to pave the way for designing a device with optimized performance suitable for digital and

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analog applications.

The *ab initio* study of quantum transport,[14] semiclassical top-of-the-barrier[15] and analytical electrical transport[16] are the three theoretical models that have been explored for the silicene-based FETs. However, a 3D coupled Poisson-quantum transport model to accurately evaluate the electrical characteristics of a DG silicene FET has not been explored yet. In this paper, numerical simulations are carried out based on the self-consistent solution of the 3D Poisson and Schrödinger equations, within the non-equilibrium Green's function (NEGF) formalism,[17] implemented in NANOTCAD ViDES simulator.[18,19] The nearest-neighbor tight-binding (TB) Hamiltonian is expressed on a p_z orbital basis set in the real-space.[20]

The rest of this paper is organized as follows: Section 2 discusses the band structure calculation of the unstrained and uniaxially tensile strained ASiNR, where an analytical formula is derived for the effective mass as a function of bandgap of the ribbon and the strain. Next, it elucidates the quantum transport of DG ASiNR FET within NEGF approach. In Section 3, the influence of physical and structural parameters on the electrical characteristics of 4-ASiNR FET is investigated. The method for designing a device with balanced electrical parameters is thoroughly presented in Section 4. In Section 5, we provide a summary.

2. Approach

The schematics of the device under study and the potential profile along the channel are presented in Fig. 1. The DG structure is employed to provide better gate electrostatic control over the channel. For the channel and source/drain regions, we use a single-layer ASiNR of the family $N = 3m+1$ (m is a positive integer). It is well known that this family of 2D materials is semiconducting with promising characteristics for switching applications.[21] The intrinsic channel length is $L = 12$ nm and the gate insulator thickness is $t_{ox} = 2$ nm of SiO_2. Source/drain structures are considered to be heavily doped. In this case, unlike Schottky barrier (SB) FETs, the potential barrier height and conductance of ASiNR channel are efficiently modulated by the gate voltage.[19] In order to evaluate the performance potential of 4-ASiNR FET, a two-step procedure is followed. In the first step we use TB method to choose a proper channel structure with the desired energy bandgap and eventually in the second step, we compute the ballistic drain current and electrical parameters of 4-ASiNR FET based on NEGF formalism, employing the device Hamiltonian together with the self-consistent potential.

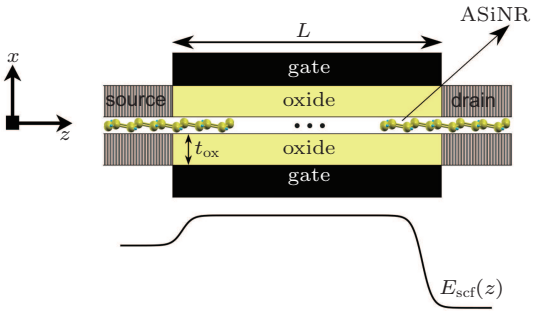


Fig. 1. (color online) Schematics cross-section of (top) the simulated DG FET with the intrinsic 4-ASiNR as the channel material and (bottom) the self-consistent electrostatic potential profile along the device.

2.1. Electronic bandstructure calculations

We have employed TB approach for computing the energy bandgap of ASiNRs as a function of the ribbon's width shown in Fig. 2(a). Related energy values are verified by density functional theory (DFT) approach.[13] The dangling bonds at the edges of the ASiNRs are assumed to be passivated by H atoms and additionally, related TB parameters are obtained via first principle plane wave calculations.[22] Analogous to graphene, the energy bandgap of ASiNRs gradually reduces as the ribbon width increases.[23] ASiNRs with low energy bandgap suffer from a high band-to-band tunneling (BTBT) subthreshold leakage current, which may ultimately limit the performance and scalability of FETs.[24] Accordingly,

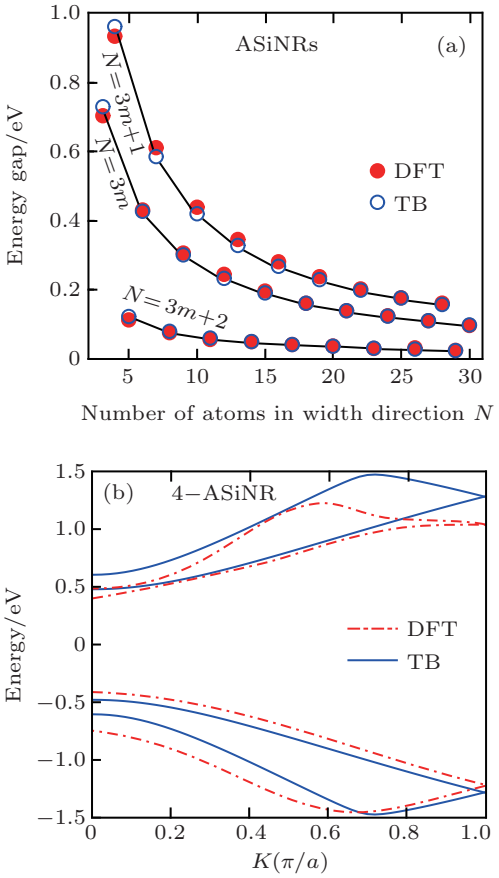


Fig. 2. (color online) (a) Energy bandgap of ASiNRs as a function of the ribbon's width calculated by TB formalism and verified by DFT approach. (b) E–K dispersion of relaxed 4-ASiNR.

in this work we focus on 4-ASiNR with a bandgap value of 0.95 eV and width of $W = 5.75$ Å to achieve efficient performance with suppressed band-to-band leakage current. Figure 2(b) shows the electronic band structure for the undeformed 4-ASiNR. Electron effective mass can be calculated by fitting a parabola at the minimum of the first conduction band, at $K = 0$.

Strain is a well-known efficient method, which modulates the electrical transport properties of a nanoscale system. This procedure has a significant influence not only on the energy bandgap but also on the effective mass. We analyze the effect of uniaxial tensile strain on the electronic properties of 4-ASiNR within a TB approach. The applied strain is limited to 5%, to ensure that we are in the elastic response regime. The Harrison's model is utilized to modify the binding parameters for the strain calculations.[25] In the presence of strain, each binding parameter is scaled down by a dimensionless factor $\|l_0/l\|^2$, where l_0 and l are the unstrained and strained bond-lengths, respectively. We have calculated the energy bandgap and the electron effective mass of 4-ASiNR versus the uniaxial strain as depicted in Fig. 3. Over the strain range considered, the effective mass and energy bandgap have a similar trend and show the family behavior. As mentioned, the electron effective mass is calculated by

$$m_{\mathrm{e}}^{*} = \hbar^2 \frac{1}{\left(\dfrac{\mathrm{d}^2 E(K)}{\mathrm{d}K^2}\right)}, \tag{1}$$

where $E(K)$ is the E–K dispersion relation.

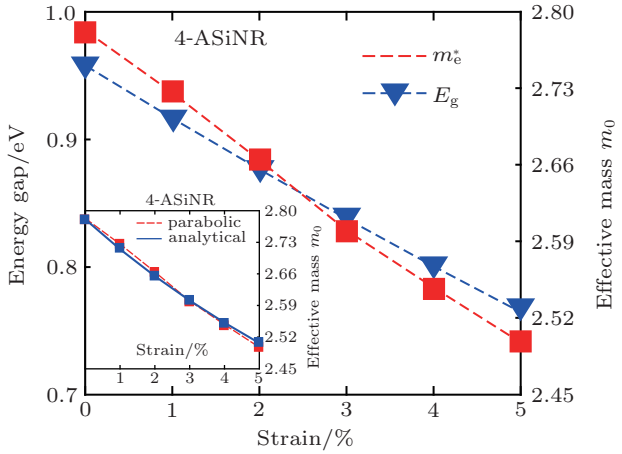


Fig. 3. (color online) Energy bandgap and the electron effective mass of 4-ASiNR as a function of the uniaxial tensile strain. The inset image shows the electron effective mass calculated by the analytical formula compared with the effective mass value derived from the E–K dispersion relation.

We present a general model power (GMP) to access an explicit relation between the electron effective mass and the bandgap value of ASiNR under strain. The analytical formula is applicable for different indexes of ASiNR and defined as follows:

$$G(\varepsilon) = \frac{m_{\mathrm{e}}^{*}(\varepsilon)}{E_{\mathrm{g}}(\varepsilon)(\varepsilon+1)} \approx G(0)(\varepsilon+1)^{b(\Delta l - l_0)}, \tag{2}$$

$$m_{\mathrm{e}}^{*}(\varepsilon) \approx G(0)E_{\mathrm{g}}(\varepsilon)(\varepsilon+1)^{b(\Delta l - l_0)+1} = \frac{m_{\mathrm{e}}^{*}(0)}{E_{\mathrm{g}}(0)}E_{\mathrm{g}}(\varepsilon)(\varepsilon+1)^{b(\Delta l - l_0)+1}, \tag{3}$$

where ε is the strain magnitude, $G(\varepsilon)$ is a general function, $E_{\mathrm{g}}(\varepsilon)$ is the energy gap, and $m_{\mathrm{e}}^{*}(\varepsilon)$ is the electron effective mass, all as a function of the applied strain. The buckling value of silicene, b, is considered to be 0.44 Å and $\Delta l = l - l_0$ is introduced as the difference between the unstrained and strained bond-length. The electron effective mass calculated directly by this analytical formula shows good agreement with the effective mass derived from the bandstructure of the nanoribbon.

2.2. Transport calculation

The ballistic transfer characteristic is calculated by using the NEGF formalism.[17] The retarded Green's function of the channel, G_{ch}, can be obtained as follows:

$$G_{\mathrm{ch}} = [(E + \mathrm{i}\eta)I - (H_{\mathrm{ch}} + U + \beta_{\mathrm{S}}^{\dagger} g_{\mathrm{S}} \beta_{\mathrm{S}} + \beta_{\mathrm{D}} g_{\mathrm{D}} \beta_{\mathrm{D}}^{\dagger})]^{-1}, \tag{4}$$

where E is the energy grid matrix for different energy levels, η is an infinitesimal positive energy value (10^{-5} eV in this simulation), I is the identity matrix, H_{ch} is the Hamiltonian of the channel derived from the TB approach, U is the electrostatic potential obtained by solving the 3D Poisson equation self-consistently, using Newton–Raphson (NR) method, coupled with the NEGF formalism,[18,19] $\beta_{\mathrm{S(D)}}$ is the coupling matrix between the channel and source (drain) reservoir, and $g_{\mathrm{S(D)}}$ is the surface Green's function of the respective contact which can be calculated using an iterative scheme developed by Sancho *et al.*[26]

Once G_{ch} is obtained, the transmission probability, $T(E)$, of ASiNR FET can be evaluated for energies in the transport direction as $T(E) = \mathrm{Trace}\left[\Gamma_{\mathrm{S}} G_{\mathrm{ch}}\, \Gamma_{\mathrm{D}} G_{\mathrm{ch}}^{\dagger}\right]$, where $\Gamma_{\mathrm{S(D)}}$ is the broadening function for the source (drain) contact and is defined as $\Gamma_{\mathrm{S(D)}} = -2\,\mathrm{Im}\left[\beta_{\mathrm{S(D)}}^{\dagger} g_{\mathrm{S(D)}} \beta_{\mathrm{S(D)}}\right]$. Finally, the ballistic current through the device can be computed by[27]

$$I_{\mathrm{S}\to\mathrm{D}} = \frac{2q}{h}\int \mathrm{d}E\, T(E)\left[f_{\mathrm{S}}(E) - f_{\mathrm{D}}(E)\right]. \tag{5}$$

Here, $f_{\mathrm{S(D)}}$ is the source (drain) Fermi function at a fixed temperature.

3. Results and discussion

The transfer characteristic of an 4-ASiNR FET is presented in Fig. 4 for three different power supply voltages. Subthreshold swing and the transconductance are the electrical parameters, which help assess the switching behavior of the device and can be directly calculated from the transfer characteristic.[28] Ambipolar conduction, characterized by a superposition of hole and electron currents is observed in the I_{D}–V_{G} curves. However, ambipolarity and the increase of

the drain voltage enhance the off-state leakage current, I_{OFF}. Here, I_{OFF} is defined as the minimum of the drain current in the transfer characteristics. The higher I_{OFF} implies the higher power dissipation in the off-state as well as a lower on–off current ratio (I_{ON}/I_{OFF}) for the 4-ASiNR FET. The variation of the on-state current by the drain voltage is negligible. This is due to the fact that the ballistic transport condition is considered in our initial assumption and any scattering mechanism that may proportionally increase the channel resistance is ignored.

Among the important electrical parameters of ASiNR-FET, on–off current ratio and subthreshold swing are two significant parameters for low power fast switching speed applications whereas transconductance and intrinsic delay are remarkable for telecommunication usage.[28,29] The impact of several design parameters including temperature, uniaxial tensile strain, and gate insulator thickness on the electrical characteristics of 4-ASiNR is thoroughly investigated. The results are presented in Figs. 5(a)–5(d). As implied in Table 1, each parameter is considered independently to assess its effect on the performance of 4-ASiNR FET.

The first figure of merit that is perceived is the on–off current ratio, Fig. 5(a). Here, I_{ON}/I_{OFF} has a decreasing trend with several increasing values of the uniaxial tensile strain from 1% to 5%. This trend is attributed to the fact that there is a reverse relationship between the source to the drain tunneling probability of the off-state current and the effective mass value as the strain magnitude is increased. However, the on-state current is not considerably sensitive to the energy bandgap variation.[24]

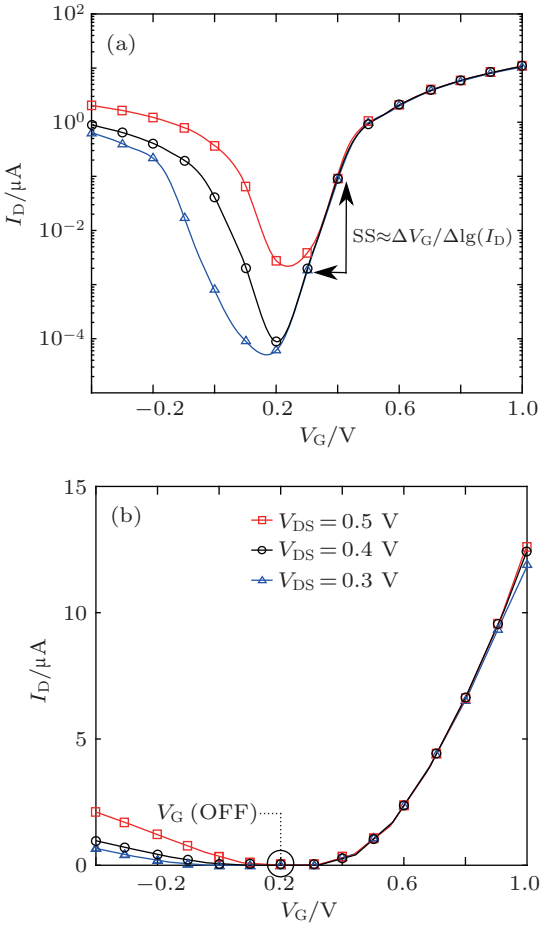


Fig. 4. (color online) I_D–V_G transfer characteristic in (a) logarithmic and (b) linear scales of 4-ASiNR FET for V_{DS} = 0.3, 0.4, and 0.5 V. Subthreshold swing is calculated as SS ≈ $\Delta V_G/\Delta \lg(I_D)$ from Fig. 4(a) and the transconductance is computed as $g_m = dI_D/dV_G$ around the on-state region (V_G(OFF) + V_{DS}) extracted from Fig. 4(b).

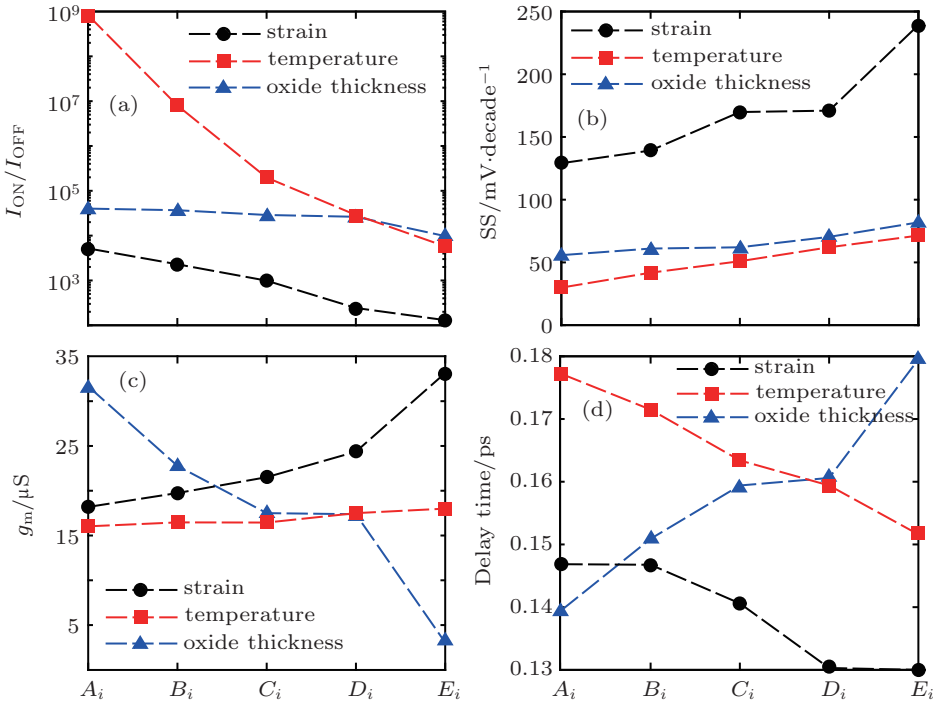


Fig. 5. (color online) (a) On–off current ratio in logarithmic scale, (b) subthreshold swing, (c) transconductance, and (d) the delay time characteristics of a 4-ASiNR FET for V_{DS} = 0.4 V; A_i–E_i classes are selected according to Table 1.

Table 1. Design parameters that are employed for assessing the performance of 4-ASiNR FET, related results are depicted in Fig. 5.

Parameters	A_i	B_i	C_i	D_i	E_i	Constant parameters
Strain/%, $i = 1$	1	2	3	4	5	$t_{ox} = 2$ nm & $T = 300$ K
Temperature/K, $i = 2$	150	200	250	300	350	$t_{ox} = 2$ nm & strain = 0%
Oxide thickness/nm, $i = 3$	1	1.5	2	2.5	3	$T = 300$ K & strain = 0%

The gate capacitance of DG structure, C_G, can be modeled as a series combination of the gate oxide capacitance, $C_{ox}(\propto 2k\varepsilon_0/t_{ox})$, and the quantum capacitance, C_Q, which is proportional to the density of states.[30] In the off-state region, as the temperature increases, thermal energy increases the carrier concentration in the conduction band that significantly results in the channel conductance and consequently the leakage current enhancement. However, in the on-state region, C_Q increases as compared with C_{ox} which implies that the electron concentration in the conduction band exceeds the density of states. As a result, due to the high carrier concentration, the on-state current is not supposedly influenced by the temperature. Evidently, on–off current ratio degrades significantly as the temperature goes beyond 150 K. The impact of gate insulator thickness is assessed to evaluate the electrical performance of the unstrained device at room temperature. For the FETs including heavily doped contacts, the gate merely modulates the channel conductance. The increase of the gate insulator thickness induces an unreliable gate control over the channel[31] that eventually results in the increase of the subthreshold leakage current and a gentle degradation of the on–off current ratio.

Next, we focus on subthreshold swing (SS). This parameter determines how efficiently the transistor can be turned off by varying the gate source voltage, depicted in Fig. 5(b). Thermionic emission current mechanism limits the subthreshold swing value of the conventional metal-oxide-semiconductor FET to 60 mV/dec at room temperature,[32] but this value may decrease in FETs based on 2D materials. Due to the dominance of source-to-drain tunneling current in devices with a reduced energy bandgap and a lower electron effective mass, SS increases as the strain value is increased. The saturation drain current is almost not affected by the temperature hence subthreshold swing faces a gentle upward slope as the temperature goes beyond 150 K. Additionally, as expected, SS has a mild upward trend as the gate insulator thickness increases to 3 nm.

The impact of key design parameters on the transconductance of the device under study is presented in Fig. 5(c). The transconductance of ASiNR FETs is comparable with the related value of the armchair graphene nanoribbon (AGNR) FETs.[33] Obviously, the transconductance depends upon two parameters, i.e., the carrier concentration and the carrier mobility. As discussed in Section 2, the energy bandgap in the nanoribbon reduces as the strain magnitude is increased. Similar to graphene, it can be argued that there exists an inverse relationship between the carrier mobility and the bandgap value of ASiNR.[34] The carrier mobility is increased as the strain value is enhanced but the carrier concentration remains almost unvaried, hence the g_m value increases in highly strained structure. As implied earlier, the carrier concentration and consequently the drain current in the on-state regime are not sensitive to the temperature variation. Furthermore, in the absence of phonon scattering the carrier mobility variation is negligible.[35] Accordingly, an approximate constant g_m is expected. Overall, transconductance is defined as a measure of the sensitivity of drain current amplitude to any change in gate-bias voltage. For the thicker oxide layers, gate control over the channel and naturally, g_m are reduced.

The final performance metric considered here is the intrinsic switching delay time. The delay time shows how fast a transistor can switch and is calculated as $\tau = (Q_{ON} - Q_{OFF})/I_{ON}$, where $Q_{ON(OFF)}$ is the total charge in the channel in the on(off)-state.[36] Impact of strain, temperature, and gate oxide thickness on the intrinsic delay time is presented in Fig. 5(d). It is straightforward to see that the off-state charge density becomes excessive due to the BTBT phenomena in narrow gap devices with a light carrier effective mass as the strain magnitude is increased. However, the on-state charge density and drain current remain approximately constant. Evidently, the intrinsic delay time decreases and therefore the switching performance of 4-ASiNR improves with the tensile strain. Similarly, the intrinsic delay time progressively reduces as the temperature increases. This trend is due to the fact that at low gate voltages, thermal energy given to the carrier helps them to increase thermionic emission current from source to the channel that as a consequence gives rise to the increase of carrier concentration in the channel. As the gate voltage increases, the influence of thermal energy on the on-state charge density and drain current variation is negligible.[37] On the contrary, as predicted, the intrinsic delay time enhances considerably with the gate oxide thickness increment. In this condition, the time required for the injection of charge carriers from source into the channel increases and consequently a slow transition occurs from the on-state to the off-state, so by assuming a constant on-state current, employing a thicker gate oxide increases the intrinsic delay time.

In this step, the effect of gate insulator material on the performance of unstrained 4-ASiNR FET is analyzed comprehensively for $T = 300$ K. SiO_2 ($k = 3.9$), ZnO ($k = 8.5$), Al_2O_3

($k = 9.8$), ZrO_2 ($k = 20$), and HfO_2 ($k = 25$) are five different common insulators that are compatible with the silicon in FET technology. The on-state current dependence of the on–off current ratio and transconductance are calculated in particular and the results are depicted in Fig. 6. Clearly seen, HfO_2 provides the best electrical parameters among the other proposed insulators and as expected, the increase of relative dielectric constant does not affect much the subthreshold swing and the delay time (the results are not shown here).[31] Utilization of low-k insulator as the gate oxide material diminishes the gate control over the electrostatic potential but on the other hand, employment of high-k dielectric material is beneficial for the gate insulator of 4-ASiNR as it can provide efficient charge injection from the source into the channel and reduce the off-state current. It is worth noting that for high-k insulators, C_{ox} can compete with the quantum capacitance results in better gate coupling over the channel, improved on–off current ratio, and g_m enhancement in 4-ASiNR FET.

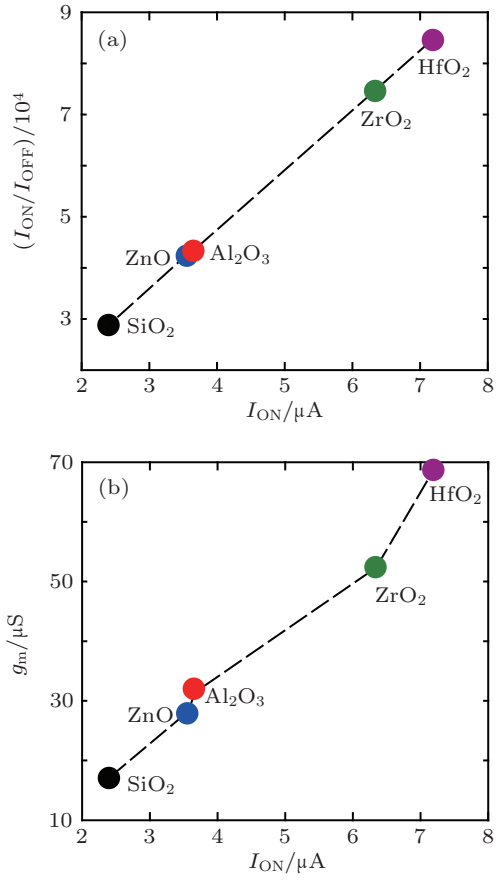


Fig. 6. (color online) (a) On–off current ratio and (b) transconductance of 4-ASiNR FET for various types of gate insulator materials versus the on-state current for $V_{DS} = 0.4$ V.

4. Optimized structure design analysis

As implied in Figs. 5 and 6, temperature, strain, and gate insulator thickness/material affect the operation of the device individually. Device performance has typically been improved by reducing the gate insulator thickness as well as the usage of high-k dielectric materials. Simulation results reveal that employment of HfO_2 as the gate insulator allows better coupling of the gate electrode to the channel and increases the inversion charge carrier density to enhance the drive current and switching speed of the ASiNR-FET. However, increasing both the temperature and strain magnitude improves the transconductance and intrinsic delay time but on the other hand degrades the on–off current ratio and subthreshold swing. It seems, therefore, that for attainment of an 4-ASiNR FET with efficient digital and analog applications, the best combination of strain magnitude and operating temperature should be obtained in the vicinity of a proper gate insulator thickness/material. As a result, the evaluation of four main electrical parameters for a wide range of strain magnitude and operating temperature with 1 nm of HfO_2 as the gate insulator seems helpful to develop constitutive optimized design able to yield high on–off current ratio, high transconductance, low intrinsic delay time and reduced value of subthreshold swing, simultaneously.

Here, we propose a novel variation matrix, $\mathrm{Var}(m,n)$, to gain insight into the effect of temperature and strain fluctuations on device performance. The objective of the variation matrix is to determine the region that provides the best combination of temperature and strain values that produces the desired balanced improvement of all the electrical parameters. First, we define the function $E_p(m,n)$ that denotes the effective contribution of the electrical parameters of 4-ASiNR FET to the variations of temperature and strain values. The two-parameter function is defined as follows:

$$E_p(m,n) = \pm \frac{f_p(m,n) - \phi_p}{\phi_p}, \tag{6}$$

where the variable p represents essential performance indicators including; $p = 1$: I_{ON}/I_{OFF}, $p = 2$: SS, $p = 3$: g_m, and $p = 4$: τ. Furthermore, we define variables m as the temperature range (150–350 K) and n as the strain range (0–5%). For the purpose of determining the susceptibility of each electrical parameter to design parameter fluctuations, we specify $f_p(m,n)$ as the related value of electrical parameter p and ϕ_p as the corresponding value of the initially proposed device in Fig. 4. The negative sign in Eq. (6), is used for subthreshold swing and intrinsic delay parameters. We also normalize $E_p(m,n)$ by its maximum value to equilibrate the identical influence of all the electrical parameters on device performance. Next, the two most significant electrical parameters for switching performance (i.e., I_{ON}/I_{OFF} and SS) of 4-ASiNR FET are included in group G_1 and related electrical parameters for analog applications (i.e., g_m and τ) are located in group G_2. Finally, we compute the variation matrix by the product of mean value of G_1 and G_2

$$G_{1(2)} = \left| \frac{E_{1(3)}(m,n) + E_{2(4)}(m,n)}{2} \right|, \tag{7}$$

$$\mathrm{Var}(m,n) = G_1 \times G_2. \quad (8)$$

The 2D variation matrix is sketched in Fig. 7(a) as a function of temperature and strain magnitude. The maximum value of the variation matrix occurs in the bottom-left and top-right corners, where the best improvement of relevant parameters of G_1 and G_2 groups, respectively, are obtained. As we progress from the corners to the central blue (color figure) region, the proposed combination of temperature and strain values provides relative average growth of the whole parameters. In other words, the central region does not exhibit the best performance metric of all the electrical parameters but retains the optimized conditions for the operation of 4-ASiNR FET. The found dependence of efficient device performance on design parameters qualitatively paves the way for appropriate design of experimental 4-ASiNR FET. To validate our approach, the normalized values of electrical parameters for the suggested device with design parameters extracted from the central equilibrium region of Fig. 7(a) and the initially proposed device in Fig. 4 are depicted as a histogram in Fig. 7(b). The suggested 4-ASiNR is simulated at $T = 250$ K under 3% of strain with 1 nm of HfO_2 as the gate insulator and as illustrated in Fig. 7(b), all the electrical parameters of the suggested optimized device have balanced improvement as compared to the proposed device.

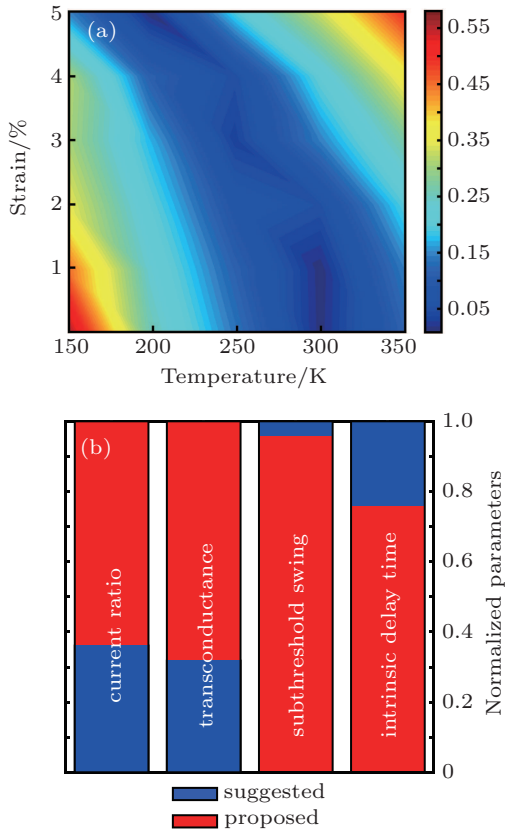


Fig. 7. (color online) (a) Temperature and strain dependence of 2D variation matrix. (b) Histogram for normalized value of electrical parameters for the optimized suggested (dark region) device and the primitive proposed (light region) 4-ASiNR FET, $V_{DS} = 0.4$ V.

5. Summary

We have investigated the behavior of a monolayer 4-ASiNR DG FET by performing 3D self-consistent quantum transport simulations to address design considerations for obtaining a device with improved electrical performance. The effects of temperature, uniaxial tensile strain, and gate oxide thickness/material on the main electrical parameters of the ASiNR FET have been theoretically studied. Our simulation results based on NEGF formalism demonstrate that as the ribbon temperature and the strain magnitude go up, the electrical parameters of the 4-ASiNR FET have a dramatic change. The performance benefits are achieved in terms of the transconductance and intrinsic delay time, but on the other hand an increase in the subthreshold swing and a major degradation in the on–off current ratio seem challenging. However, using a thin oxide layer and high-k insulators are helpful techniques for obtaining a superior gate control over the channel and improvement of device main electrical parameters, as a consequence. Eventually, the device efficiency in terms of entire electrical parameters is improved by optimizing the related design parameters. An optimization method has been developed which provides a valuable reference for the simultaneous impact of temperature and stain magnitude on the electrical characteristics of the 4-ASiNR FET. As emphasized in this work, proper combination of temperature and strain magnitude and employing HfO_2 as the gate insulator may lead to average improvement of all the electrical parameters. We hope that this work will facilitate the research aiming at the application of silicene-based FET in nanoelectronics.

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