Effects of back gate bias on radio-frequency performance in partially depleted silicon-on-inslator nMOSFETs

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The effects of back gate bias (BGEs) on radio-frequency (RF) performances in PD SOI nMOSFETs are presented in this paper. Floating body (FB) device, T-gate body-contact (TB) device, and tunnel diode body-contact (TDBC) device, of which the supply voltages are all 1.2 V, are compared under different back gate biases by different figures of merit, such as cut-off frequency ($f_{\rm T}$), maximum frequency of oscillation ($f_{\rm max}$), etc. Because of the lack of a back gate conducting channel, the drain conductance ($g_{\rm d}$) of TDBC transistor shows a smaller degradation than those of the others, and the trans-conductance ($g_{\rm m}$) of TDBC is almost independent of back gate bias. The values of $f_{\rm T}$ of TDBC are also kept nearly constant under different back gate biases. However, RF performances of FB and TB each show a significant degradation when the back gate bias is larger than $\sim$ 20 V. The results indicate that TDBC structures could effectively improve the back gate bias in RF performance.

Keywords: silicon-on-insulator (SOI), back gate bias, tunnel diode body contact, radio-frequency (RF)

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1. Introduction

Silicon-on-insulator (SOI) technology has been considered as a potential technology for high frequency application due to the high cut-off frequency, which has already reached to 500 GHz, and also for the harsh environment, such as high temperature and radiation environment.[1] Although SOI metal-oxide semiconductor field-effect transistors (MOSFETs) suffer floating body effect (FBE) caused by impact-ionization which restricts the application in analog integrated circuits, the body contacts with different structures are investigated to suppress FBE, such as T-gate (TB), H-gate, body-tied-source, etc. As we previously reported,[2] tunnel diode body-contact (TDBC) structures suppress the FBE successfully without adding additional parasitics compared with the conventional body-contact structures. TDBC structure could also achieve a similar cut-off frequency ($f_{\rm T}$) and even better maximum frequency of oscillation ($f_{\rm max}$) due to smaller parasitic gate–source capacitance.

In general, the effect of back gate bias (BGEs) of the N-type MOSFET in partially depleted (PD) SOI is very small and it is always ignored. However, it has been reported that with the decreasing of the buried oxide thickness (box), the penetration of electric field from the source/drain region into the body via the box decreases, thus enhancing the immunity to short channel effect (SCE),[3] and improving the heat dissipation ability.[4] However the characteristics become sensitive to the back gate bias ($V_{\rm BG}$) in PD SOI MOSFET, and the influences of $V_{\rm BG}$ on DIBL,[5] hysteresis effect,[6] and carrier mobility[7] have recently been investigated. In this paper, BGEs on RF performance in PD SOI nMOSFETs are investigated experimentally.

2. Devices and measurement

The RF performances of three different types of transistors of which supply voltages are all 1.2 V are investigated by applying various values of $V_{\rm BG}$, namely 1) floating body (FB), 2) T-gate body-contact (TB), and 3) tunnel diode body-contact (TDBC). All of the devices are fabricated by using the 0.13-μm PD SOI CMOS technology. The devices investigated in this paper have the same dimensions. The devices are designed with multi-fingers with the same gate length, 0.13 μm and total width, 40 μm. The finger width, finger number are 2 μm and 20 respectively. The gate oxide, top silicon, buried oxide thickness are 1.8 nm, 100 nm, and 145 nm. For each FB device and TDBC device, the gate is contacted from both sides to reduce the parasitic gate resistance. TB device is designed to contact from only one side due to design rule limiting, which could result in a higher value of gate resistance. The difference between FB and TDBC devices is that for the TDBC device one Esaki diode[8] is embedded in the source region to suppress the floating body effect. Fabrication procedure can be found in Ref. [9]. For the TB device, P+ implantation is performed to form the P+ body contact area. Poly in the body-contact side is designed to separate the P+ implantation area from source/drain area. The top view of FB and TB devices are shown in Figs. 1(a) and 1(b), and the cross-section view of TDBC is shown in Fig. 1(c).

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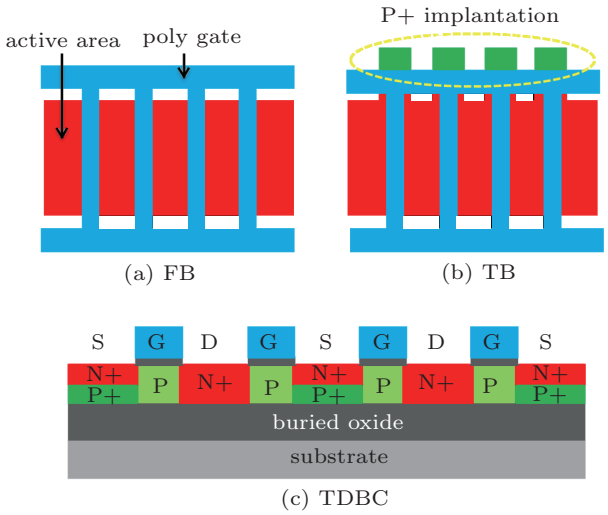


Fig. 1. (color online) (a) Top view of FB, (b) top view of TB devices, and (c) cross-section view of TDBC.

To investigate the BGEs on the RF performance, two-port S-parameters under different V_{BG} values are measured with frequency varying from 0.1 GHz to 30 GHz in steps of 100 MHz. The V_{BG} varies from -20 V to 50 V. Open and short de-embedding method is used to assess the practical performance of these devices. All of the measurements are made with an Agilent B1500 and Agilent PNA-X N5244A with a Cascade Summit 12000M probe station.

3. Results and discussion

The f_T and f_{max} are the key parameters for evaluating the RF performance of transistors.[10] The f_T is the frequency when the drain current gain is unity, and f_{max} is the frequency when the power gain is unity. The f_T could be extracted by the equation $f_0 \times |H_{21}|$ and f_{max} could be obtained from $f_0 \times \sqrt{MUG}$, where f_0 is the applied transport frequency, H_{21} is the current gain, and MUG is the Manson's unilateral power gain. For the physics background, f_T and f_{max} can be expressed as in the following equations:[11]

$$f_T = \frac{f_C}{\left(1+\frac{C_{gd}}{C_{gs}}\right)+(R_s+R_d)\left(\frac{C_{gd}}{C_{gs}}(g_m+g_d)+g_d\right)}, \quad (1)$$

$$f_{max} = \frac{f_C}{2\left(1+\frac{C_{gd}}{C_{gs}}\right)\sqrt{g_d(R_g+R_s)+\frac{1}{2}\frac{C_{gd}}{C_{gs}}\left(R_s g_m+\frac{C_{gd}}{C_{gs}}\right)}}, \quad (2)$$

where $f_C = g_m/2\pi C_{gs}$ represents the intrinsic cut-off frequency; g_d is the output conductance for DC case; g_m is the trans-conductance for low frequency; C_{gs} is gate-to-source capacitance; C_{gd} is gate-to-drain capacitance; and, R_g, R_s, R_d are gate resistance, source resistance, and drain resistance, respectively.

S-parameter under zero back gate bias is performed to extract the f_T and f_{max} when the back gate bias is zero. Figure 2 shows the variations of f_T and f_{max} with drain voltage at $V_G = 0.8$ V and $V_{BG} = 0$ V. From Fig. 2(a), f_T of TDBC reaches 85 GHz when drain voltage is 1.2 V, similar to that of FB, 87 GHz. The reason for f_T of TDBC lower than that FB is that the threshold voltage of TDBC is higher than that of FB device. The f_T of TB device is 74 GHz when $V_D = 1.2$ V, 13% lower than that of TDBC device due to the higher parasitic capacitance. Owing to the lower parasitic resistance and parasitic, f_{max} of TDBC could reach 150 GHz, $\sim$ 20% higher than that of FB, 125 GHz and $\sim$ 58% higher than that of TB, 95 GHz.

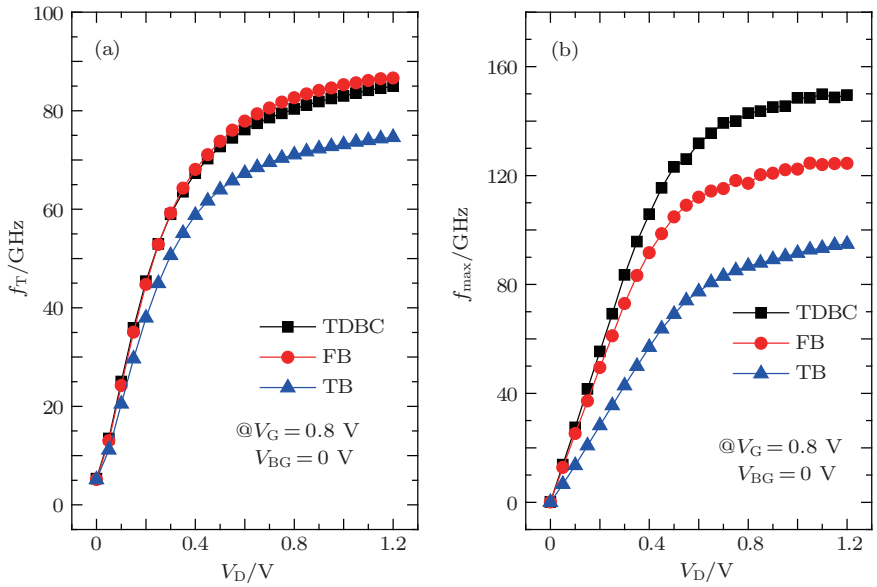


Fig. 2. (color online) Variations of cut-off frequency (f_T), maximum frequency of oscillation (f_{max}) with V_D when $V_G = 0.8$ V and $V_{BG} = 0$ V.

To perform the influence of back gate bias for different devices, S-parameters are measured under V_{BG} values ranging from -20 V to 50 V. The values of f_T and f_{max} are obtained to evaluate the BGEs of different devices. Figure 3 shows that f_T and f_{max} each behave as a function of V_{BG} when $V_G = 0.8$ V and $V_D = 1.2$ V. The negative back gate bias has little influence on f_T and always keeps a same value under zero back gate bias. While the f_T values of FB and TB each have a significant degradation when V_{BG} is larger than ~ 20 V. The reason for the degradation is that the transconductance (g_m) degrades when the inversion appears between silicon and buried oxide. Unlike the behaviors of FB and TB, the f_T value of TDBC slightly increases as V_{BG} rises. Figure 4 shows the influences of V_{BG} on g_m of the three devices. As V_{BG} increases, the g_m values of FB and TB devices reduce after $\sim$20 V, while the g_m value of TDBC slightly increases. When the V_{BG} is positive and large enough, the inversion layer forms and the gate faces increase difficulty in modulating the new deep lying electron conducting paths between source and drain in FB and TB devices.[12] However, due to the existence of a P+ region under the source, it is difficult to form a conducting channel between the source and the drain. As a result, the g_m values of TDBC devices almost remains the same.

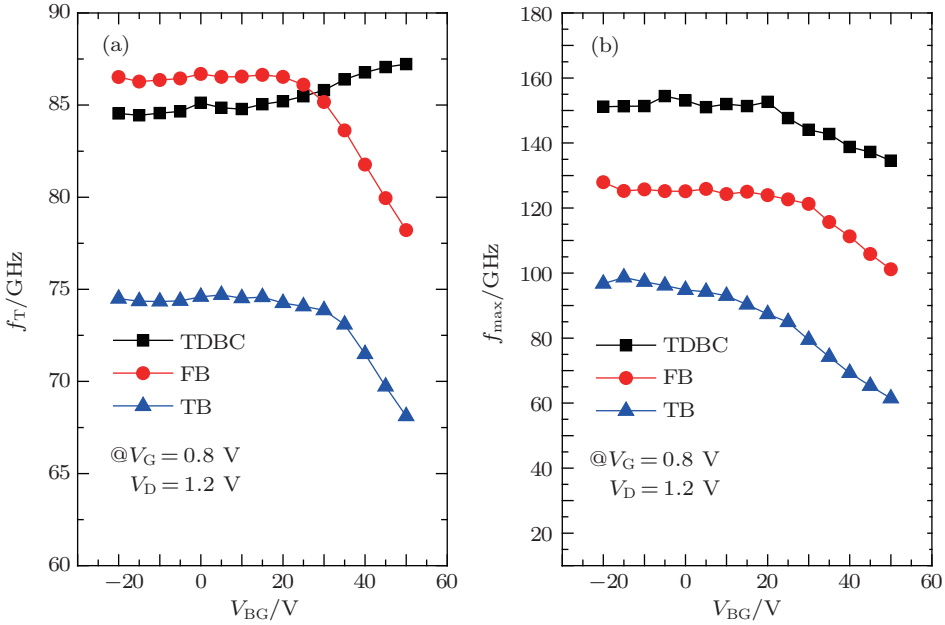


Fig. 3. (color online) Variations of (a) cut-off frequency (f_T), (b) maximum frequency of oscillation (f_{max}) extracted by the S-parameters with V_{BG} when $V_G = 0.8$ V and $V_D = 1.2$ V at a frequency of 10 GHz.

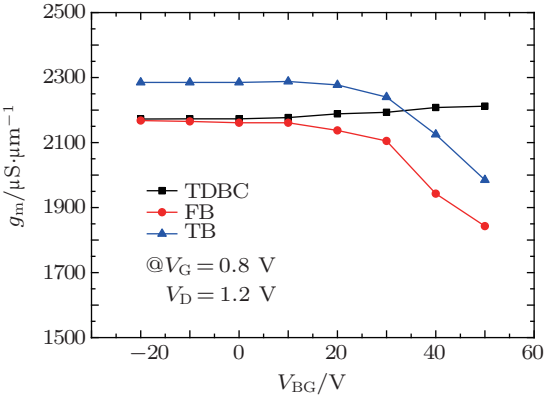


Fig. 4. (color online) Variations of transconductance (g_m) of FB and TB with back gate bias (V_{BG}) when $V_D = 1.2$ V and $V_G = 0.8$ V, while g_m value of TDBC slightly increases as V_{BG} rises.

It is demonstrated that the degradation for f_{max} of MOSFET is mainly related to the decrease of C_{gs}/C_{gd} ratio and the increase of g_d.[13] Figure 5 shows the comparison of the ratio of f_{max} to f_T among the three different devices when $V_G = 0.8$ V and $V_D = 1.2$ V. The f_{max}/f_T value of TDBC reaches 1.8 when back gate bias is zero, $\sim 25\%$ higher than that of FB device, 1.44 and $\sim 42\%$ higher than that of TB device, 1.27. However, the f_{max}/f_T ratio decreases when V_{BG} is positive. For FB and TB devices, the reason for reducing the ratio is the decreasing g_m and increasing g_d, as shown in Fig. 3 and Fig. 5. For the TDBC device, the g_m is almost constant as V_{BG} increases, and C_{gs} and C_{gd} are also independent of V_{BG}. As a result, the intrinsic cut-off frequency, f_C, almost has no dependence on V_{BG} for TDBC. The decreasing of the ratio for TDBC mainly happens because of the degradation of g_d and the slight increase of f_T.

The g_d is an important parameter for MOSFETs in microwave application because it has a significant effect on the f_{max}, as indicated in Eq. (2). Figure 6 shows the g_d values of TDBC, FB and TB devices with V_{BG} when frequency is 100 MHz where g_d can be extract by Re (Y_{22}). Due to the inversion layer between box and silicon, which could connect

the drain and source when V_{BG} is larger than ~ 20 V, the g_d degradation slopes of FB and TB devices are 10.5 μS/(μS·V) and 12 μS/(μS·V), respectively. However, due to the lack of a back gate channel, the g_d value of TDBC shows less degradation than those of FB and TB devices. The g_d degradation of TDBC is only 3.35 μS/(μS·V), 68% lower than that of FB device, and 72% lower than that of TB device. The results show that BGEs of TDBC is much smaller than those of FB and TB.

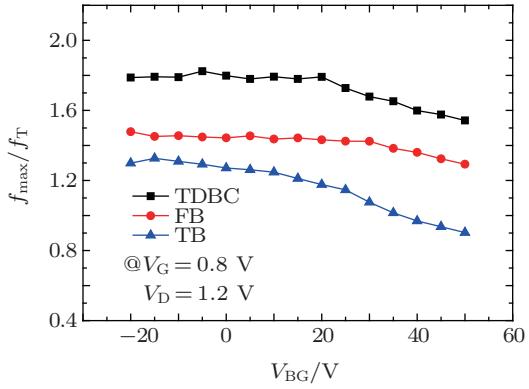


Fig. 5. (color online) Variations of f_{max}/f_T ratio of TDBC, FB and TB with V_{BG} when $V_g = 0.8$ V $V_d = 1.2$ V.

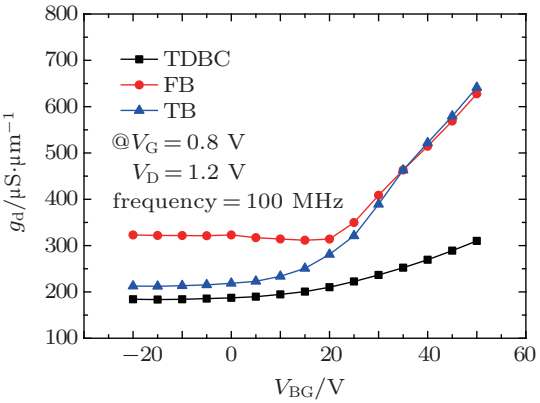


Fig. 6. (color online) Variations of g_d values of TDBC, FB and TB devices, extract by Re (Y_{22}), with V_{BG} when frequency is 100 MHz, $V_G = 0.8$ V and $V_D = 1.2$ V.

4. Conclusions

To investigate the influence of back gate bias on RF performance in PD SOI MOSFETs, different figures of merit are extracted under different back gate biases. The values of f_T and f_{max} of TDBC reported in this paper reach 75 GHz and 150 GHz, respectively. Back gate bias has a significant influence on RF performances in FB and TB devices while it has less effects on the RF performance of the TDBC device. The f_T value of TDBC shows scarcely the dependence on V_{BG} while the f_{max} value of TDBC shows a slight dependence on V_{BG} due to the degradation of g_d. The f_{max}/f_T ratios are also compared among the three types of devices, and the results show that the TDBC devices have a higher f_{max}/f_T ratio than the others. High positive back gate bias can cause the g_m values of FB and TB to decrease because of the emergence of strong inversion layer connecting the source and drain. The g_d degradation of TDBC caused by back gate bias is much lower than those of FB and TB devices because of the absence of a back gate conducting channel. The results indicate that TDBC structure could effectively improve the BGEs in PD SOI NMOSFETs.

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