Switching mechanism for TiO_2 memristor and quantitative analysis of exponential model parameters*

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The memristor, as the fourth basic circuit element, has drawn worldwide attention since its physical implementation was released by HP Labs in 2008. However, at the nano-scale, there are many difficulties for memristor physical realization. So a better understanding and analysis of a good model will help us to study the characteristics of a memristor. In this paper, we analyze a possible mechanism for the switching behavior of a memristor with a Pt/TiO_2/Pt structure, and explain the changes of electronic barrier at the interface of Pt/TiO_2. Then, a quantitative analysis about each parameter in the exponential model of memristor is conducted based on the calculation results. The analysis results are validated by simulation results. The efforts made in this paper will provide researchers with theoretical guidance on choosing appropriate values for $(\alpha, \beta, \chi, \gamma)$ in this exponential model.

Keywords: memristor, switching behavior, electronic barrier, exponential model

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1. Introduction

The memristor postulated in classical papers by Dr. Leon Chua in 1971[1] and 1976[2] as the fourth basic circuit element has spurred a great deal of research interest since its physical implementation was released by HP Labs in 2008.[3] Chua also proposed how to recognize a memristor from its electrical properties.[4,5] Nowadays, only a few groups can fabricate a memristor which satisfies these electrical properties, and most researchers still use mathematical models and physical theory to carry on their study by theoretical analysis and simulation.[6–10]

To date, a large number of mathematical models have appeared.[11–26] Many models are based on modeling equations proposed by HP Labs, which approximate the kinetic behavior of intrinsic dopants of the memristor in linear[3] and nonlinear manners.[11–13] In addition, advances in memristor modeling have been discussed, including a model incorporating an exponential ionic drift equation, which was used to model oxygen vacancy movement,[14] a model correlating more closely to physical characterization data,[15–17] a hyperbolic sine model,[15,18–22] approximating the metal–insulator–metal (MIM) tunnel junction,[23] a model using an ideal closed-loop operational amplifier,[24] a model based on a light-dependent resistor,[25] and the threshold flux-controlled memristor model.[26] However, these published models have failed to accurately describe the relationship between the model parameters and the mechanism of the switching behavior, which is meaningful for the future research of the memristor's application in various areas of electrical technology.

In this paper, we suggest a mechanism for switching behavior of Pt/TiO_2/Pt structure introduced in Ref. [27], and discuss the parameters of the exponential model proposed in Ref. [14]. Then, an in-depth understanding of the switching mechanism and exponential model is achieved. Additionally, based on the switching mechanism, we quantitatively analyze the effect of each parameter in the exponential model of the memristor's characteristics, which can provide a theoretical reference to researchers on how to choose the appropriate parameters in the exponential model.

The rest of this paper is organized as follows. Section 2 illustrates the mechanism for the switching behavior of TiO_2 memristor. In Section 3, we analyze the correlation between the parameters $(\alpha, \beta, \chi, \gamma)$ in the exponential model and the physical realization of memristors, and give the simulation results. Finally, our conclusions are drawn in Section 4.

2. Mechanism for the switching behavior of the memristor

The physical structure of memristor was released by HP Labs in 2008, as shown in Fig. 1, the upper layer is composed of stoichiometric titanium dioxide, which is an electrical insulator. In contrast, the bottom layer is doped with oxygen

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vacancies, which makes this layer a conductor.[3] Due to the difference of work function between metal and metal oxide, the Schottky barrier is formed at the interface between metal and insulator. In the bottom layer, the high concentration of oxygen vacancies serves to collapse the Schottky barrier, and the Ohmic contact is produced at the interface of Pt/TiO_{2-x}. In the upper layer, the low concentration of oxygen vacancies maintains the Schottky barrier at the interface of Pt/TiO_2.

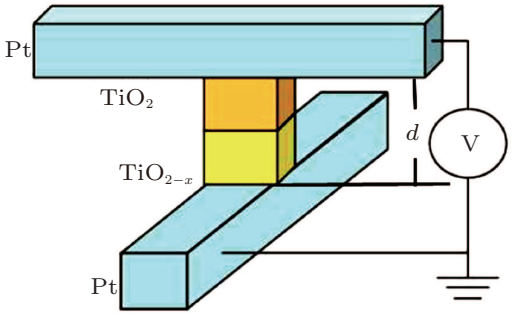


Fig. 1. (color online) The structure of Pt/TiO_2/Pt memristor.[27]

With an external electrical field, the positively charged vacancies drift in the given direction. The positive voltage can make the vacancies drift to TiO_2 layer, then the Schottky barrier at the interface of Pt/TiO_2 becomes an Ohmic contact and the memristor is switched to the ON state. When a negative voltage is applied to memristor, the vacancies in the conducting channel are repelled away from TiO_2 layer and the original Schottky barrier is regained and the memristor is switched to the OFF state. This is suggested to be an example of bipolar switching, in which the ON and OFF states are switched with opposite bias polarity. This switching mechanism is inspired by valence-change, as illustrated in Ref. [28].

2.1. ON switch process of the memristor

When a voltage is applied to the top electrode in Fig. 1, the positively charged vacancies in the oxide drift to the undoped TiO_2 layer and result in an increase in the doping concentration of the TiO_2 layer, which in turn makes the Schottky barrier width at the interface of Pt/TiO_2 narrow. Based on the principle of quantum tunnelling,[19] when the barrier is as thin as the De Borglie wave length of electron (now the barrier is quantum barrier, the electron can tunnel through the barrier by electron wave property), the electron can tunnel through the barrier easily in the channels formed by the drift of oxygen vacancies and then the device is switched ON.

Supposing that the Schottky barrier is formed by a barrier of height Φ_B and half width a. The barrier height Φ_B is the difference between metal work function W_m and semiconductor electron affinity q_χ [29,30]

$$\Phi_B = W_m - q_\chi. \tag{1}$$

The electron affinity q_χ is measured from the bottom of conduction band E_c to the vacuum level

$$q_\chi = W_s + E_F - E_c, \tag{2}$$

where W_s is the work function of semiconductor, E_F is the Fermi energy level of semiconductor, and E_c is the bottom of conduction band level. So the barrier height Φ_B can be given by

$$\Phi_B = W_m - W_s + E_c - E_F. \tag{3}$$

And the barrier height of semiconductor is

$$\Phi_s = W_m - W_s. \tag{4}$$

The barrier height is associated with the material, the relationship between the barrier height Φ_B and the barrier width X_D is

$$X_D = \sqrt{\frac{2\varepsilon_0\varepsilon_r\Phi_B}{qN_D}}, \tag{5}$$

where q is electronic charge ($q = 1.6\times10^{-19}$ C), ε_0 is the permittivity of vacuum, ε_r is the relative dielectric constant of TiO_2, N_D is the concentration of vacancies in semiconductor. Without the external bias voltage, the probability of an electron jumping the barrier is

$$P = v\exp\left(-\frac{\Phi_B}{k_0T}\right), \tag{6}$$

where v is the probability of electron transition without the barrier, k_0 is Boltzmann constant, and T is temperature.

With the external field, electrons drifting from semiconductor to metal will be aided, while it will be opposed from metal to semiconductor. This effect is equal to replacing the effective barrier by $\Phi_B - aqV/d$ coincided with the direction of the external field, and $\Phi_B + aqV/d$ opposite to the direction of the external field[14,31] when the thickness of oxide layer is d. Therefore, the probability of an electron jumping the barrier can be concluded as

$$\begin{aligned} P &= v\exp\left(-\frac{\Phi_B}{k_0T}\right)\left[\exp\left(\frac{aq}{k_0Td}V\right) - \exp\left(-\frac{aq}{k_0Td}V\right)\right] \\ &= 2v\exp\left(-\frac{\Phi_B}{k_0T}\right)\sinh\left(\frac{aq}{k_0Td}V\right). \end{aligned} \tag{7}$$

Consequently, when n electrons are available to carry the current, the number N electrons which can jump the barrier can be obtained by $N = nP$. So the tunneling current from semiconductor to metal can be given by multiplying electronic charge q by N

$$I_1 = Nq = nPq = 2nqv\exp\left(-\frac{\Phi_B}{k_0T}\right)\sinh\left(\frac{aq}{k_0Td}V\right). \tag{8}$$

2.2. OFF switch process of the memristor

When a voltage V is applied to the top electrode, the vacancies in the conducting channel are repelled away from the top interface and the original Schottky barrier is regained. Based on the thermionic emission theory,[32] just like how electrons in metal pass through the potential energy barrier into semiconductor, the electrons in the semiconductor can penetrate into the metal layer as long as they have sufficient energies to overcome the potential barrier. We can calculate the current from semiconductor to metal by multiplying the number of electrons per unit volume which can hop the barrier by electronic charge q. The velocity of electrons is resolved into its three components v_x,v_y,v_z, with the x-axis parallelling to the transport direction, namely from semiconductor to metal. The number of electrons in per unit volume is

$$\begin{aligned} \mathrm{d}n' &= n_0 \left(\frac{m_n^*}{2\pi k_0 T}\right)^{3/2} \exp\left[-\frac{m_n^*(v_x^2+v_y^2+v_z^2)}{2k_0T}\right] \\ &\quad \times \mathrm{d}v_x \mathrm{d}v_y \mathrm{d}v_z, \end{aligned} \tag{9}$$

where n_0 is concentration of electrons in the conduction band in thermal equilibrium

$$n_0 = 2\frac{(2\pi m_n^* k_0 T)^{3/2}}{h^3} \exp\left(-\frac{E_\mathrm{c}-E_\mathrm{F}}{k_0T}\right). \tag{10}$$

In per unit electrode area, when the volume is equal to v_x, the number of electrons which can arrive at the interface between metal and semiconductor in per unit time is

$$\begin{aligned} \mathrm{d}N &= n_0 \left(\frac{m_n^*}{2\pi k_0 T}\right)^{3/2} \exp\left[-\frac{m_n^*(v_x^2+v_y^2+v_z^2)}{2k_0T}\right] \\ &\quad \times v_x \mathrm{d}v_x \mathrm{d}v_y \mathrm{d}v_z, \end{aligned} \tag{11}$$

where m_n^* is the effective mass of electron, h is the Planck constant. When the potential of semiconductor is $V_{\mathrm{s}0}$, $\Phi_\mathrm{s} = -qV_{\mathrm{s}0}$. From Eqs. (3) and (4), the barrier height of metal Φ_B is

$$\Phi_\mathrm{B} = E_\mathrm{c} - E_\mathrm{F} - qV_{\mathrm{s}0}. \tag{12}$$

If $V_{\mathrm{s}0}+V<0$, the electrons which can penetrate the barrier must satisfy the following condition:

$$\frac{1}{2}m_n^* v_x^2 \geq -q(V_{\mathrm{s}0}+V). \tag{13}$$

The minimum velocity required in the x-direction is v_{x0}

$$v_{x0} = \left[\frac{-2q(V_{\mathrm{s}0}+V)}{m_n^*}\right]^{1/2}. \tag{14}$$

Because there is no exist barrier in the y-direction and in the z-direction, neither of the velocities in these two directions are limited. Current can be obtained by multiplying electron number N by electron charge q, so the current density formed by the electrons from semiconductor to metal is

$$\begin{aligned} J_{2a} &= qn_0 \left(\frac{m_n^*}{2\pi k_0 T}\right)^{3/2} \int_{-\infty}^{\infty} \mathrm{d}v_z \int_{-\infty}^{\infty} \mathrm{d}v_y \\ &\quad \times \int_{v_{x0}}^{\infty} \exp\left[-\frac{m_n^*(v_x^2+v_y^2+v_z^2)}{2k_0T}\right] v_x \mathrm{d}v_x \\ &= qn_0 \left(\frac{m_n^*}{2\pi k_0 T}\right)^{3/2} \frac{2\pi k_0 T}{m_n^*} \frac{k_0 T}{m_n^*} \\ &\quad \times \exp\left(-\frac{m_n^* v_{x0}^2}{2k_0T}\right). \end{aligned} \tag{15}$$

By substituting Eqs. (10), (12), (14) into Eq. (15), we get

$$\begin{aligned} J_{2a} &= \frac{4\pi q m_n^* k_0^2}{h^3} T^2 \exp\left(-\frac{E_\mathrm{c}-E_\mathrm{F}}{k_0T}\right) \exp\left[\frac{qV_{\mathrm{s}0}+qV}{k_0T}\right] \\ &= A^* T^2 \exp\left(-\frac{\Phi_\mathrm{B}}{k_0T}\right) \exp\left(\frac{qV}{k_0T}\right), \end{aligned} \tag{16}$$

and

$$A^* = \frac{4\pi q m_n^* k_0^2}{h^3}. \tag{17}$$

A^* is the effective Richardson constant for thermionic emission.[33]

The electrons in the metal are distributed in less than 0.1-nm film, while the thickness of the space charge layer (the electrons at the semiconductor surface) in a semiconductor is usually at the micron level. Therefore, the potential change caused by external voltage mainly concentrates in the semiconductor. The barrier height from metal into semiconductor remains the same. Therefore, the current density J_{2b} formed by the electrons from metal to semiconductor remains constant, which equals to the current flowing from the semiconductor into the metal when thermal equilibrium prevails; i.e., when $V=0$. This corresponding current density is obtained from Eq. (16) by setting $V=0$,

$$J_{2b} = -A^* T^2 \exp\left(-\frac{\Phi_\mathrm{B}}{k_0T}\right). \tag{18}$$

Supposing the area of electrode is S, so the total current is given by

$$\begin{aligned} I_2 &= S \times (J_{2a}+J_{2b}) \\ &= SA^* T^2 \exp\left(-\frac{\Phi_\mathrm{B}}{k_0T}\right)\left[\exp\left(\frac{qV}{k_0T}\right)-1\right]. \end{aligned} \tag{19}$$

The tunneling current and the thermionic emission current exist simultaneously. It is important which one is at the leading position. So the current through the memristor is the sum of tunneling current and thermionic emission current:

$$\begin{aligned} I &= I_1 + I_2 \\ &= 2nqv \exp\left(-\frac{\Phi_\mathrm{B}}{k_0T}\right) \sinh\left(\frac{aq}{k_0Td}V\right) \\ &\quad + SA^* T^2 \exp\left(-\frac{\Phi_\mathrm{B}}{k_0T}\right)\left[\exp\left(\frac{qV}{k_0T}\right)-1\right]. \end{aligned} \tag{20}$$

3. Qualitative analysis of parameters in memristor modeling

Yang *et al.*[27] used the following model to describe the *I*–*V* switching characteristics of the memristor. This model can reproduce the *I*–*V* characteristics and has been widely used to model the physical structure of memristor

$$I = \omega^n \beta \sinh(\alpha V) + \chi(\exp(\gamma V) - 1), \tag{21}$$

where ω is the state variable of memristor, and is normalized to $[0,1]$. When the memristor is in the ON state, ω is close to 1 and ω^n is close to 1, the current is dominated by the first term in Eq. (21). When the memristor is in the OFF state, ω is close to 0 and ω^n is close to 0, the current is dominated by the second term in Eq. (21). The exponent n determines the effect of ω on the *I*–*V* curve. For the simplicity, the parameters $(\alpha, \beta, \chi, \gamma)$ are mainly discussed in this paper.

Remark 1 Yang *et al.*[27] suggested that the parameters $(\alpha, \beta, \chi, \gamma)$ were fitting constants, dimensionless, and depended on physical properties of the material of memristor. Next, the model equation (21) is compared with theoretical derivation expression (20). A quantitative analysis about the parameters $(\alpha, \beta, \chi, \gamma)$ effect on the *I*–*V* characteristic of memristor is conducted from a physical point of view.

In this section, we use the model (21) and establish the HSPICE code to analyze qualitatively each parameter's effect on the properties of the memristor and discuss the reasons causing the phenomenon. We call the part with big current values "low resistance" ($R_{\rm low}$) and that with small current values "high resistance" ($R_{\rm high}$). On the condition that the input signal is ideal sinusoidal signal with the frequency 1 kHz and the amplitude 1 V, the *I*–*V* characteristic curves of memristor become a twisted hysteresis. The high resistance $R_{\rm high}$ and the low resistance $R_{\rm low}$ are measured with a voltage 0.7 V. At the same time, the *I*–*V* characteristics of the memristor are also discussed with applied voltage of different frequency.

3.1. Qualitative analysis of parameter α's influence on memristor

The first term in Eq. (21) represents the tunneling current produced by the electrons tunneling through barrier when the memristor is in ON state. From Eq. (8), the parameter α is

$$\alpha = \frac{aq}{k_0 T d}. \tag{22}$$

Given the material of memristor, the parameter α is only associated with the half width of barrier a. According to Eq. (5), the parameter α is proportional to $\sqrt{1/N_{\rm D}}$ with $\Phi_{\rm B}$ constant. When the concentration of oxygen vacancies $N_{\rm D}$ decreases, the barrier width $X_{\rm D}$ and half barrier width a increase from Eq. (5). At the same time, the increasing a results in the decreasing barrier height $\Phi_{\rm B} - aqV/d$ and increasing barrier height $\Phi_{\rm B} + aqV/d$. According to Eq. (7), the probability of the electrons through the barrier P increases with the barrier height decreasing. Hence, the number of electrons tunneling through the barrier raises at the electric field direction and reduces at the opposite direction, which together lead to the increasing forward current. Therefore, when the parameter α increases (due to the above-mentioned decrease in the oxygen vacancy concentration $N_{\rm D}$ and consequent increase in half barrier width a), the current increases. The above analysis can be validated by the following simulation results.

Figure 2 shows the I/V characteristic when parameter α takes different values (i.e., 2, 2.5, 3, 3.5). When $\alpha = 2$, the maximum positive current and negative current are 215 nA and -210 nA, respectively. When $\alpha = 3.5$, the maximum positive current and negative current are 1085 nA and -850 nA, respectively. With the increase of α, the conductivity of memristor increases.

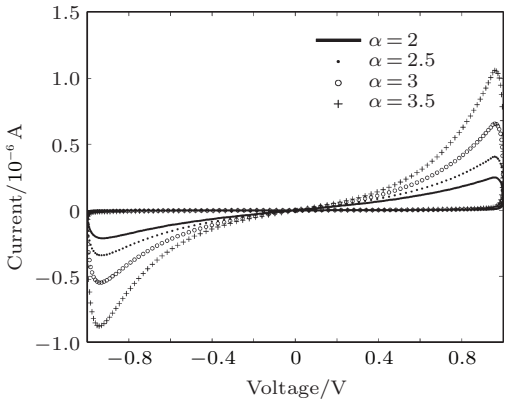


Fig. 2. The I/V characteristics for different parameter α.

If the frequency of the applied voltage is changed, such as $f = 500$ Hz, 2 kHz, 5 kHz, 10 kHz, as α increases, both of the high and low resistances of the memristor decrease, as shown in Table 1; namely, the conductivity of memristor increases.

Table 1. High and low resistances under different frequency input voltage signals and different α (the unit of the resisitance is in MΩ).

	$f = 500$ Hz		$f = 2$ kHz		$f = 5$ kHz		$f = 10$ kHz	
	$R_{\rm high}$	$R_{\rm low}$	$R_{\rm high}$	$R_{\rm low}$	$R_{\rm high}$	$R_{\rm low}$	$R_{\rm high}$	$R_{\rm low}$
$\alpha = 2$	209.9	4.8	209.9	13.72	207.7	124.1	198.6	176.9
$\alpha = 2.5$	167.4	3.3	167.9	9.46	166.3	92.8	158.8	138.8
$\alpha = 3$	130.8	2.29	131.3	6.64	129.9	68.6	123.4	106.1
$\alpha = 3.5$	100.3	1.6	100.6	4.65	99.3	50.4	93.6	79.3

3.2. Qualitative analysis of parameter β's influence on the memristor

Comparing the first term in Eq. (21) with Eq. (8), the parameter β is given by

$$\beta = 2nqv \exp\left(-\frac{\Phi_{\rm B}}{k_0 T}\right), \tag{23}$$

the parameter β is determined by Φ_B (the barrier height) and v (the transition probability without barrier). The barrier height Φ_B does not change when the material remains the same. So the parameter β is proportional to v. Given the same number of electrons, a large value of v indicates that more electrons likely penetrate the barrier to generate the current. Therefore, a larger value v will give a larger current.

Figure 3 shows the simulation results. When β is 5, 7, 9, and 11, the corresponding maximum positive current is 113.4 nA, 187.2 nA, 236.5 nA, and 316.9 nA. Then the conductivity of memristor increases.

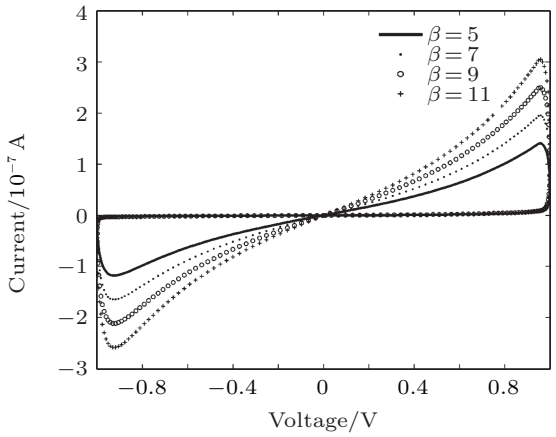


Fig. 3. The I/V characteristics for different parameter β.

As shown in Table 2, if the frequency of the applied voltage is changed, as β increases, both of the high and low resistances of the memristor decrease; namely, the conductivity of memristor increases.

Table 2. High and low resistances under different frequency input voltage signals and different β (the unit of the resisitance is in MΩ).

	$f = 500$ Hz		$f = 2$ kHz		$f = 5$ kHz		$f = 10$ kHz	
	R_{high}	R_{low}	R_{high}	R_{low}	R_{high}	R_{low}	R_{high}	R_{low}
$\beta = 5$	275.6	8.6	274.5	24.05	272.4	183.2	257.3	236.5
$\beta = 7$	238.1	6.19	237.3	17.5	235.7	148	223.6	202.3
$\beta = 9$	209.9	4.8	209.9	13.72	207.7	124.1	198.6	176.9
$\beta = 11$	186.7	3.15	186.7	11.3	185.7	106.9	177.2	156.6

3.3. Qualitative analysis of parameter χ's influence on the memristor

The second term of Eq. (21) represents the thermionic current when memristor is switched OFF. The parameter χ is obtained from Eq. (19)

$$\chi = SA^*T^2 \exp\left(-\frac{\Phi_B}{k_0 T}\right). \tag{24}$$

Parameter χ is determined by both electrode's area S and temperature T, and is independent of the bias voltage. When the electrode's area S remains unchanged, the thermionic emission current through memristor changes exponentially with temperature T. Based on the thermionic emission theory, higher temperature results in the higher electrons' kinetic energy, which allows more electrons satisfy Eq. (13). As a result, the current flowing through the memristor becomes larger.

Where the temperature is unchanged, χ is proportional to the area of electrode. Recalling the analysis of the OFF switching process above, the current density through memristor is calculated by summing up the total number of electrons penetrating the barrier in unit area per unit time. Then, the current is the product of the current density and electrode's area. So the number of electrons tunneling through barrier increases with the increased electrode area S, causing the current through memristor to increase.

Figure 4 shows the I–V curves when χ is 0.01, 0.1, 0.5, and 1, respectively. When χ is changed from 0.01 to 0.1, only minimal change is observed in the I–V characteristics. However, when χ is adjusted from 0.5 to 1, the current increases significantly from 458 nA to 722 nA. When $\chi = 1$, the high resistance part approaches the low resistance part. This happens because as the temperature T goes up, the electron emission speeds up dramatically. Then, a steep increase of current through the memristor can be observed.

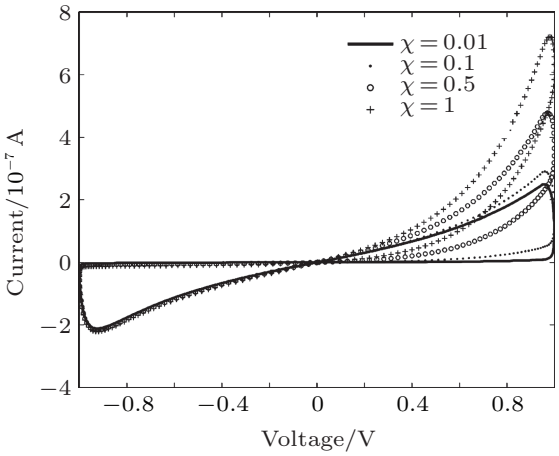


Fig. 4. The I/V characteristics of different parameter χ.

As shown in Table 3, with applied voltage of different frequency, as χ increases, both of the high and low resistances of the memristor decrease, then the current increases, which is the same as the analysis above.

Table 3. High and low resistances under different frequency input voltage signals and different χ (the unit of the resisitance is in MΩ).

	$f = 500$ Hz		$f = 2$ kHz		$f = 5$ kHz		$f = 10$ kHz	
	R_{high}	R_{low}	R_{high}	R_{low}	R_{high}	R_{low}	R_{high}	R_{low}
$\chi = 0.01$	209.9	4.8	209.9	13.72	207.7	124.1	198.6	176.9
$\chi = 0.1$	40.7	4.4	40.46	10.77	40.2	35.7	36.45	36.25
$\chi = 0.5$	8.87	3.16	36.65	5.51	8.5	7.9	8.12	8.09
$\chi = 1$	4.48	2.34	4.48	3.43	4.4	3.95	4.06	4.05

3.4. Qualitative analysis of parameter γ's influence on the memristor

The doping concentration of the memristor discussed in Section 2 is 0.5%. With the external field applied, the oxygen vacancies transfer to the Pt/TiO_{2-x} interface, which makes the oxygen vacancies concentration at the interface of the Pt/TiO_2 decrease. So it is pure TiO_2. γ can be given by comparing Eqs. (21) and (19) which is mainly used to present the relationship between the current through the memristor and the external voltage V

$$\gamma = \frac{q}{k_0 T}. \tag{25}$$

The parameter γ is inversely related to temperature T. So this part will mainly discuss the influence of temperature T on the conductivity under the condition of low oxygen vacancy concentration. Based on the theory of the semiconductor's conductivity, the drift mobility is determined by the lattice scattering under the circumstance of the low oxygen vacancy concentration. As temperature T increases, the scattering probability becomes bigger, finally it makes drift mobility decrease. Owing to the reverse relationship between the resistivity and electron drift mobility, the resistivity of memristor becomes big as the drift mobility decreases. Eventually, it makes the current through memristor become small. In other words, the reduction in γ (due to the above mentioned increase in temperature T) causes the current through the memristor to decrease.

The I–V characteristics of memristor are shown in Fig. 5 when γ is set to 4, 6, 7, and 8. The change of parameter γ has a little influence on the memristor when $\gamma = 4, 6$. When $\gamma = 7, 8$, the current dramatically increases from 316 nA to 487 nA. We can observe that the high resistance part comes closely to the low resistance part when $\gamma = 8$. According to the theory of quantum tunneling, when the temperature T falls low enough, the tunneling current becomes dominant, which causes the high resistance close to the low resistance.

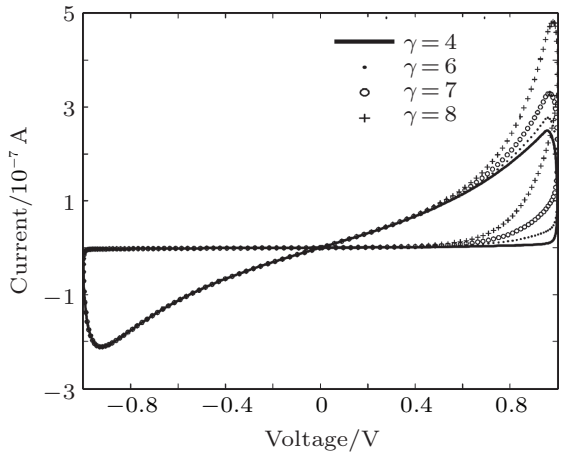


Fig. 5. The I/V characteristics of different parameter γ.

In Table 4, with different frequency applied voltage, as γ increases, both of the high and low resistances of the memristor decrease, and then the current increases, which is the same as the analysis above.

Table 4. High and low resistances under different frequency input voltage signals and different γ (the unit of the resisitance is in MΩ).

	$f = 500$ Hz		$f = 2$ kHz		$f = 5$ kHz		$f = 10$ kHz	
	R_{high}	R_{low}	R_{high}	R_{low}	R_{high}	R_{low}	R_{high}	R_{low}
$\gamma = 4$	209.9	4.8	209.9	13.72	207.7	124.1	198.6	176.9
$\gamma = 6$	83.73	4.67	83.3	12.46	81.9	65.4	68.63	67.85
$\gamma = 7$	46.4	4.46	46.05	11.11	44.9	40.01	36.1	35.8
$\gamma = 8$	24.4	4.09	24.14	8.89	23.3	22.95	17.6	17.3

Remark 2 As illustrated in Subsection 2.2, when a negative voltage is applied to the memristor, the thermionic emission current generated by switch-OFF process is at the leading position. When the external negative voltage is applied to the top Pt electrode, the barrier height at the semiconductor increases. The number of electrons flowing from semiconductor to metal decreases, and then the electrons flowing from metal to semiconductor play the dominant role. Because the barrier height at the metal is relatively large, it is difficult for electrons in the metal to surmount. Then the number of electrons flowing from metal to semiconductor is very small. Namely, the current from semiconductor to metal is very small. Also, the barrier at the metal remains unchanged when the external voltage changes, so the current from semiconductor to metal is constant. Therefore, the external voltage has no effect on the current when a negative voltage is applied to memristor. Because the parameters χ and γ present the voltage's effect on the current of memristor when the memristor is switched OFF, the changes in parameters χ and γ have no effect on the negative part of the I–V curve.

4. Conclusions

In this paper, the mechanism for the switching behavior of the memristor has been elaborated, which includes the quantum tunnel effect when the memristor is switched to the ON state, and Schottky thermionic-emission theory when the memristor is switched to the OFF state. Based on the mechanism and the exponential ionic drift equation, the relationships between each parameter in exponential model and the switching mechanism are analyzed at great length. The changes in the physical parameters of the switching process bring about the variations in the parameter α, β, χ,γ of the exponential model. When these parameters become bigger, the current through memristor increases, which is validated by the simulation results on HSPICE. It is believed that the analysis of the parameter α, β, χ,γ may be useful for the choice of the parameters' proper values, which is meaningful for future research.

References

[1] Chua L O 1971 *IEEE Trans. Circuit Theory* **18** 507
[2] Chua L O and Kang S M 1976 *Proc. IEEE* **64** 209
[3] Strukov D B, Snider G S, Stewart G R and Williams R S 2008 *Nature* **453** 80
[4] Adhikari S P, Sah M P, Kim H and Chua L O 2013 *IEEE Trans. Circ. Syst. I* **60** 3008
[5] Chua L O 2012 *Proc. IEEE* **100** 1920
[6] Merrikh-Bayat F and Shouraki S B 2013 *IEEE Trans. Cybern.* **43** 269
[7] Zhou J and Huang D 2012 *Chin. Phys. B* **21** 048401
[8] Tian X B, Xu H and Li Q J 2013 *Chin. Phys. B* **22** 088502
[9] Tian X B and Xu H 2014 *Chin. Phys. B* **23** 068401
[10] Bao B C, Hu F W, Liu Z and Xu J P 2014 *Chin. Phys. B* **23** 070503
[11] Biolek Z, Biolek D and Biokova V 2009 *Radioengineering* **18** 211
[12] Joglekar Y N and Wolf S J 2009 *Eur. J. Phys.* **30** 661
[13] Benderli S 2009 *Electron. Lett.* **45** 377
[14] Strukov D B and Williams R S 2009 *Appl. Phys.* **94** 515
[15] Yakopcic C, Taha T M, Subramanyam G, Pino R E and Rogers S 2011 *IEEE Electron Dev. Lett.* **32** 1436
[16] Pino R E, Bohl J W, McDonald N, Wysocki B, Rozwood P, Campbell K A, Oblea A and Timisina A 2010 *Proc. IEEE/ACM Int. Symp. Nanoscale Archit.*, June 17–18, 2010, Anaheim, CA, USA, p. 1
[17] Abdalla H and Pickett M D 2011 *IEEE Int. Symp. Circ. Syst.*, May 15–18, 2011, Rio de Janeiro, p. 1832
[18] Laiho M, Lehtonen E, Russell A and Dudek P 2010 *Neuromorphic Eng.* **10** 24
[19] Wu G Y and Wu K P 1992 *J. Appl. Phys.* **71** 1259
[20] Lehtonen E and Laiho M 2010 *12th International Workshop on Cellular Nanoscale Networks and Their Applications*, February 3–5, 2010, Berkeley, CA, USA, p. 1
[21] Chang T, Jo S H, Kim K H, Sheridan P, Gaba S and Lu W 2012 *Appl. Phys.* **102** 857
[22] Zhu X, Tang Y H, Wu C Q, Wu J J and Yi X 2014 *Chin. Phys. B* **23** 028501
[23] Simmons J G 1963 *J. Appl. Phys.* **34** 1793
[24] Xu K D, Zhang Y H, Wang L, Yuan M Q, Joines W T and Liu Q H 2013 *Proc. SPIE* **8911** 89110H
[25] Wang X Y, Andrew L F, Herbert H C I, Victor S and Qi W G 2012 *Chin. Phys. B* **21** 108501
[26] Wu H G, Bao B C and Chen M 2014 *Chin. Phys. B* **23** 118401
[27] Yang J J, Pickett M D, Li X, Ohlberg D A, Stewart D R and Williams R S 2008 *Nat. Nanotechnol.* **3** 429
[28] Kwon D H, Kim K M, Jang J H, Jeon J M, Lee M H, Kim G H, Li X S, Park G S, Lee B, Han S W, Kim M Y and Hwang C S 2010 *Nat. Nanotechnol.* **5** 148
[29] John B 1947 *Phys. Rev.* **71** 717
[30] Doghish M Y and Ho F D 1992 *IEEE Trans. Electron Dev.* **39** 2771
[31] Charlesby A 1953 *Proc. Phys. Soc. B* **66** 533
[32] Sze S M and Ng K K 2007 *Physics of Semiconductor Devices* (New Jersey: John Wiley & Sons Inc.) pp. 134–187
[33] Ohdomari I and Tu K N 1980 *J. Appl. Phys.* **51** 3735