Hetero-epitaxy of $L_g = 0.13$-μm metamorphic AlInAs/GaInAs HEMT on Si substrates by MOCVD for logic applications*

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In this work, a hetero-epitaxial $Al_{0.49}In_{0.51}As/Ga_{0.47}In_{0.53}As$ metamorphic high electron mobility transistor (mHEMT) grown by metal–organic chemical vapor deposition (MOCVD) on p-type silicon substrate has been successfully demonstrated. A novel AlGaAs/AlAs period multiple quantum well (MQW) composite buffer scheme is developed to effectively tune the leakage current from the buffer layer. The quantized room-temperature Hall mobility of the two-dimensional electron gas (2DEG) is larger than 7800 $cm^2/V{\cdot}s$, with an average sheet carrier density of 4.6×10^{12} cm^{-2}. Two-stage electron beam (EB) lithography technology by a JBX-6300 e-beam lithography system is developed to realize a 0.13-μm mHEMT device on Si substrate. A maximum transconductance G_m of up to 854 mS/mm is achieved, and is comparable to that of mHEMT technology on GaAs substrate with the same dimension. The f_T and f_{max} are 135 GHz and 120 GHz, respectively.

Keywords: AlInAs/GaInAs, silicon, metamorphic high electron mobility transistor (mHEMT), metal-organic chemical vapor deposition (MOCVD), multiple quantum well (MQW)

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1. Introduction

As Si-based complementary metal–oxide semiconductor (CMOS) scaling is approaching to the limit of Moore's Law, the urgency to explore a new alternative to the conventional Si devices is increasing. Over the past decade, III–V materials have received active and continuous attention as channel alternatives for an n-field effect transistor (n-FET) in future CMOS technology. GaInAs as a channel material closely matches InP, and has shown tremendous potential due to its high electron mobility and low power operations.[1] Recently, AlInAs/GaInAs high electron mobility transistor (HEMT) on Si substrate, which effectively takes advantage of the high carrier drift velocity of GaInAs channel HEMT and the large wafer size and mechanical strength of Si substrate, has been expected to be the most promising device for high-speed and low-power digital logic applications.[2,3] A seamless, robust heterogeneous integration of high-performance GaInAs mHEMT on Si substrate will enable low-voltage, high-speed III–V-based logic circuit blocks to be combined with the main stream Si CMOS technologies for microprocessor applications in the foreseeable future. To combine the superior carrier transport properties of III–V compounds with Si technologies, one straightforward wafer-level solution directly heteroepitaxially deposits good-quality III–V materials on silicon substrates for device applications. Several different technologies are used in most of the recent studies, such as MBE and MOCVD, to develop AlInAs/GaInAs mHEMTs on the same epi-wafer. However, they still have major technological challenges to be overcome, including the high-density threading dislocation defects in the epi-layers resulting from the large lattice mismatch and the differences in the thermal expansion coefficient between the Si and grown III–V compounds.[4–7] In 2008, Lau *et al.* were the first to report and demonstrate metamorphic layer structures grown on Si substrates by MOCVD.[2] However, the device suffered relatively large gate leakage current from the Ge intermediate layer or composition grading buffer layers.

In this paper, in order to reduce the leakage current and improve the comprehensive DC and RF characteristics, a combination of expitial composite buffer growth technology of AlGaAs/AlAs MQW and two-stage EB lithography technology is developed to realize a 130-nm AlInAs/GaInAs mHEMT on Si substrate. The unique composite buffer layer of an AlGaAs/AlAs MQW for the transition from Si to the active device layer is developed to optimize the quality of the heterostructure material and to improve the DC and RF performances. The surface morphology and threading dislocation

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defects of mHEMT during the epitaxial growth by MOCVD are analyzed in detail. Finally, the devices of 130-nm gate-length mHEMT with a novel, less than 2-μm metamorphic buffer layer are fabricated and comprehensive DC and RF device characteristics are reported.

2. Materials growth and device fabrication

The $Al_{0.49}In_{0.51}As/Ga_{0.47}In_{0.53}As$ mHEMT is grown on a 4-inch (001) oriented p-type silicon substrate by MOCVD (1 inch = 2.54 cm). From top to bottom in Fig. 1(a), the $Al_{0.49}In_{0.51}As/Ga_{0.47}In_{0.53}As$ mHEMT consists of a 13-nm $Ga_{0.47}In_{0.53}As$ cap layer heavily doped with Si (7×10^{18} cm^{-3}), 13-nm undoped $Al_{0.49}In_{0.51}As$ Schottky barrier layer, Si-delta-doping layer (6×10^{12} cm^{-3}), 5-nm undoped $Al_{0.49}In_{0.51}As$ spacer layer, 30-nm $Ga_{0.47}In_{0.53}As$ channel, and a 2.0-μm composite buffer stack. From bottom to top, the 2.0-μm composite buffer stack includes 300-nm GaAs nucleation layer, 10-period AlGaAs/AlAs MQW layers (1 μm), 300-nm low temperature (HT)/high temperature (HT) GaAs buffer layer, 30-nm $Ga_{0.47}In_{0.53}As$ strain balance layer, and 300-nm composite LT/HT InP-lattice-matched AlInAs buffer layer grown at 500 °C/600 °C. The corresponding epitaxial structure schematic diagram is shown in Fig. 1(a). The 10-period AlGaAs/AlAs MQW (1 μm) is introduced into the HT-GaAs buffer layer to further prevent the defection or dislocation from penetrating into the top InP-matched layer. The thickness of the composite buffer is successfully scaled down to 2 μm for the first time. High-resolution triple-axis x-ray diffraction (HRXRD) is used to monitor the composition and relaxation state of these layers. The measured full-width at half maximum (FWHM) values of the GaAs buffer and InP buffer are around 328 arcsec and 320.3 arcsec, respectively, which indicates a good crystalline quality that is desirable for the good device performance.

A cross-sectional TEM image of the mHEMT grown on Si substrate with composite buffer is shown in Fig. 1(b), where few misfit dislocations and 60-degree threading dislocations could be observed in the composite buffer. The actual thickness of each layer is consistent with the designed thickness. The 300-nm thick AlInAs buffer, which includes LT and HT grown layers, is grown as a high resistivity isolation layer. A comparatively low defect density exists in the HT-AlInAs buffer due to the insert of LT-AlInAs layer, which has a thickness of at least 150 nm as an effective buffer to effectively prevent the threading dislocations. The simulated band diagram and corresponding electron distribution of $Al_{0.49}In_{0.51}As/Ga_{0.47}In_{0.53}As$ mHEMT with a quantum well structure is illustrated in Fig. 1(c). The excellent characteristic of distribution of channel carries and crystalline quality guarantee the development of high-performance GaInAs mHEMT on silicon substrate.

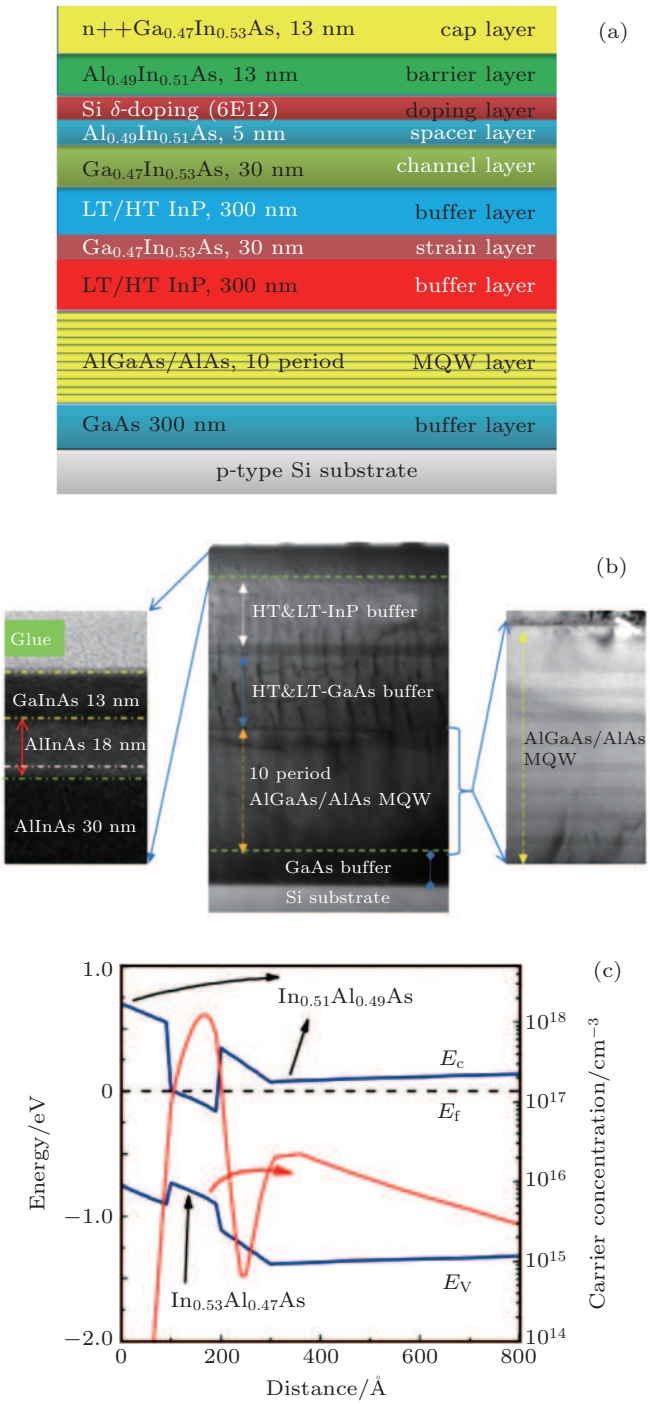


Fig. 1. (color online) (a) Nominal structure of mHEMT device on Si substrate, (b) TEM cross-section micrograph of mHEMT structure (note: panels (a) and (b) are not drawn to scale), (c) simulated band diagram and electron distribution of the mHEMT with quantum well structure.

An atomic force microscopy (AFM) image of an $Al_{0.49}In_{0.51}As/Ga_{0.47}In_{0.53}As$ mHEMT structure across a scanned area of 5 μm×5 μm is shown in Fig. 2(a). The root mean square (RMS) value of surface roughness of 2.4 nm is measured. Compared with Lau *et al.*'s work,[2] a smoother surface is demonstrated. In order to characterize the quality of the 2D electron gas (DEG), the Van Der Pauw–Hall measurements are carried out at 300 K and 77 K. The mea-

sured electron mobilities of 7800 $cm^2/V{\cdot}s$ and 23000 $cm^2/V{\cdot}s$ are obtained at 300 K and 77 K, with corresponding sheet carrier densities of 5×10^{12} cm^{-2} and 3×10^{12} cm^{-2}, respectively. The mobility of 2DEG at 77 K is greatly enhanced, and these mobility values are somewhat comparable to that of similar structure grown on GaAs substrate by MOCVD.[8,9] The excellent mobility performance of AlInAs/GaInAs mHEMT on Si substrate is attributed to the smoother InP-lattice-matched AlInAs buffer layer and AlGaAs/AlAs MQW composite buffer layer.

Two-stage electron beam (EB) lithography technology by a JBX-6300 e-beam lithography system is developed to fabricate a 130-nm AlInAs/GaInAs mHEMT on Si substrate. Firstly, AlInAs/GaInAs mHEMT is isolated by wet chemical etching, followed by source/drain definition. Then, the Ohmic metallization is achieved by the electron beam evaporation of Ni/Ge/Au/Ge/Ni/Au and lift-off process. At the same time, the measurement of contact resistivity is performed by transmission line model (TLM) method, a typical result is 0.06 Ω·mm. Secondly, first-stage EB lithography is used to determine the gate-footprint of T-shaped gate. The 100-nm SiN_x layer is deposited, followed by coating ZEP520 electron beam (EB) resist. ZEP520 EB resist is exposed at 1000 μc/cm^2 and is then developed in ZEN-N50 for 5 s. Then, SiN_x film is etched by $CHF_3/CF_4/O_2$ reactive ion etching (RIE) to mechanically support the T-shaped gate. The second-stage EB lithography is employed to form the gate-head pattern by coating bilayer polymethylmethacrylate/polymethylglutarimide (PMMA/PMGI) EB resist, followed by the EB exposition and selective development.[10,11] Thirdly, the gate-recess etching is performed by the use of Succinic-based acid to remove the highly doped GaInAs cap layer, followed by gate metallization through evaporating Ti/Pt/Au on the AlInAs barrier layer and lifting off. Finally, the electrodes of the mHEMT device were formed by the e-beam evaporation of Ti/Au and the lift-off process for the AlInAs/GaInAs mHEMT. A SEM cross-sectional photograph of T-shaped gate with 130-nm gate-length and 400-nm head-widths is shown in Fig. 2(b).

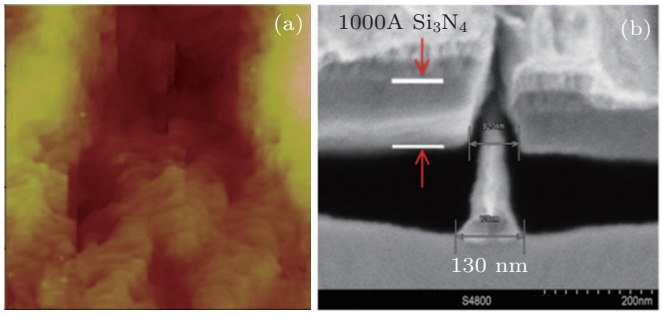


Fig. 2. (color online) (a) AFM image of a typical mHEMT structure, and (b) TEM cross-section micrograph of T-shaped gate

3. DC Characteristics

The measured current–voltage output characteristics of 0.13 μm×100 μm AlInAs/GaInAs mHEMT on Si substrate at room temperature by HP 4155 semiconductor parameter analyzer are shown in Fig. 3(a), where the gate–source voltage V_{GS} increases from (bottom) −2.4 V to (top) 0.6 V in step of 0.2 V. The maximum drain current ($I_{DS,max}$) of 1.13 A/mm is obtained at $V_{GS} = 0.6$ V and $V_{DS} = 2$ V, and is a new record of GaAs mHEMT on Si substrate. The peak extrinsic transconductance ($G_{m,max}$) of 854 mS/mm is obtained at the gate bias $V_{GS} = -0.15$ V and the drain bias $V_{DS} = 1.5$ V as shown in Fig. 3(b). The threshold voltage (V_{th}) of −0.8 V is derived by a linear extrapolation from the transfer curve shown in Fig. 3(b) at $V_{DS} = 1$ V, and indicates that the device is a depletion-mode transistor. The drain current after pinch-off is less than 1.8 mA/mm at $V_{GS} = -2.0$ V and $V_{DS} = 1.0$ V. The leakage current characteristic of the gate Schottky barrier of the mHEMT on Si substrate is shown in the inset of Fig. 3(b), where a slightly high reverse gate leakage current is due to the lack of passivation and a relatively high Schottky barrier height of 0.4 V is determined as the gate voltage when gate current is 0.1 mA. The gate leakage characteristic can be further improved by optimizing the structure of MQW composite buffer and InP-lattice-matched AlInAs buffer, which will be performed in future.

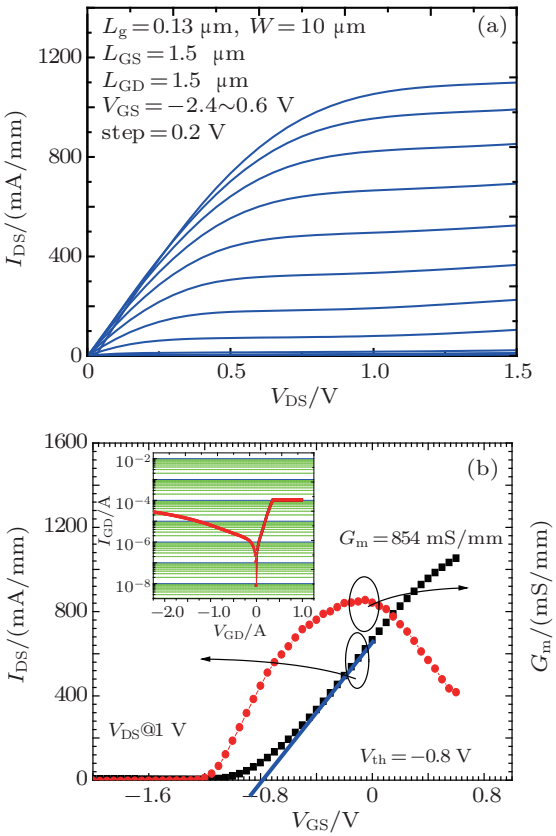


Fig. 3. (color online) DC characteristics of a 0.13 μm× 100 μm mHEMT: (a) *I–V* characteristics and (b) transfer characteristics.

4. RF performance

The RF performance of 0.13 μm×100 μm AlInAs/GaInAs mHEMT on Si substrate is obtained from the *S*-parameter measurements in a frequency range from 0.1 GHz to 39.1 GHz by Cascade Microtech probes and an HP8722 network analyzer at room temperature. The network analyzer is calibrated using an off-wafer standard short-open-load-through calibration, and on-wafer open and short patterns are used to de-embed the parasitic capacitances and inductances of the probe pads from the measured *S*-parameters of the mHEMT. Figure 4(a) shows the current gain $|h_{21}|^2$ and the maximum stable gain (MSG)/maximum available power gain (MAG) from the measured *S*-parameters after de-embedding as a function of frequency under the peak f_T bias condition $V_{GS} = -0.4$ V and $V_{DS} = 1.0$ V. The current cutoff frequency f_T is estimated to be 135 GHz from the extrapolation of $|h_{21}|^2$ with −20 dB/decade line, and the maximum frequency of oscillation f_{max} of 120 GHz is extrapolated by the −20 dB/decade slope in MSG/MAG curve. To the best of our knowledge, f_T of 135 GHz is the highest ever reported for AlInAs/GaInAs mHEMT on Si substrate by MOCVD featuring the same gate-length. The dependence of f_T on the gate bias is shown in Fig. 4(b), where f_T is symmetrical about gate voltage V_{GS} and demonstrates a good linearity with V_{GS} at both low and high gate biases.

The relationship between f_{max} and f_T is characterized by Eq. (1),[11] and is determined by the source resistance R_s, gate resistance R_g, drain conductance G_{ds}, intrinsic transconductance G_m, capacitance ratio C_{gs}/C_{gd} between the input gate-source capacitance and the feed-back gate–drain capacitance, and voltage gain G_m/G_{ds}. Table 1 shows the extracted equivalent circuit model parameter values from the measured 10 GHz–30 GHz *S*-parameters at $V_{GS} = -0.1$ V and $V_{DS} = 1.0$ V. Especially, to a great extent, the value of f_{max} largely depends on the capacitance ratio C_{gs}/C_{gd} and voltage gain G_m/G_{ds}. The relatively low output conductance (G_{ds}) of 14.8 mS and G_m/G_{ds} of 7.2 are successfully obtained. Moreover, the capacitance ratio C_{gs}/C_{gd} of 2.4, which is mainly responsible for the degradation of f_{max} in our mHEMT, leads to the high f_{max} of 120 GHz.

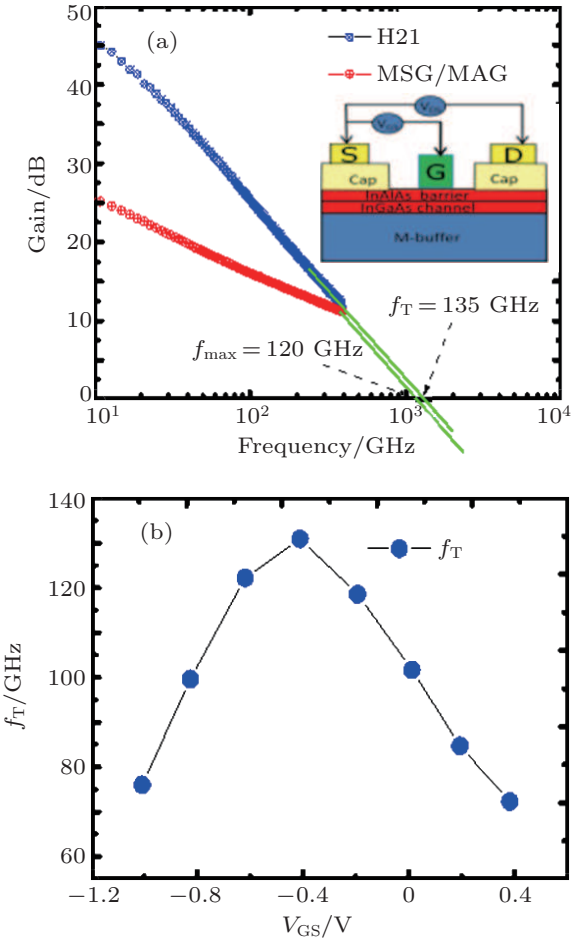


Fig. 4. (color online) (a) Current gain and MSG/MAG as a function of frequency for a 0.13 μm×100-μm mHEMT ($V_{DS} = 1.0$ V, $V_{GS} = -0.1$ V). (b) Small-signal characteristic of a 0.13 μm×100-μm mHEMT with V_{GS} varying from −0.8 V to 0.4 V.

$$f_{max} = \frac{f_T}{\sqrt{4\left(R_{in} \times G_{ds} + \dfrac{R_s + R_g}{1/G_{ds} + R_s \times G_m/G_{ds}}\right) + \dfrac{4}{5C_{gs}/C_{gd}}\left(1 + \dfrac{2.5}{C_{gs}/C_{gd}}\right)(1 + G_m R_s)^2}}. \quad (1)$$

Table 1. Small-signal equivalent circuit model parameters of 130-nm mHEMTs.

C_{gs}/fF	C_{gd}/fF	G_m/mS	G_{ds}/mS	C_{gs}/C_{gd}	G_m/G_{ds}
20.7	8.13	107	14.8	2.4	7.2

Table 2 shows a comparison of mobility (μ), G_m, f_T, and f_{max} for the recently reported AlInAs/GaInAs HEMTs, which are grown by MBE or MOCVD on GaAs or InP or Si substrates. The DC performance of mHEMTs grown by MOCVD is comparable to those of HEMTs by MBE. The metamorphic growth technology is used to manufacture mHEMTs on Si substrates in this work, and therefore more dislocations and rougher surface are inevitably introduced in the active layers than lattice-matched ones on InP substrates. However, they still exhibit attractive RF characteristics, which are very encouraging to the manufacture of metamorphic HEMTs on Si substrates by MOCVD for high-speed and low-power digital logic applications in the future.

Table 2. Comparison of performance among AlInAs/GaInAs HEMTs.

Hetero-structure	Sub	Growth	μ	L_g/nm	G_m/(mS/mm)	f_T/GHz	f_{max}/GHz	Date	Ref.
$In_{0.52}AlAs/In_{0.53}GaAs$	GaAs	MBE	N/A	100	750	154	300	2004	[12]
$In_{0.52}AlAs/In_{0.53}GaAs$	GaAs	MBE	9100	150	750	140	240	2007	[13]
InAlAs/InGaAs	InP	MBE	8500	150	800	151	172	2006	[14]
$AlIn_{0.50}As/GaIn_{0.53}As$	Si	MOCVD	4540	1000	587	32	44	2008	[2]
$In_{0.7}GaAs$ /$In_{0.52}AlAs$	Si	MBE	10000	80	1200	302		2007	[3]
$AlIn_{0.48}As/GaIn_{0.60}As$	Si	MOCVD	7800	130	854	135	120	2014	this work

5. Conclusions

In this work, metamorphic AlInAs/GaInAs HEMTs on silicon substrates grown by MOCVD have been successfully fabricated by two-stage EB lithography technology and MQW composite buffer growth technology. In these high-quality $Ga_{0.47}In_{0.53}As$ structures, the novel metamorphic buffer layer developed has a length of less than 2 μm, which effectively accommodates the lattice mismatch between the mHEMT device and the silicon substrate, thereby leading to a high-performance mHEMT with a relatively small gate leakage current. A 130-nm gate-length depletion-mode mHEMT exhibits a saturated peak DC transconductance of 854 mS/mm and an intrinsic f_T of 135 GHz at $V_{DS} = 1.0$ V and $V_{GS} = -0.1$ V. These encouraging results show the possibility of integrating the high-speed and low-power AlInAs/GaInAs mHEMT with the large-size and strong-mechanical-strength Si substrate for ultra-high-speed logic digital applications. The technology of mHEMT on silicon substrate by MOCVD that we have developed is very attractive for manufacturing low cost, large-scale similar CMOS ICs.

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