Charge trapping behavior and its origin in Al_2O_3/SiC MIS system*

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Charge trapping behavior and its origin in Al_2O_3/SiC MOS structure are investigated by analyzing the capacitance–voltage (C–V) hysteresis and the chemical composition of the interface. The C–V hysteresis is measured as a function of oxide thickness series for an Al_2O_3/SiC MIS capacitor. The distribution of the trapped charges, extracted from the C–V curves, is found to mainly follow a sheet charge model rather than a bulk charge model. Therefore, the electron injection phenomenon is evaluated by using linear fitting. It is found that most of the trapped charges are not distributed exactly at the interface but are located in the bulk of the Al_2O_3 layers, especially close to the border. Furthermore, there is no detectable oxide interface layer in the x-ray photoelectron spectroscope (XPS) and transmission electron microscope (TEM) measurements. In addition, Rutherford back scattering (RBS) analysis shows that the width of the Al_2O_3/SiC interface is less than 1 nm. It could be concluded that the charge trapping sites in Al_2O_3/SiC structure might mainly originate from the border traps in Al_2O_3 film rather than the interface traps in the interfacial transition layer.

Keywords: Al_2O_3, SiC, charge trapping sites, interface

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1. Introduction

The SiC metal-oxide semiconductor field-effect transistor (MOSFET) is a promising power transistor for high efficiency application. However, there are still many problems stemming from its gate dielectric (SiO_2), which is generated by thermal oxidation, such as low channel mobility and low reliability.[1–10] Alternative gate insulators have aroused increasing interest, especially in high permittivity (high-k) dielectrics, due to their ability to reduce both the electric field and the leakage current across the gate insulator. Among various high-k dielectrics, aluminum oxide (Al_2O_3) is a possible candidate due to its high dielectric constant (7–9), wide band gap (6.2 eV–7.0 eV), and high conduction band offset (1.7 eV) on 4H–SiC.[11–15]

Al_2O_3 film grown by atomic layer deposition (ALD) has demonstrated its excellent potential to be applied to SiC MOSFETs, which was proven to have ultra-high carrier mobility and low interface-trap density.[16–18] However, Al_2O_3 films have the microstructures and chemical natures different from those of SiC substrates. Therefore, the electrical properties of Al_2O_3/SiC structure grown by ALD method are not as good as expected due to the high density of charge trapping sites existing at the interface or in the bulk oxide.[19] These charge trapping sites can be manifested as hysteresis in the C–V response, resulting in device instability. Some studies demonstrate that the C–V hysteresis of Al_2O_3/SiC structure could be reduced by high-temperature annealing, whereas the amorphous Al_2O_3 layer begins to crystallize and a sub-oxide layer forms at the interface after being annealed at 900 °C in an inert gas atmosphere.[15,20,21] In addition, forming gas annealing (FGA) has also been used to improve the interfacial properties Al_2O_3/substrate.[22] The hydrogen in the FGA is useful to passivate the dangling bonds, whereas it seems to have no distinct effect on the reduction of the C–V hysteresis.[23] Furthermore, an ultrathin SiO_2 layer has been inserted between the Al_2O_3 and SiC substrate as a barrier layer against electron injection.[24,25] Significant V_{FB} shifts are still observed under a high electric field and the properties of Al_2O_3/SiO_2/SiC structure appear to be dominated by the SiO_2/SiC interface, exhibiting a high D_{it} close to E_c.[19,26–28] So far, the issue of C–V hysteresis in Al_2O_3/SiC MOS system has not been solved. The density, physical position, and origin of the charge trapping sites are still not clear. The study of C–V hysteresis is important because it provides a method to analyze and quantify the density and physical distribution of charge trapping sites. Thus, a better understanding of the origin of the charge trapping sites can be gained and further improvements can be achieved based on these experimental results.

In this work, we investigate the charge trapping behavior and its origin by analyzing the C–V hysteresis and the chemical composition of Al_2O_3/SiC interface. To examine the den-

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sity and distribution of the trapped charges, *C–V* hysteresis is measured as a function of oxide thickness series for Al_2O_3/SiC MIS capacitor. It is found that the distribution of the trapped charges mainly follows a sheet charge model and the actual distribution of the trapped charge is not applicable for the case at the interface. Furthermore, the microstructures of the interface are investigated by XPS, TEM, and RBS measurements. No distinct interface oxide is found through XPS measurement or TEM measurement, indicating that an abrupt interface is achieved. It can therefore be concluded that the charge trapping sites in Al_2O_3/SiC structure originate from the native defects in Al_2O_3 film, predominantly the border traps. These experimental results also provide an insight into methods that can further reduce the density of trapping sites.

2. Experiment

N-type, 4° off (0001) oriented, 4H–SiC wafers with 12-μm thick epilayer ($N_D \sim 8 \times 10^{15}$ cm^{-3}) of nitrogen were used. The thickness and resistivity of each of the n-type SiC substrates were 350 μm and 0.023 Ω·cm, respectively. These wafers were purchased from the EpiWorld International Co. Ltd. The wafers were cleaned by the conventional Radio Corporation of America (RCA) clean procedure, and then dipped into a diluted hydrofluoric acid solution to remove native oxide from the SiC surface. Al_2O_3 films of different thickness values, 12.9 nm–50 nm, were deposited by ALD technique at 350 °C using TMA and water as precursors. MIS capacitors were fabricated to evaluate the electrical characterization. The gate pads were patterned into circles each with a diameter of 100 μm. Then 20 nm/200 nm Ni/Au layers were deposited by e-beam evaporation and followed by lift-off process. A 200-nm Al layer was sputtered to form the back contact. For x-ray photoelectron spectroscopy (XPS) analysis, a thin Al_2O_3 film (2 nm) on a 4H–SiC substrate was prepared. In addition, a 21.6-nm Al_2O_3 film on the 4H–SiC substrate was prepared for TEM and RBS measurements.

Film thickness was determined by UVISEL spectroscopic ellipsometry and TEM. The ellipsometry model was adjusted according to TEM results. The triple-angle method with incident angles of 65°, 70°, and 75° was applied to optical properties and thickness of the Al_2O_3 film. The *C–V* measurements were conducted by the Agilent 4284A precision impedance analyzer at room temperature (1 kHz∼ 1 MHz) under dark condition. All the *C–V* hysteresis measurements were performed in voltage steps of 0.1 V. The sweep voltages were measured by starting from inversion, and sweeping towards the accumulation region, and subsequently sweeping back towards inversion. There was no hold time in accumulation. The interface state density (D_{it}) was determined by the conductance technique. The capacitance and conductance were measured in a frequency range from 1 kHz to 1 MHz. Before applying the conductance method, the values of the series resistance were determined for each frequency from the impedance measured in a strong accumulation region. Then, series resistance was removed from the measured capacitance and conductance.[29] The interface state density is linked to G_P by

$$G_P/\omega = e^2 S D_{it} \int_{-\infty}^{+\infty} \frac{\ln(1+(\omega\tau\exp(\eta)^2)}{2\omega\tau\exp(\eta)} \times \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{\eta^2}{2\sigma^2}\right) \mathrm{d}\eta, \quad (1)$$

where G_P is the interface state conductance, ω is the angular frequency, S is the area of the gate electrode, and e (1.602×10^{-19} C) is the elementary electric charge. The interface state density (D_{it}), the time constant of the interface states (τ), and the standard deviation (σ) are determined using a simple method provided by Nicollian and Brews.[29] The energy level (E_c–E_T) of interface states is calculated from

$$E_C - E_T = e(0.21 - \psi_s) \quad (2)$$

by taking into account the Fermi level of the SiC epilayer (E_c-0.21 eV) at room temperature. Here ψ_s is the surface potential determined from a comparison of ideal *C–V* curve and measured high frequency *C–V* curve.[29] XPS analysis was performed by using a Thermo SCIENTIFIC ESCALAB 250 spectrometer equipped with a monochromatic Al Kα x-ray source (1486.6 eV) from a 90° take-off angle (normal to surface). The atomic structures at the interface and in the bulk Al_2O_3 were investigated through the peak deconvolution of Si 2p and Al 2p photoelectron spectra. The microstructure and the composition of the Al_2O_3/SiC interface were investigated by TEM and RBS.

3. Results and discussion

To examine the density and distribution of the trapped charges, the *C–V* hysteresis is measured as a function of oxide thickness series for Al_2O_3/SiC MIS capacitors. Both the bulk charge model and the sheet charge model are used to fit the curves of *C–V* hysteresis versus physical thickness (t_{ox}).[30] For the bulk charge model, the trapped charges are considered to be uniformly distributed throughout the oxide. The *C–V* hysteresis is then proportional to the square of the oxide thickness, as expressed below

$$\Delta V = \frac{qQ_{trapped} \times t_{ox}^2}{2\varepsilon_0\varepsilon_k}, \quad (3)$$

where ε_0 is the vacuum permittivity, ε_k is the relative permittivity of Al_2O_3, t_{ox} is the physical thickness, and $Q_{trapped}$ is the population of trapped charge in cm^{-2}. For the sheet charge model, the trapped charges are located at the interface or in a plane within the oxide. The *C–V* hysteresis increases linearly with the increasing of oxide thickness. This linear relationship can be expressed by the following equation:

$$\Delta V = \frac{qQ_{trapped} \times t_{ox}}{\varepsilon_0\varepsilon_k}. \quad (4)$$

During the C–V measurements, keeping the same maximum electric field (E_{max}) in the accumulation region (i.e., the same $E_{max} = (V_{max} - V_{FB})/t_{ox}$) is very important for Al_2O_3/SiC MIS capacitors with varying oxide thickness values. The comparison is valid because the same quantity of majority carriers will accumulate at the SiC surface when the values of E_{max} are the same. Figure 1 presents the relationship between the equivalent oxide thickness (EOT) and physical thickness (t_{ox}) for Al_2O_3/SiC MOS structures with t_{ox} ranging from 12.9 nm to 50 nm. The EOT is calculated from the capacitance in accumulation region of 1-kHz C–V curve. The dielectric constant of Al_2O_3 extracted from the slope of the EOT versus t_{ox} curve is 8.39. V_{FB} is extracted from the maximum capacitance in accumulation (C_{max}) and the minimum capacitance in depletion (C_{min}) from 1-MHz C–V curves. The dielectric capacitance (C_{ox}) is extracted from the capacitance and conductance measured in strong accumulation region. The C_{min} coupled with C_{ox} is used to determine the substrate capacitance in depletion, allowing an evaluation of the substrate doping level. The total capacitance in the flat band condition is then calculated from the substrate capacitance in the flat band condition and C_{ox}. The substrate doping concentrations have also been obtained from the reciprocal of the slope of the $1/C^2$ versus

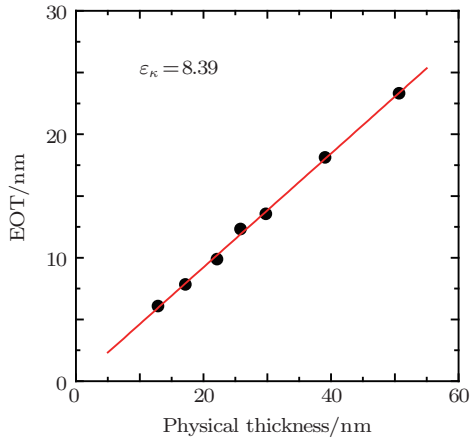


Fig. 1. (color online) Plot of the EOT versus t_{ox} for MIS capacitors with t_{ox} ranging from 12.9 nm∼50 nm.

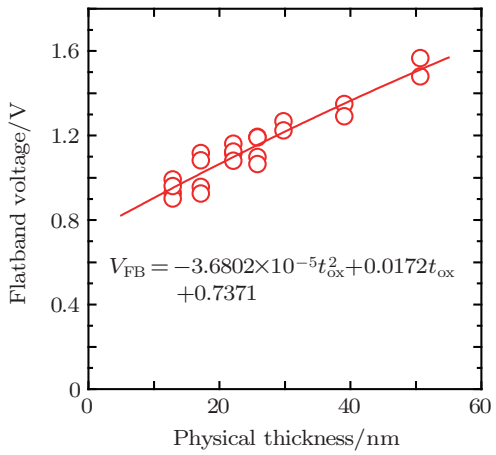


Fig. 2. (color online) Plot of V_{FB} versus t_{ox} for Al_2O_3/SiC MIS capacitors.

V_G curves.[31] For both methods, the calculated substrate doping concentrations are both about 8×10^{15} cm^{-3}, which is consistent with the data offered by the wafer producer. The extracted V_{FB} as a function of oxide thickness is depicted in Fig. 2. The D_{it} is extracted from the G_p/ω-frequency characteristics by the conductance technique, as shown in Fig. 3. Figure 4 shows the D_{it} as a function of the position in the band-gap from a 12.9-nm Al_2O_3/SiC sample.

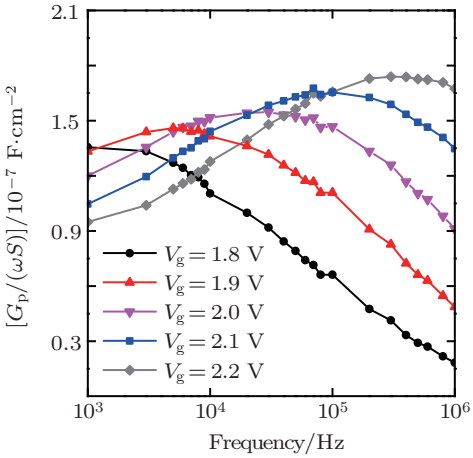


Fig. 3. (color online) Curves of $G_p/(\omega S)$ versus frequency at several biases for a 12.9-nm Al_2O_3/SiC MIS capacitor. S is the area of the capacitor.

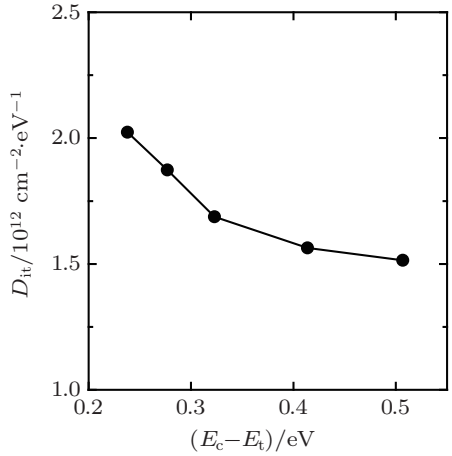


Fig. 4. Plot of the density of interface states as a function of the position in the band gap, calculated from $G_P/(\omega S)$ versus frequency data from Fig. 3.

The C–V hysteresis (1 MHz) is measured as a function of oxide thickness series for Al_2O_3/SiC MIS capacitors at different maximum electric fields (3.10, 3.49, 3.87, and 4.26 MV/cm). The change of the V_{FB} as a function of oxide thickness is also taken into consideration to determine the E_{max}. For example, in order to achieve a maximum electric field of 4.26 MV/cm for all the samples, the maximum voltages in the accumulation region are varied from 6.5 V to 23.5 V for Al_2O_3 layers with different thickness values, as shown in Fig. 5. The C–V hysteresis is estimated from the shift of V_{FB} between forward and backward C–V curves. Both quadratic fit and linear fit have been adopted to fit the C–V

hysteresis versus t_{ox} curves, which are summarized in Table 1. For the quadratic fitting, the quadratic coefficients are all kept at a value of 0.0016, indicating that the densities of the injected electrons in the bulk Al_2O_3 films are kept constant under different values of E_{max}. However, the linear coefficients increase rapidly with the increase of the E_{max}. It can be concluded that the majority of the charge trapping possibly occurs in a plane near the Al_2O_3/SiC interface and is not uniformly distributed throughout the oxide. Thus, a simple sheet charge model approximation (linear fit) is used to evaluate the actual effect of the electron injection phenomenon, as depicted in Fig. 6. The $Q_{trapped}$ is extracted from the slope of linear fit, based on Eq. (4). The injected charge quantity increases with increasing the value of E_{max} and reaches a highest value, i.e., 1.29×10^{13} cm^{-2}, at an E_{max} of 4.26 MV/cm, as shown in Table 1. When the Al_2O_3/SiC capacitor is biased at a high electric field, the trap levels in Al_2O_3 layer, which are primarily located above the SiC conduction band under the flat band condition, will be located below the SiC conduction band.[32] Then, the electron trapping from the substrate is energetically favorable. As the maximum electric field increases, more charge trapping sites will be located below the SiC conduction band and the extent of SiC band bending will also be aggravated. Thus, more electrons will be injected into the Al_2O_3 layer from SiC substrate. The level of trapped charge sites is comparable to the interface states density (D_{it}) of Al_2O_3/SiC structure (2.02×10^{12} cm^{-2}·eV^{-1} at E_c–E_t = 0.23 eV), which highlights the importance of electron trapping in Al_2O_3/SiC system. Furthermore, it can be noted that none of the linear fitted lines intersect the origins of the plot and the intercepts of X axis are all on the right half axis in Table 1. If the electrons are injected into the interface of Al_2O_3/SiC, then the fitted line should follow the format of Eq. (4) and pass through the origin of the plot. We speculate that most of the trapped charges are not distributed exactly at the interface but are located in the bulk of the Al_2O_3 layers and they are especially close to the border, resulting in the right shift of fitted line along the X axis. A similar behavior has been reported in Si-based MOS capacitors with Al_2O_3/SiO_2 gate stacks.[28,33] So the equivalent injection depths of the trapped charges can be extracted from the intercept of X axis from the linear fitting formulas. For the E_{max} values ranging from 3.10 MV/cm to 4.26 MV/cm, the equivalent injection depths, extracted from the intercepts of X axis, are 3.53, 3.19, 3.29, and 3.69 nm, respectively.

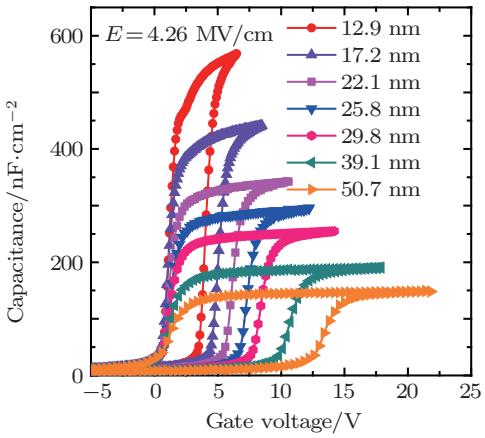


Fig. 5. (color online) Bi-direction C–V curves for MIS capacitors with an E_{max} value of 4.26 MV/cm (gate swings from −5 V to V_{max} and then back to −5 V).

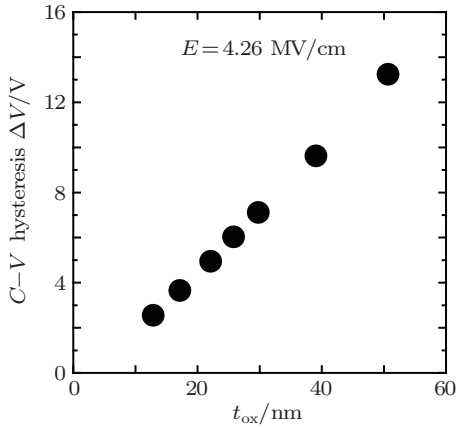


Fig. 6. C–V hysteresis as a function of oxide thickness for Al_2O_3/SiC MIS capacitors.

Table 1. Fitting formulas of C–V hysteresis versus t_{ox} curves. Both the $Q_{trapped}$ and the equivalent injection depths are extracted from the linear fitting formulas.

E_{max}/(MV/cm)	Quadratic fit	Linear fit		
			$Q_{trapped}$/cm^{-2}	Depth/nm
4.26	$0.0016t_{ox}^2+0.1801t_{ox}+0.2954$	$0.2789(t_{ox}-3.69)$	1.29×10^{13}	3.69
3.87	$0.0015t_{ox}^2+0.1453t_{ox}+0.4572$	$0.2378(t_{ox}-3.29)$	1.10×10^{13}	3.29
3.49	$0.0016t_{ox}^2+0.1042t_{ox}+0.6794$	$0.2033(t_{ox}-3.19)$	0.94×10^{13}	3.19
3.10	$0.0016t_{ox}^2+0.0745t_{ox}+0.7465$	$0.1765(t_{ox}-3.53)$	0.81×10^{13}	3.53

The microstructure and chemical structure of the Al_2O_3/SiC interface are also investigated to further seek the origin of these charge trapping sites. As shown in Fig. 7, no distinct interface transition layer is found between the amorphous Al_2O_3 layer and 4H–SiC substrate through the TEM measurement. The plots of composition of the Al_2O_3/SiC film versus the depth are shown in Fig. 8, which is calculated from the RBS data. The width of the Al_2O_3/SiC interface (the transition from SiC layer into Al_2O_3 layer) is limited to less than 1 nm. Considering the fact that the injection depth is a

distance ranging from 3 nm to 4 nm, the distribution of the trapped charges is far from the interface. To analyze the XPS data, the spin–orbit splitting of Al 2p spectra is considered from Al $2p_{3/2}$ and Al $2p_{1/2}$ lines split by 0.41 eV and an intensity ratio of 2:1. Figure 9(a) shows the Al 2p spectra of 2-nm Al_2O_3/SiC sample. The XPS curves can be well fitted by two Gauss peaks corresponding to the Al_2O_3. It is indicated that Al_2O_3 is formed at the first 2 nm. But, this does not mean that defects relating to Al do not exist in the film. Considering that the density of the charge trapping sites is about 1×10^{13} cm^{-2} and the Al areal density in Al_2O_3 layer is 6.94×10^{16} cm^{-2}, it is beyond the measurement range of XPS method. The Si 2p spectra are deconvoluted into two components corresponding to the Si atoms from the bulk SiC substrate and the Si atoms in the intermediate oxide states (Si 1+), as shown in Fig. 9(b). As reported by Gao *et al.*, the Si^{1+} atomics form a monolayer on top of SiC and below Al_2O_3, right at the interface.[13] So in the ALD process, the Al_2O_3 layer is attached by bridging oxygen atoms to the topmost Si layer of 4H–SiC (0001) surface. This oxygen bridge has also been reported at Al_2O_3/Si interface.[34,35] It is commonly believed that the presence of Al_2O_3 has been concluded in catalyzing the oxidation of Si (SiC). The intermediate oxide states 1+ of silicon atoms originate from Si–O–Al bond at the interface between Al_2O_3 and SiC. No other sub-oxides of Si are found and it may benefit from the reported "self-cleaning" effect of the ALD Al_2O_3 process.[36] A sharp interface is achieved, which accords with our TEM result.

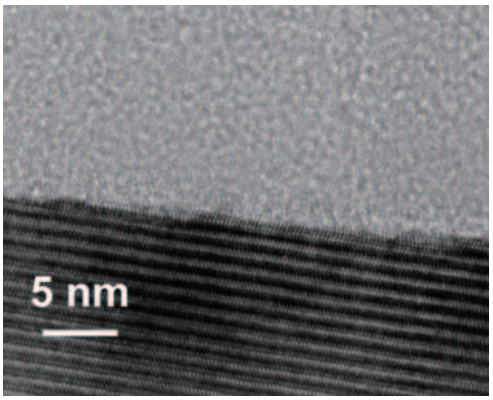


Fig. 7. TEM image, showing the interface region of a 21.6-nm Al_2O_3 film on the 4H–SiC substrate.

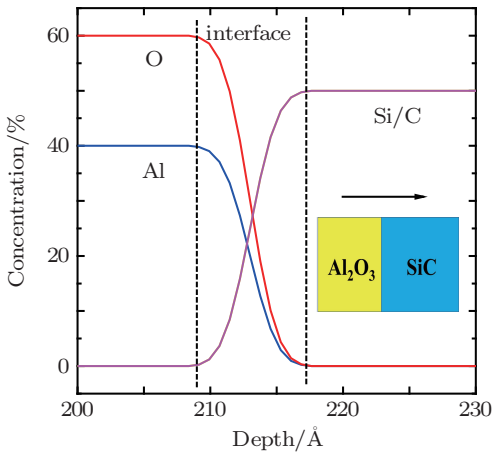


Fig. 8. (color online) Variations of composition of the Al_2O_3/SiC films with depth.

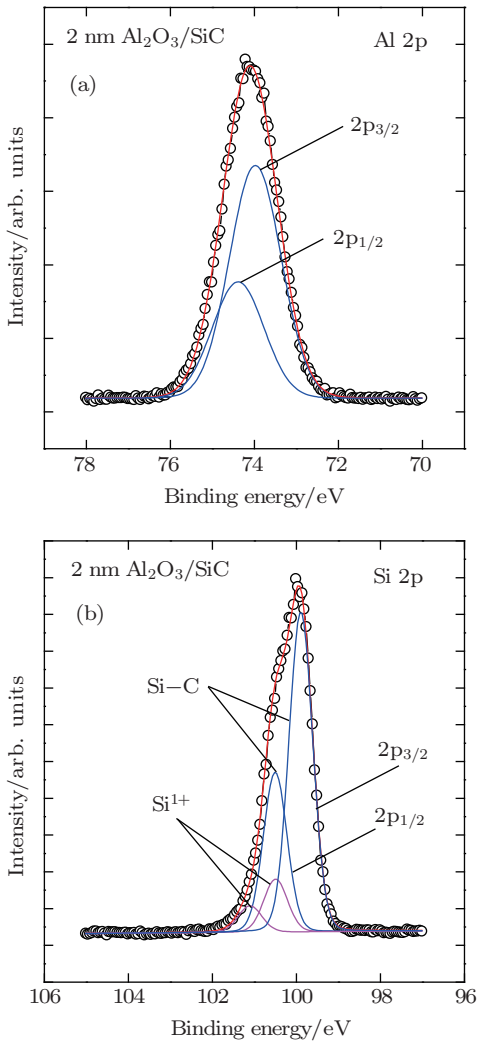


Fig. 9. (color online) XPS spectra of (a) Al 2p in 2-nm Al_2O_3 on 4H–SiC substrate, and (b) Si 2p in 2-nm Al_2O_3 on 4H–SiC substrate.

4. Conclusions

Charge trapping behavior in an Al_2O_3/SiC MOS structure is investigated. *C–V* hysteresis is measured as a function of oxide thickness series for Al_2O_3/SiC MIS capacitors. The distribution of the trapped charges mainly follows a sheet charge model rather than a bulk charge model. Then, a linear fitting is adopted to evaluate the density and injected depth of the trapped charges. A remarkable *C–V* hysteresis is observed and the density of trapped charges could be as high as 10^{13} cm^{-2}. The injection depths are 3.53, 3.19, 3.29, and 3.69 nm for the E_{max} values ranging from 3.10 MV/cm to 4.26 MV/cm. It is revealed that the actual distribution of the trapped charges is not applicable for the case at the interface. No distinct interface transition layer is found in the TEM result or in the XPS

result. The intermediate oxide states 1+ of silicon atoms in XPS results are attributed to Si–O–Al bond at the interface of Al_2O_3 and SiC. According to the RBS data, the width of transition from SiC to Al_2O_3 is less than 1 nm. These results indicate that a sharp interface is achieved between Al_2O_3 and SiC. It can be concluded that charge trapping sites in Al_2O_3/SiC structure originate from the native defects in Al_2O_3 film rather than the interface traps in the interface transition layer. Further research into the improvement of quality of Al_2O_3 film is still required to reduce the number of charge trapping sites.

References

[1] Li H, Dimitrijev S, Harrison H B and Sweatman D 1997 *Appl. Phys. Lett.* **70** 2028

[2] McDonald K, Weller R A, Pantelides S T, Feldman L C, Chung G Y, Tin C C and Williams J R 2003 *J. Appl. Phys.* **93** 2719

[3] Dhar S, Song Y W, Feldman L C, Isaacs-Smith T, Tin C C, Williams J R, Chung G, Nishimura T, Starodub D, Gustafson T and Garfunkel E 2004 *Appl. Phys. Lett.* **84** 1498

[4] Lu C Y, Cooper J A, Tsuji T, Chung G, Wiliams J R, McDonald K and Feldman L C 2003 *IEEE Trans. Electron Dev.* **50** 1582

[5] Chung G Y, Tin C C, Wiliams J R, McDonald K, Chanana R K, Weller R A, Pantelides S T, Feldman L C, Holland O W, Das M K and Palmour J W 2001 *IEEE Electron Dev. Lett.* **22** 176

[6] Rozen J, Ahyi A C, Zhu X G, Williams J R and Feldman L C 2011 *IEEE Trans. Electron Dev.* **58** 3808

[7] Fujihira K, Tarui Y, Imaizumi M, Ohtsuka K, Takami T, Shiramizu T, Kawase K, Tanimura J and Ozeki T 2005 *Solid-State Electron.* **49** 896

[8] Yoshioka H, Nakamura T and Kimoto T 2014 *J. Appl. Phys.* **115** 014502

[9] Noborio M, Grieb M, Bauer A J, Peters D, Friedrichs P, Suda J and Kimoto T 2011 *Jpn. J. Appl. Phys.* **50** 090201

[10] Matocha K, Dunne G, Soloviev S and Beaupre R 2008 *IEEE Trans. Electron Dev.* **55** 1830

[11] Lazar H R, Misra V, Johnson R S and Lucovsky G 2001 *Appl. Phys. Lett.* **79** 973

[12] Groner M D, Elam J W, Fabreguett H H and George S M 2002 *Thin Solid Films* **413** 186

[13] Gao K Y, Seyller T, Ley L, Ciobanu F, Pensl G, Tadich A, Riley J D and Leckey R G C 2003 *Appl. Phys. Lett.* **83** 1830

[14] Tanner C M, Perng Y C, Frewin C, Saddow S E and Chang J P 2007 *Appl. Phys. Lett.* **91** 203510

[15] Avice M, Grossner U, Pintilie I, Svensson B G, Servidori M, Nipoti R, Nilsen O and Fjellvag H 2007 *J. Appl. Phys.* **102** 054513

[16] Hino S, Hatayama T, Miura N, Oomori T and Tokumitsu E 2007 *Mater. Sci. Forum* **556** 787

[17] Moriya H, Hino S, Miura N, Oomori T and Tokumitsu E 2009 *Mater. Sci. Forum* **615** 777

[18] Hino S, Hatayama T, Kato J, Tokumitsu E, Miura N and Oomori T 2008 *Appl. Phys. Lett.* **92** 183503

[19] Cheong K Y, Moon J H, Eom D, Kim H J, Bahng W and Kim N K 2007 *Electrochem. Solid ST* **10** H69

[20] Avice M, Diplas S, Thogersen A, Christensen J S, Grossner U, Svensson B G, Nilsen O, Fjellvag H and Watts J F 2007 *Appl. Phys. Lett.* **91** 052907

[21] Wang Y Y, Shen H J, Bai Y, Tang Y D, Liu K A, Li C Z and Liu X Y 2013 *Chin. Phys. B* **22** 078102

[22] Kim E J, Wang L, Asbeck P M, Saraswat K C and Mclntyre P C 2010 *Appl. Phys. Lett.* **96** 012906

[23] Hu J and Philip Wong H S 2012 *J. Appl. Phys.* **111** 044105

[24] Lichtenwalner D J, Misra V, Dhar S, Ryu S and Agarwal A 2009 *Appl. Phys. Lett.* **95** 152113

[25] Hatayama T, Hino S, Miura N, Oomori T and Tokumitsu E 2008 *IEEE Trans. Electron Dev.* **55** 2041

[26] Hosoi T, Harada M, Kagei Y, Watanabe Y, Shimura T, Mitani S, Nakano Y, Nakamura T and Watanabe H 2009 *Mater. Sci. Forum* **615** 541

[27] Avice M, Grossner U, Pintilie I, Svensson B G, Nilsen O and Fjellvag H 2006 *Appl. Phys. Lett.* **89** 222103

[28] Hosoi T, Kagei Y, Kirino T, Mitani S, Nakano Y, Nakmura T, Shimura T and Watanabe H 2011 *Mater. Sci. Forum* **679** 496

[29] Nicollian E H and Brews J R 2003 *MOS Physics and Technology* (Hoboken: Wiley) pp. 212–226 and 325–328

[30] Lin J, Gomeniuk Y Y, Monaghan S, Povey I M, Cherkaoui K, Connor E O, Power M and Hurley P K 2013 *J. Appl. Phys.* **114** 144105

[31] Schroder D K 2006 *Semiconductor Material and Device Characterization*, 3rd edn. (Hoboken: Wiley) pp. 71–75

[32] Xu M, Xu C H, Ding S J, Lu H L, Zhang D W and Wang L K 2006 *J. Appl. Phys.* **99** 074109

[33] Kerber A, Cartier E, Degraeve R, Pantisano L, Roussel P and Groeseneken G 2002 *Symposium on VLSI Dig.*, June 11–13, 2002, Honolulu, USA, p. 76

[34] Puurunen R L and Vandervorst W 2004 *J. Appl. Phys.* **96** 4878

[35] Frank M M, Chabal Y J and Wilk G D 2003 *Appl. Phys. Lett.* **82** 4758

[36] Klejna S and Elliot S D 2012 *J. Phys. Chem. C* **116** 643