Characteristics of drain-modulated generation current in n-type metal-oxide-semiconductor field-effect transistor*

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Drain-modulated generation current I_{DMG} induced by interface traps in an n-type metal-oxide-semiconductor field-effect transistor (nMOSFET) is investigated. The formation of I_{DMG} ascribes to the change of the Si surface potential φ_s. This change makes the channel suffer transformation from the inversion state, depletion I state to depletion II state. The simulation result agrees with the experiment in the inversion and depletion I states. In the depletion II state, the theoretical curve goes into saturation, while the experimental curve drops quickly as V_D increases. The reason for this unconformity is that the drain-to-gate voltage V_{DG} lessens φ_s around the drain corner and controls the falling edge of the I_{DMG} curve. The experiments of gate-modulated generation and recombination currents are also applied to verify the reasonability of the mechanism. Based on this mechanism, a theoretical model of the I_{DMG} falling edge is set up in which I_{DMG} has an exponential attenuation relation with V_{DG}. Finally, the critical fitting coefficient t of the experimental curves is extracted. It is found that $t = 80\ \text{mV} = 3kT/q$. This result fully shows the accuracy of the above mechanism.

Keywords: interface trap, generation, surface potential, nMOSFET

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1. Introduction

The generation current in the metal-oxide-semiconductor field-effect transistor (MOSFET) is a leakage current that results from the interface traps which serve as the generation sites when the channel is in the non-equilibrium state.[1,2] Since this type of current is closely related to the traps, it is widely used to detect the damage created by the hot carrier and the negative bias temperature instability (NBTI) stresses.[3–5] Scoot *et al.* applied this current to study the radiation damage in x-ray imagers and proposed a new pixel design based on gated diode structures that will provide the improved image quality.[6] Our previous paper studied the degradation of MOSFET by the method of generation current transconductance,[7] then we discussed the effect of substrate bias on the generation current and recently set up a theoretical model for this current.[8,9] In addition, the generation current was also involved in several researches about the fin field-effect transistor and its reliability issues.[10,11]

All the generation currents used in the above studies are gate-modulated. This type of current can be measured by the method of sweeping the gate which makes the channel state change from accumulation, depletion to inversion. In the measurement, the drain bias V_D is fixed to keep the quasi-Fermi level of the substrate minority carrier unchanged, and therefore it plays the role of maintaining the non-equilibrium state in the depletion region during the formation of gate-modulated generation current. However, V_D is often varied in the work condition of MOSFET meaning that the non-equilibrium state is dynamic. Since the dynamic non-equilibrium state should affect the generation function of interface traps, a new important problem arises: what is the feature of the generation current under the dynamic non-equilibrium condition? It can also be expressed as: how does the drain modulate the generation current? Nonetheless, little attention has been paid to this problem so far.

On the basis of the above discussion, this paper aims to reveal the features of drain-modulated generation current I_{DMG} and expound the deep physical mechanisms behind these features. The nMOSFET with a 4-nm gate oxide thickness was used in this paper. Through analyzing the changes of I_{DMG} versus V_D, their relationship and the related physical mechanisms are discussed deeply by combining experimental results with theoretical analysis.

2. Experiments and drain-modulated generation current theory

The device used in this paper was an nMOSFET with an n^+ poly-Si gate fabricated by using 90-nm complementary-metal-oxide-semiconductor (CMOS) technology. The gate oxide thickness t_{ox} was 4 nm with width/length = 6 μm/0.35 μm. The threshold voltage of the device was 0.49 V. For the drain-modulated generation current measurement, floating the source and grounding the substrate, the drain was swept from −0.2 V to 1.0 V. The gate bias V_G was fixed at 0.1, 0.2, 0.3, 0.4,

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0.5, 0.6, and 0.8 V. The drain current was I_{DMG}. The schematic diagram of the I_{DMG} measurement is shown in Fig. 1. All electrical tests were performed by using a Keithley 4200 precision semiconductor parameter analyzer. In addition, all the simulations were done using the MATLAB software.

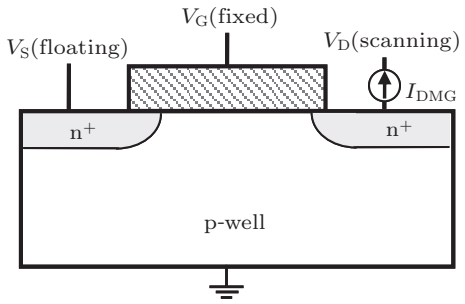


Fig. 1. The schematic diagram of the drain modulated generation current I_{DMG} measurement with nMOSFET.

The I_{DMG} is an interface trap-induced drain leakage current because of the Shockley–Read–Hall (SRH) effect. In the SRH model, the electron density n_s and hole density p_s at the interface Si/SiO_2 can change the generation rate g. The relationship between them is[12]

$$g = (n_i^2 - n_s p_s)/(n_s + p_s + 2n_i), \tag{1}$$

where n_s and p_s can be written as

$$n_s = n_0 \exp[(\varphi_s - mV_D)/\beta], p_s = p_0 \exp(-\varphi_s/\beta), \tag{2}$$

with n_0 and p_0 the substrate minority and majority carrier density, respectively, $p_0 = N_A$ and $\beta = kT/q$, m is the adjustment coefficient for the practical device and $m = 1$ in the ideal situation, while φ_s is the surface potential given by

$$\varphi_s = \frac{q\varepsilon_s N_A}{C_{ox}^2} + V_G - V_{FB} - \frac{(2q\varepsilon_s N_A)^{1/2}}{C_{ox}} \sqrt{\frac{q\varepsilon_s N_A}{2C_{ox}^2} + V_G - V_{FB} + V_D}. \tag{3}$$

When the substrate doping is not heavy, the first and fourth items in Eq. (3) are too small and can be ignored. Thus φ_s is dominated by (V_G–V_{FB}). If $V_G > 0$ V, $\varphi_s > 0$ V because V_{FB} is negative generally. The change of V_D results in the change of n_s at the given V_G according to Eq. (2), which eventually causes g changes. Since V_D is larger than 0, n_s decreases with the increase in V_D.

When $n_s \geq p_0$, the channel Si surface is stepped into the inversion state, then a larger number of electrons make the interface traps lose their generation roles and g is zero. In this case, V_D can be deduced according to the expression of n_s in Eq. (2) as follows:

$$V_D \leq [\varphi_s - 2\beta \ln(p_0/n_i)]/m. \tag{4}$$

As V_D increases, n_s decreases which leads to the Si surface presenting the depletion state, then g should increase with the increase in V_D.

When $n_s \leq n_i/5$ that is one-tenth of $2n_i$, the change of n_s has no effect on g. In this case, V_D should be

$$V_D \geq [\varphi_s - \beta \ln(5p_0/n_i)]/m. \tag{5}$$

For p_s, it cannot affect g only if $p_s <= n_i/5$. According to Eq. (2), there is

$$\varphi_s \geq \beta \ln(p_0/n_i) + \beta \ln 5, \tag{6}$$

so combining Eqs. (3) and (6), it is deduced as

$$V_G \geq V_{FB} + \beta \ln(5p_0/n_i), \tag{7}$$

which shows that V_G should be very small or even negative in the case of $p_s = n_i/5$ under $V_{FB} < 0$ V when p_0 is not heavy. Hence, if V_G is larger than this critical value, p_s has no influence on g in theory. In a word, g should almost keep constant when the value of V_D satisfies Eq. (5).

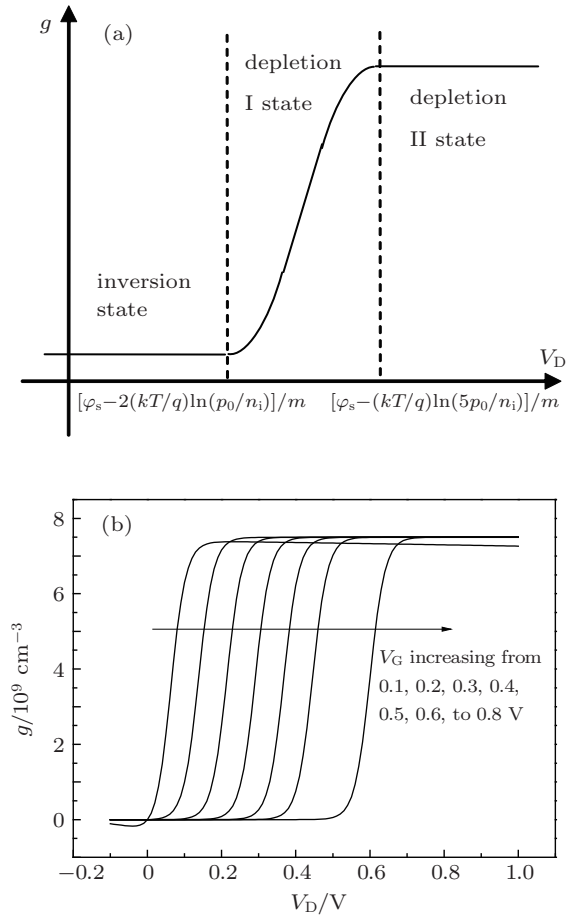


Fig. 2. (a) A schematic diagram of the relationship between V_D and g. (b) Curves of the simulated g versus V_D. In the simulation, $t_{ox} = 4$ nm and $p_0 = N_A = 4 \times 10^{15}$ cm^{-3}, $m = 1.25$ and $V_{FB} = -0.35$ V.

Figure 2(a) shows a schematic diagram of the relationship between V_D and g. As V_D increases with a given V_G, g increases and the channel state changes from inversion to depletion. Moreover, the depletion divides into two depletion

states: I state and II state. Figure 2(b) shows the simulated g versus V_D curves under different given V_G. It can be seen that the simulated g curve complies with the schematic diagram basically and the g curve shifts rightwards as V_G increases with the reason that V_G induces the change of φ_s.

Since I_{DMG} is in direct proportion to g, that is

$$I_{DMG} = rg, \tag{8}$$

where $r = aqN_{it}\sigma v_{th}$, a is the gate area, q is the single electron charge, N_{it} is the density of interface traps, σ is the cross section of a trap, and v_{th} is the thermal velocity, the variation of the I_{DMG} curve has the same trend as the g curve. Once V_G is given, I_{DMG} increases with V_D increasing at first and afterwards steps into saturation in which I_{DMG} cannot increase any more.

3. Results and discussion

Figure 3 shows the experimental I_{DMG} curves. For a given V_G, the I_{DMG} curve is almost zero at the beginning of V_D increasing from -0.2 V, then all of a sudden it augments. After exceeding its maximum, the curves start to drop with V_D increasing and finally present a peak shape. It can be seen that the curves shift rightwards and the peaks almost keep constant as V_G changes from 0.1 to 0.8 V. Figure 3 also shows the simulated I_{DMG} curves based on g in the Fig. 2(b). Compared with the simulated curve, the experimental curve is basically consistent with it from the inversion to depletion I state.

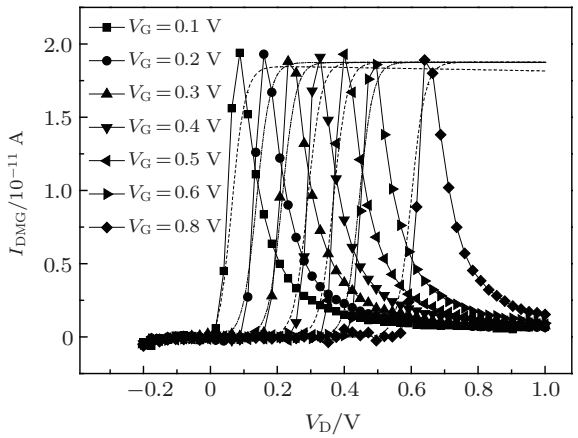


Fig. 3. Comparison of the experimental I_{DMG} (symbol line) and simulated I_{DMG} (dash line) based on Fig. 2(b). Here, $w/l = 6$ μm/0.35 μm. $N_{it} = 2 \times 10^{11}$ cm^{-2}, and $\sigma = 4 \times 10^{-13}$ cm^{-2}. Other structure parameters are the same as those in Fig. 2(b).

In order to better confirm the validity of the theory in depletion I state, we analyze the peak point which is the boundary point of depletion I state. Because I_{DMG} is proportional to g, g is the maximum at the I_{DMG} peak. At this peak, $n_s = n_i/5$. It defines V_{GP} and V_{DP} as the V_G and V_D corresponding to the I_{DMG} peak respectively. According to Eqs. (2) and (6), V_{GP} and V_{DP} have the following relationship:

$$V_{GP} - mV_{DP} = V_{FB} + \beta \ln \frac{5N_A}{n_i} - \frac{q\varepsilon_s N_A}{C_{ox}^2} + \frac{(2q\varepsilon_s N_A)^{1/2}}{C_{ox}} \times \sqrt{\frac{q\varepsilon_s N_A}{2C_{ox}^2} + V_{GP} - V_{FB} + V_{DP}}. \tag{9}$$

Since the third and fourth items in Eq. (9) are too small and can be ignored when $N_A < 10^{16}$ cm^{-3}, equation (9) can be simplified as

$$V_{GP} = mV_{DP} + V_{FB} + \beta \ln \frac{5N_A}{n_i}. \tag{10}$$

Figure 4 shows the relationship between V_{GP} and V_{DP} extracted from the experimental curves in Fig. 3. It can be seen that V_{GP} has a linear relationship with V_{DP}. The fitted equation is: $V_{GP} = sV_{DP}$, where $s = 1.24$, which agrees with Eq. (10) and s is very close to the value of m ($m = 1.25$) in the simulated curves in Fig. 3. Hence, the agreement fully proves the validity of the theory about the depletion state mentioned above. However, the experimental curve in Fig. 3 after reaching the peak cannot step into saturation like the simulated curve, but drops quickly with V_D increasing. This experimental result implies that the physical mechanism behind Fig. 2 does not hold in the depletion II state. Further, it can be deduced that the transport of interface generation current suffers some kind of inhibition after reaching the maximum value.

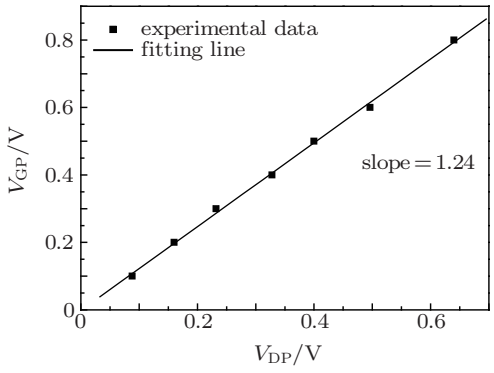


Fig. 4. Relationship between V_{GP} and V_{DP} extracted from the experimental I_{DMG} curves in Fig. 3.

To seek the real physical mechanism hidden in the I_{DMG} falling edge, figure 5(a) presents the conductance C_D of experimental I_{DMG} from Fig. 3. C_D can indicate the ability of V_D controlling I_{DMG}. It can be seen that there are two C_D peaks located in the rising edge and falling edge of I_{DMG}, C_{DRP} and C_{DFP}, respectively. All the C_{DRP} and C_{DFP} keep constant in Fig. 5(a). Obviously, V_G seems to have little influence on the C_D curve and just shifts the C_D curve rightwards. Namely, V_G cannot affect the ability of V_D controlling I_{DMG} curves. Thus the problem of V_D controlling the I_{DMG} curve can be transformed into that of the drain-gate voltage V_{DG} ($V_{DG} = V_D - V_G$)

controlling the I_{DMG} curve. The benefit of this transformation is to compress the group of I_{DMG} curves and to well make the implicit information present. Then, figure 5(b) presents the I_{DMG} curves under V_{DG}. V_{DG} at the I_{DMG} peak is defined as V_{DGP} and then $V_{DGP} = V_{DP} - V_{GP} = (1/s - 1)V_{GP} = -0.2V_{GP}$. Since V_{GP} is not beyond 0.8 V, the range of V_{DGP} is very small. Therefore, the current peaks are located at about $V_{DG} \approx 0$ V. In Fig. 5(b), the left side of the curve corresponds to the rising edge of the I_{DMG} versus V_D curve, and the right side corresponds to the falling edge of the I_{DMG} versus V_D curve. Because the difference between the simulation and experimental results in Fig. 3 is mainly focused on the falling edge of the V_D versus I_{DMG} curve, it needs to focus on the right side of the I_{DMG} versus V_{DG} curve. Further, ignoring the slight shift of the current peak, a common feature in all the curves is that the curves drop under $V_{DG} > 0$ V as V_{DG} increases. To sum up, V_{DG} controls the change of the falling edge of the experimental I_{DMG} curve in Fig. 3.

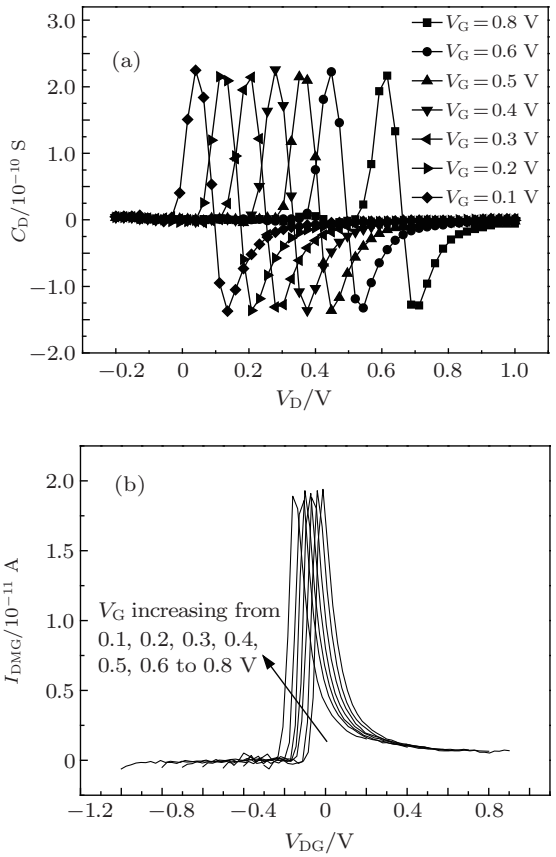


Fig. 5. (a) Conductance of the curves from Fig. 3, and (b) variations of the experimental I_{DMG} with V_{DG} extracted from Fig. 3.

Since V_{DG} is the drain-to-gate voltage drop, it affects the Si surface of the channel around the drain. Hence, the whole channel is divided into two regions: main channel region A and region B that is around the drain, as shown in Fig. 6. The generation rates of these two regions are g_1 and g_2, respectively. At a given V_G, the channel steps into depletion II state in Fig. 1 and the increase of V_D almost cannot change g_1. However, V_{DG} should increase with V_D increasing. As a consequence, the bending of the Si energy band at region B decreases and lessens the surface potential φ_s. When $p_s > n_i/5$ in region B, g_2 starts to decrease, as can be seen in Fig. 6(a). As V_D continues to increase, the channel depletion region returns to region A completely and an accumulation state can be formed in region B, as shown in Fig. 6(b). So the generation function of the interface traps in region B is shielded and g_2 is close to zero. The channel electrons created by the trap's generation are eventually collected by the drain. Based on the above discussion, the electron transport of the whole channel electron is subject to g_2. Namely, g_2 dominates the magnitude of the generation current. On the basis of the above discussion, g_2 should lessen with V_D increasing that is beyond V_{DP}. Thus, the generation current decreases. As V_D further increases, region B steps into the accumulation state, g_2 becomes zero, and the generation current disappears. As can be seen from Fig. 3, the experimental curves in the depletion II state just conform to this logical deduction.

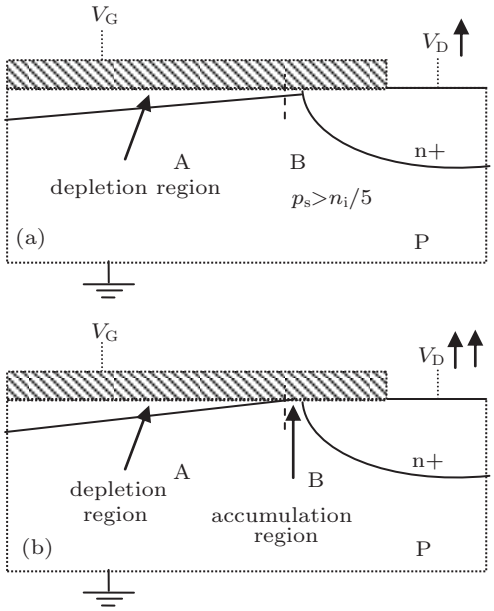


Fig. 6. Schematic diagrams of channel states as V_D varies. (a) Depletion situation of B region, and (b) accumulation situation of B region.

If the above theory of V_{DG} controlling the falling edge of I_{DMG} is reasonable, the generation current versus the V_{DG} curve should obey it no matter which measurement method is used. Figure 7(a) shows the curve of gate-modulated generation current I_{GMG} versus V_{DG}, which is obtained by scanning $V_G$with fixing V_D. It can be seen that the I_{GMG} curve changes from rising to falling when $V_{DG} > 0$ V. This phenomenon agrees with the case of I_{DMG}, which considerably indicates that the theory suits I_{GMG}. More, the curve of recombination current versus V_{DG} should present the same shape as the I_{DMG} curve because the recombination current also results from the SRH effect. Figure 7(b) shows the curve of the

gate-modulated recombination current I_{GMR} versus V_{DG} under $V_D < 0$ V. It can also be seen that the I_{GMR} curve firstly goes up and then drops when $V_{DG} > 0$ V. In general, the rationality of the theory is verified considerably by these two additional experiments above.

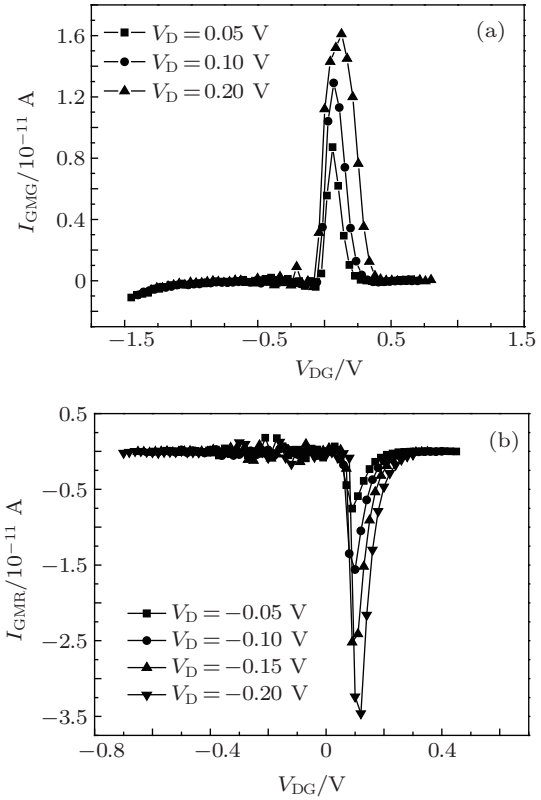


Fig. 7. (a) Variations of gate-modulated generation current (I_{GMG}) with V_{DG}, and (b) variations of gate-modulated recombination current (I_{GMR}) with V_{DG}.

On the basis of the theory's rationality, the variation of I_{DMG} in depletion II state is discussed in detail as follows. The gate-to-drain voltage drop V_{GD} dominates φ_s, the V_G in Eq. (3) should be substituted by V_{GD}. Due to $V_{GD} = -V_{DG}$, the surface potential around the drain corner φ_{SD} is

$$\varphi_{SD} = \frac{q\varepsilon_s N_A}{C_{ox}^2} + V_{GD} - V_{FB} - \frac{(2q\varepsilon_s N_A)^{1/2}}{C_{ox}} \sqrt{\frac{q\varepsilon_s N_A}{2C_{ox}^2} + V_G - V_{FB}}. \quad (11)$$

Thus, p_s is deduced as

$$p_s = p_0 \exp(-\varphi_{SD}/\beta), \quad (12)$$

which increases quickly after exceeding $n_i/5$ and then $p_s \gg n_i$ and $n_s \ll n_i$. Since p_s plays the dominant role in the falling stage of I_{DMG}, g_2 is simplified as

$$g_2 = \frac{n_i^2}{p_s + 2n_i} \approx \frac{n_i^2}{p_0} \exp(\varphi_{SD}/\beta) = n_0 \exp(\varphi_{SD}/\beta). \quad (13)$$

As mentioned before, the first and fourth terms of Eq. (11) can be ignored, then substituting Eq. (11) into Eq. (13), g_2 can be written as

$$g_2 = b \exp(-V_{DG}/\beta), \quad (14)$$

$$b = n_0 \exp[(-V_{FB})/\beta]. \quad (15)$$

In order to meet the practical devices, an additional accommodation-coefficient n is introduced in Eq. (14), then g_2 becomes

$$g_2 = b \exp[-V_{DG}/(n\beta)], \quad (16)$$

which indicates that g_2 decreases with V_{DG} increasing when V_G is given. According to Eq. (8), I_{DMG} also shows the exponential decay relationship with V_{DG}. Defining $I_0 = rb$, the theoretical model of I_{DMG} in the falling edge can be written as

$$I_{DMG} = I_0 \exp[-V_{DG}/(n\beta)]. \quad (17)$$

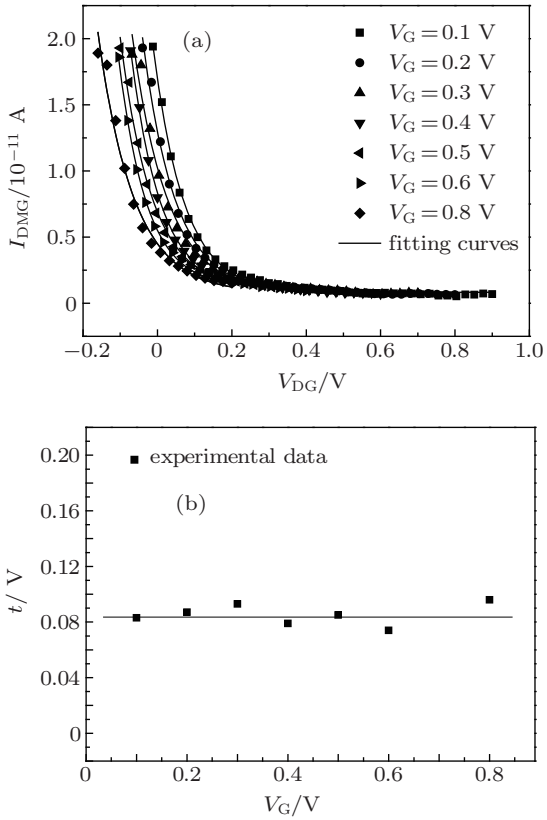


Fig. 8. (a) The falling edges of experimental and fitted I_{DMG} versus V_{DG} curves, and (b) variations of t with V_D extracted from panel (a).

In order to verify the correctness of Eq. (17), figure 8(a) extracts the experimental I_{DMG} curves at different fixed V_G from Fig. 5(b) and fits them. The expression obtained by the curve fitting is given by

$$I_{DMG} = c \exp(-V_{DG}/t), \quad (18)$$

with c and t the fitting coefficients. The experimental model of Eq. (18) mainly has the same form as the theoretical model of Eq. (17), in which I_{DMG} has the exponential attenuation relation with V_{DG}. To further test the matching degree of the theory and experiment, figure 8(b) extracts the fitting coefficient

t because t decides the degree of the exponential attenuation. As can be seen, t basically does not vary with the variation of V_G, which is about 0.08 V or 80 mV. Since the thermal potential $\beta = kT/q = 26$ mV, $t \approx 3\beta$. If $n = 3$ in Eq. (17), the decay degree with V_{DG} of Eq. (18) becomes the same as that of Eq. (17). Hence, the value of t verifies the reasonability of the theoretical model of Eq. (17). Further, this result fully shows the accuracy of the mechanism of V_{DG} controlling the falling edge of I_{DMG} proposed in the above sections.

4. Conclusions

The characteristics of the drain-modulated generation current I_{DMG} induced by interface traps in nMOSFETs are discussed. The change of V_D induces the changes of φ_s and thus changes n_s and p_s, which results in the formation of I_{DMG}. During this formation, the channel suffers from the inversion state, depletion I state to depletion II state as V_D increases with the given V_G. The results of experiment and simulation agree well with each other in the inversion and depletion I states. However, the simulated curve keeps constant and the experimental curve drops quickly when the channel steps into the depletion II state. It is found that the falling edge of the experimental I_{DMG} curve is close with the drain-to-gate voltage V_{DG}. Since V_{DG} affects the Si surface of the channel around the drain corner, the whole channel is divided into two regions: the main channel, region A, and region B, which is around the drain corner. The generation rate of region B is g_2 dominating the generation current. V_{DG} increases with V_D increasing, which lessens φ_s. Therefore, g_2 increases and results in the drop of the I_{DMG} curve. As V_D further increases, region B is into the accumulation state and then the generation function of the interface trap is screened by a large number of holes. Consequently, I_{DMG} disappears. The experiments of the gate-modulate generation and recombination currents are also applied to verify the reasonability of the above mechanism that is V_{DG} controlling the falling edge of the I_{DMG} curve. Based on this mechanism, a theoretical model is set up in which I_{DMG} has the exponential attenuation relation with V_{DG}. Finally, the fitting coefficient of the experimental curves t is extracted. It is found that $t = 80$ mV. These results fully show the accuracy of the above mechanism.

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