Normally-off metamorphic AlInAs/AlInAs HEMTs on Si substrates grown by MOCVD*

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A combination of self-aligned fluoride-based plasma treatment and post-gate rapid thermal annealing was developed to fabricate a novel 120-nm T-shaped gate normally-off metamorphic $Al_{0.49}In_{0.51}As/Ga_{0.47}In_{0.53}As$ HEMT device on a Si substrate grown by metal-organic chemical vapor deposition (MOCVD). A shift of the threshold voltage, from −0.42 V to 0.11 V was obtained and the shift can be effectively adjusted by the process parameter of CF_4 plasma treatment. Furthermore, a side benefit of reducing the leakage current of the device up to two orders of magnitude was also observed. E-mode transistors with 120 nm gate length own f_T up to 160 GHz and f_{max} of 140 GHz. These characteristics imply the potential of the fluoride-based plasma treatment technology for the fabrication of monolithic enhancement/depletion-mode mHEMTs, which also encourage the massive production with this low-cost technology.

Keywords: metamorphic AlInAs/AlInAs HEMTs, metal-organic chemical vapor deposition, normally-off, CF_4 plasma

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1. Introduction

Over the past decades, III–V materials are paid intensive and continuous attention as channel alternatives for n-FET in the future complementary metal oxide semiconductor (CMOS) technology. GaInAs, as a channel material, closely matches with InP, and have shown tremendous potential due to their high electron mobility and low power operations.[1,2] Recently, AlInAs/GaInAs high electron mobility transistors (HEMTs) on a Si substrate, which effectively take advantage of the high carrier drift velocity of GaInAs channel HEMT, the large wafer size, and the mechanical strength of Si substrate, are expected to be the most promising devices for high-speed and low-power digital logic applications in the future.[3,4] Moreover, AlInAs/GaInAs enhancement-mode (E-mode) HEMT can be integrated with the corresponding depletion-mode (D-mode) HEMT to form direct-coupled FET logic (DCFL) circuits in a simple circuit configuration, which can be combined with the mainstream Si-based CMOS process technology to implement ultra-high-speed and very-large-scale logic digital integrated circuits on Si substrate in the foreseeable future.[5] However, conventional GaInAs channel HEMT is a D-mode device, and the realization of high-performance E-mode devices will pave the way for fabrication of high-speed GaInAs channel E/D-mode CMOS-like DCFL circuits for digital applications. Therefore, most of the recent studies used different technologies, such as the gate-recess etching,[6] the buried-gate technology,[7,8] and fluorine-based plasma treatment[9–11] to develop E/D-mode AlInAs/GaInAs HEMTs on the same epi-wafer. However, the conventional gate recess process suffers the poor uniformity of threshold voltage (V_{th}) and controllability of etching depth, which is very important for the fabrication of digital circuits. Similarly, a gate-recess step is also required by the buried-gate technology, and the large leakage current is a challenging issue. Currently, many studies mainly reported the fluorine plasma treatment technology in AlGaN/GaN HEMTs on Si substrate, and few study in AlInAs/GaInAs HEMTs.

In this paper, in order to reduce the leakage current and improve the comprehensive DC and RF characteristics, a combination of self-aligned fluoride-based plasma treatment and post-gate rapid thermal annealing, which is a similar process to realize ultra-shallow junctions in advanced Si technology, was developed to realize an 120-nm E-mode AlInAs/GaInAs mHEMT on Si substrate. The effects of plasma immersion ion implantation (PIII) during the fluoride-based treatment were analyzed in detail. Finally, a significant reduction of the leakage current up to two orders of magnitude was successfully achieved. The V_{th} can be effectively shifted from −0.42 V to 0.11 V by adjusting the process parameter of CF_4 plasma treatment, and f_T of 160 GHz was obtained.

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2. Material growth and device fabrication

The schematic of epitaxial structure and TEM cross-section micrograph, including composite buffers, of the $Al_{0.49}In_{0.51}As/Ga_{0.47}In_{0.53}As$ metamorphic HEMT (mHEMT) is shown in Fig. 1. All layers were grown on 4-inch (001)-oriented semi-insulating Si substrates in an Aixtron AIX-200/4 MOCVD reactor. The Hall measurement of the grown material indicates that the two-dimensional electron gas (2-DEG) sheet carrier density is greater than 4.0×10^{12} cm^2 and the mobility is over 8000 cm^2/V·s at room temperature.

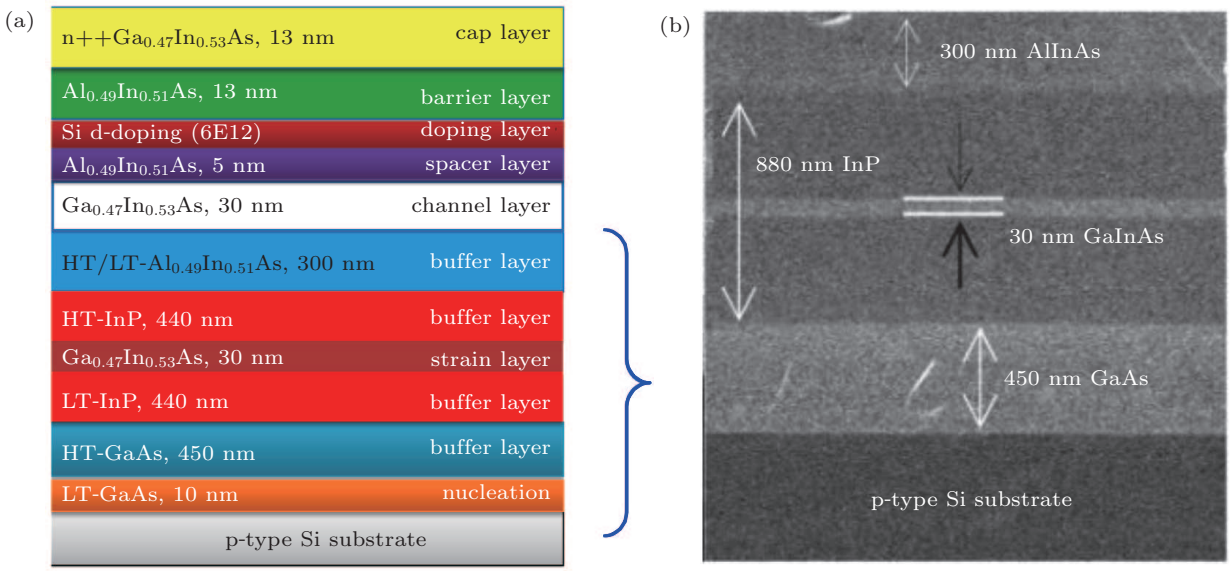


Fig. 1. (color online) (a) Nominal structure of mHEMT device on Si substrate (LT: low temperature; HT: high temperature. Note that the figure is not drawn to scale). (b) TEM cross-section micrograph of mHEMT buffer structure.

From bottom to top, the $Al_{0.49}In_{0.51}As/Ga_{0.47}In_{0.53}As$ mHEMT consists of a 10-nm GaAs nucleation layer, 450-nm HT-GaAs layer, 880-nm composite LT/HT InP-lattice-matched buffer layer grown at 500 °C/600 °C, 30-nm $Ga_{0.47}In_{0.53}As$ strain balance layer, 300-nm HT/LT-$Al_{0.49}In_{0.51}As$ buffer layer, 30-nm $Ga_{0.47}In_{0.53}As$ channel, 5-nm undoped $Al_{0.49}In_{0.51}As$ spacer layer, Si-delta-doping, 13-nm undoped $Al_{0.49}$ $In_{0.51}As$ Schottky layer, and 13-nm $Ga_{0.47}$ $In_{0.53}As$ cap layer heavily doped with Si (7×10^{18} cm^{-3}). A 30-nm thin $Ga_{0.47}In_{0.53}As$ lightly compressively-strained layer was introduced to balance the residual strain between HT/LT-InP buffer layer and HT/LT-$Al_{0.49}In_{0.51}As$ buffer layer in the composite buffer structure. The high-resolution x-ray diffraction (HRXRD) measurement was performed to obtain the full width at half maximum (FWHM) of the GaAs buffer of 328 arcsec and InP buffer of 320.3 arcsec. The good crystalline quality characterized by these FWHM values is important for the manufacture of good-performance devices. Moreover, the TEM cross-sectional image of the whole composite buffer layers shown in Fig. 1 clearly shows few misfit dislocations and smooth surface. 60-degree threading dislocations, obtained by the formula related with FWHM of the HRXRD measurement, were confined in the buffer and is comparable to our previous work.[12]

The combination of self-aligned fluoride-based plasma treatment and post-gate rapid thermal annealing was developed to fabricate an 120-nm E/D-mode AlInAs/GaInAs mHEMTs on Si substrate. Firstly, E/D-mode mHEMTs were isolated by wet chemical etching, followed by source/drain definition and ohmic metallization by evaporating Ni/Ge/Au/Ge/Ni/Au using an electron beam evaporator. Then a two-stage electron beam lithography technology was used to fabricate the 120-nm T-shape gate. SiN_x (100 nm) was deposited, followed by coating ZEP520 electron beam (EB) resist and the first EB exposure and development. Then SiN_x film is etched by $CHF_3/CF_4/O_2$ reactive ion etching (RIE) to define the gate footprint and mechanically supports the T-shaped gate. The second EB lithography was employed to form gate head pattern by bilayer polymethylmethacrylate/polymethylglutarimide (PMMA/PMGI) EB resist technology, which is similar to our previous work.[13] After the gate-recess etching with succinic-based acid to completely remove the highly doped $Ga_{0.47}In_{0.53}As$ cap layer and expose the $Al_{0.49}In_{0.51}As$ barrier layer, devices were treated by CF_4 plasma in an RIE system, followed by gate metallization and lift-off for the E-mode mHEMTs. The followed CF_4 plasma treatment can be directly processed in the $Al_{0.49}In_{0.51}As$ barrier layer and the F^- ions introduced by CF_4 plasma treatment can be effectively enhanced. Then the sample was annealed in nitrogen at 400 °C for 10 min to recover the plasma-induced

damages in $Al_{0.49}In_{0.51}As$ barrier and channel. This plasma treatment can effectively convert the treated devices from the D-mode to E-mode mHEMTs with proper CF_4 treatment parameters, and the magnitude of threshold voltage shift depends on the treatment conditions, such as plasma power and treatment time. The post-gate rapid thermal annealing has been found to have no effect on the threshold voltage shift introduced by the plasma treatment.[11] Finally, the electrodes of E/D-mode mHEMTs devices were followed by the e-beam evaporation of Ti/Au and lift off.

To characterize the surface morphology of gate-recess region, figure 2 shows atomic force microscope (AFM) images of device with and without CF4 plasma treatment across a scanned area of 10×10 μm^2. The corresponding root mean square (RMS) values are 2.16 nm and 2.76 nm, respectively. It can be found that devices suffer low surface damage during the CF_4 plasma treatment.

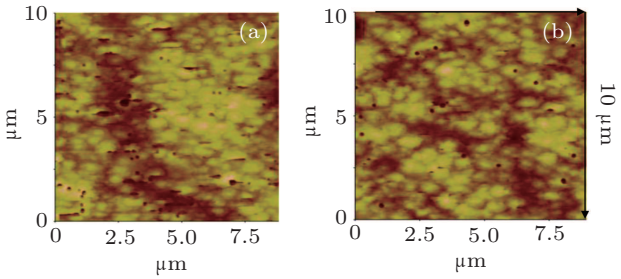


Fig. 2. (color online) The AFM picture of (a) sample a (without CF4 treatment) and (b) sample b (CF_4 treatment: 150 W/150 s).

To examine the distribution profile of negatively charged F^- ions introduced by CF_4 plasma treatment and ascertain how far the F^- ion tail extends, E/D mode HEMTs were probed by the secondary ion mass spectrum (SIMS) with and without the CF_4 plasma treatment. Figure 3 shows the SIMS measurement as a function of depth from the surface for sample a without CF_4 treatment and sample b treated by 150 W CF_4 treatment for 150 s, respectively. It can be found from Fig. 3 that the concentration of F atoms is the highest near the surface and drops by one order of magnitude in the channel. It can be deduced that the fluorine ions produced by the CF_4 plasma were mainly incorporated into the device surface and the fluorine ions can be neglected at the GaInAs channel layer.

The corresponding conduction-band profiles with and without the fluoride ions incorporated in AlInAs barrier layer is shown in Fig. 4, where the electric field formed from the immobile negatively charged F^- ions bends the conduction band in AlInAs barrier and causes an additional barrier height Φ_F. Conduction band in the GaInAs channel layer is over the Fermi level, which makes the 2-DEG completely depleted and converts HEMT from D-mode to E-mode. Moreover, the raised barrier height Φ_F effectively enhances the gate Schottky barrier height, resulting in the significant suppression to the reverse and forward current of gate Schottky diode of AlInAs/GaInAs HEMT.

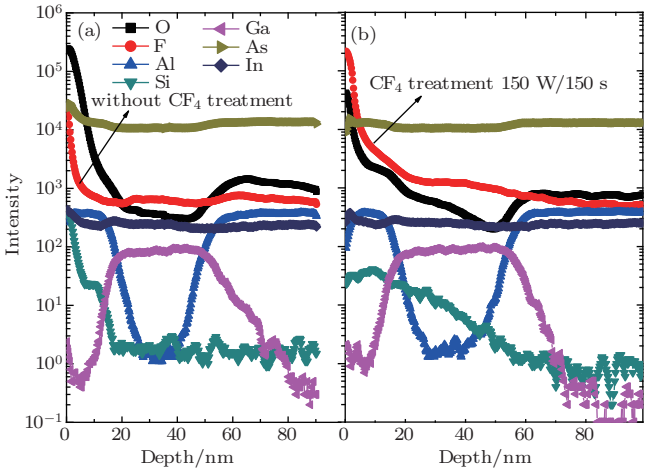


Fig. 3. (color online) The SIMS measurements of (a) sample a (without CF_4 treatment) and (b) sample b (CF_4 treatment: 150 W/150 s).

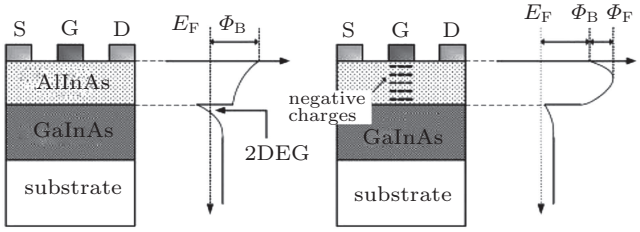


Fig. 4. Diagram of the band structure with fluoride-based plasma treatment.

3. Results and discussion

Typical current–voltage (I–V) and transfer characteristics of $Al_{0.49}In_{0.51}As/Ga_{0.47}In_{0.53}As$ mHEMTs on Si substrate with and without CF_4 plasma treatment are measured by HP4156A semiconductor parameter analyzer, as shown in Fig. 5. The maximum drain current (I_{DSmax}) was 560 mA/mm for D-mode mHEMT and 220 mA/mm for E-mode mHEMT treated by CF_4 plasma at power of 150 W for 150 s at $V_{GS} =$ 0.6 V and $V_{DS} = 1.5$ V. The reduction of I_{DSmax} for E-mode mHEMT is largely attributed to the reduction of the channel electrons partly depleted from immobile F^- ions at the same biased voltage. The V_{th} is extracted by the linear extrapolation of drain current at gate bias corresponding to the peak transconductance (g_m) in I_{DS}–V_{GS} transfer characteristics, and the V_{th} of D-mode mHEMT is -0.42 V, while it is 0.11 V for E-mode mHEMT. Similarly, these immobile negative charges is incorporated into the AlInAs barrier during the CF_4 plasma treatment and the channel electron is effectively depleted, resulting in the shift of V_{th}.[10] The peak g_m was 760 mS/mm for the D-mode mHEMT and 330 mS/mm for the E-mode mHEMT at $V_{DS} = 1.0$ V. It should be noted that the fluoride ions might get implanted to reach the channel so that the saturation current of the E-mode HEMT dropped to about 50% of the original value in the untreated D-mode HEMT. Therefore,

CF_4 treatment and the barrier thickness should be further optimized to improve the saturation drain current and the peak g_m of the E-mode HEMT.

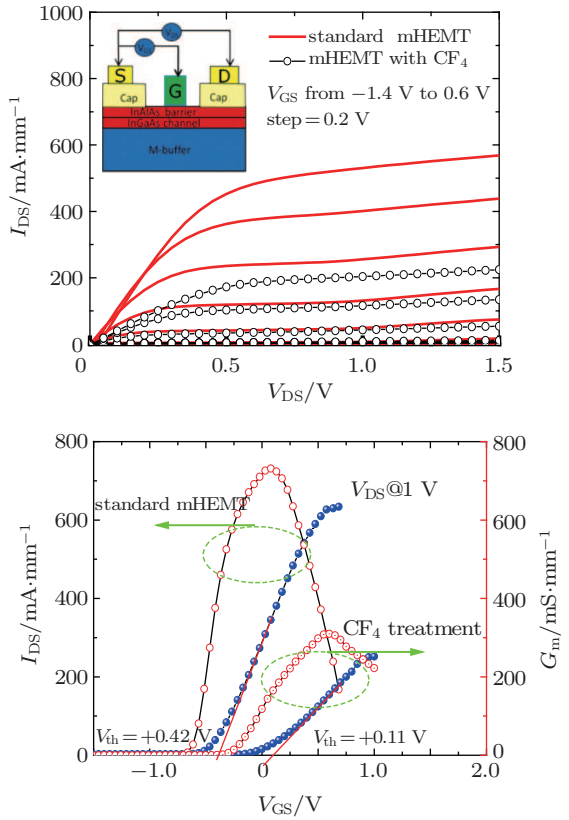


Fig. 5. (color online) *I–V* transfer and output characteristics of mHEMTs after different CF_4 plasma treatment conditions.

The dependence of V_{th} on the power of CF_4 plasma treatment is shown in Figs. 6(a) and 6(b), where the shift of V_{th} increases as the plasma power increases. The shift characteristics of V_{th} is attributed to the fact that the increased plasma power makes the ionization rate of CF_4 enhanced, resulting in the increase of F^- ions, and makes the diffusion depth of F^- ions be closer to the GaInAs channel, resulting in the effective depletion of 2-DEG in the channel.[11] Moreover, the linear relation between the shift of V_{th} and plasma power indicates that the precise control on V_{th} can be achieved in the fabrication process. However, as shown in Fig. 6(b), the native doping ions induced by MOCVD sometimes restrict the shift in V_{th}, resulting in some "quasi-zero" V_{th} in process, which is harmful to integration of E/D-mode HEMT to form DCFL circuits with CF_4 treatment technique. Thus, the combination of CF_4 treatment with the "gate sinking" method, which in fact demonstrates great potency, should be further studied.[14]

The gate current of AlInAs/GaInAs mHEMTs after CF_4 plasma treatments at different RF powers is shown in Fig. 6(c). The reverse-biased gate leakage currents were dramatically reduced after CF_4 plasma treatment at power of 150 W for 120 s. The gate leakage current is reduced by two orders of magnitude at $V_{GS} = -3$ V due to the fact that the raised gate Schottky barrier height Φ_F introduced by implanted F^- ions suppresses the gate current.

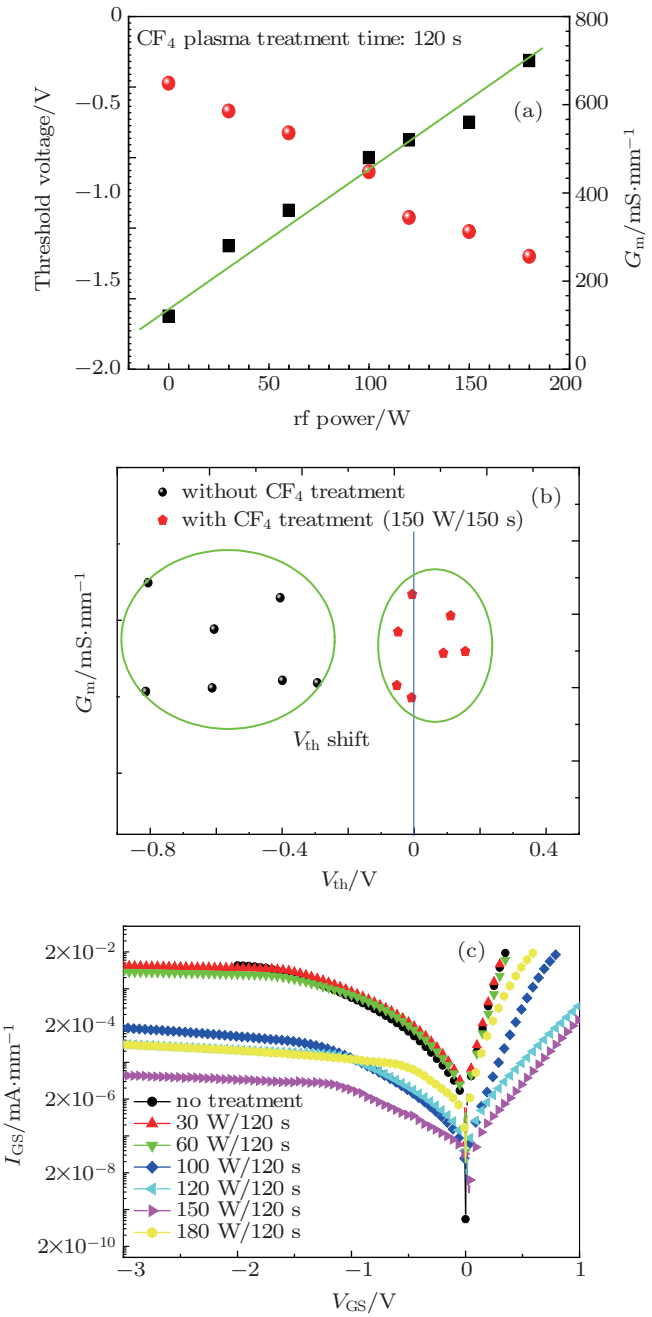


Fig. 6. (color online) (a), (b) Dependence of AlInAs/GaInAs mHEMT V_{th} on CF_4 plasma power. (c) Reverse- and forward-baised gate current of AlInAs/GaInAs mHEMTs with different CF_4 plasma treatments.

The RF performance of the devices was assessed using on-wafer small signal *S*-parameter measurements on 0.12×100 μm^2 mHEMTs on Si substrate by cascade microtech probes and an HP8722 network analyzer from 0.1 to 39.1 GHz. On-wafer open and short de-embedding structures were used to determine the parasitic capacitance of the probe pads and to de-embed the short-circuit current gain $|H_{21}|$. The current-gain cutoff frequency (f_T) and the maximum available gain (f_{max}) were calculated by extrapolating at −6 dB per octave. As shown in Fig. 7, f_T/f_{max} was about 190/140 GHz for

D-mode mHEMT and 160/140 GHz for the E-mode mHEMT treated by the combination of post-gate rapid thermal annealing process and the CF_4 plasma treatment with an power of 150 W for 120 s. Obviously, the RF characteristics suffer low degradation, and post-gate annealing effectively recovers the 2-DEG mobility degraded by the plasma treatment. So the self-aligned CF_4 plasma treatment incorporated with proper post-gate annealing process is necessary for fabricating high-performance RF E-mode AlInAs/GaInAs mHEMT on Si substrate.[15]

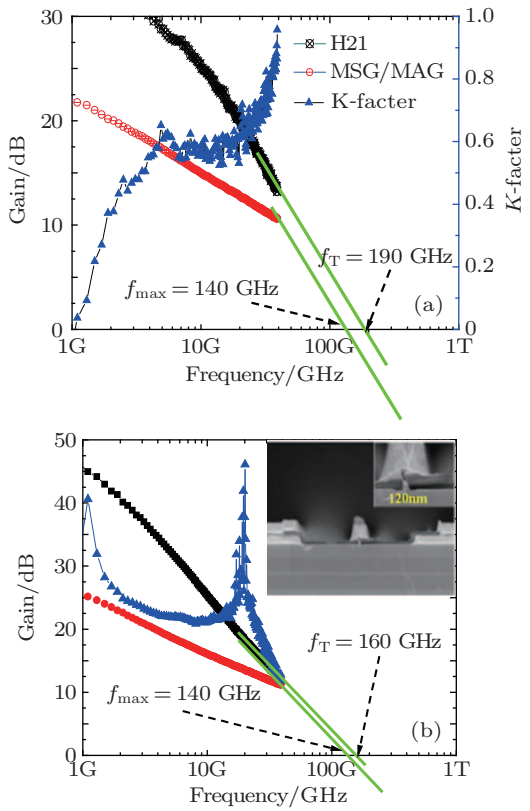


Fig. 7. (color online) Small signal RF characteristics f_T and f_{max} with (a) and without (b) CF_4 plasma treatment.

4. Conclusion

A self-aligned CF_4 plasma treatment technique was successfully developed to fabricate AlInAs/GaInAs mHEMTs on Si substrate by MOCVD, and the dramatically reduced leakage current and the significant threshold voltage shift from D-mode to E-mode were obtained due to the negatively charged fluorine ions incorporated in the AlInAs barrier layer during the CF_4 plasma treatment. The post-gate rapid thermal annealing process was combined to recover 2-DEG mobility degraded by the plasma treatment, and E-mode device suffers low surface-damage and a good RF performance was effectively obtained. The nearly linear relation between the shift in V_{th} and plasma power implies the possibilities of the fabrication of monolithic E/D-mode mHEMTs and ultra-high-speed and large-scale DCFL logic digital integrated circuits on Si substrate with the low-cost technology developed.

References

[1] Xu J B, Zhang H Y, Fu X J, Guo T Y and Huang J 2010 *Chin. Phys. B* **19** 037302
[2] Javier M L, Tomas G, Danie P, Sylvain B, Thierry P and Alain C 2004 *IEEE Trans. Electron Dev.* **51** 521
[3] Lin Y C, Yamaguchi H, Chang E Y, Hsieh Y C, Ueki M, Hirayama Y and Chang C Y 2007 *Appl. Phys. Lett.* **90** 023509
[4] Li Q, Zhou X J, Tang C W and Lau K M 2013 *IEEE Trans. Electron Dev.* **60** 4112
[5] Suehiro H, Ohori T, Nakasha Y, Miyata T, Watanable Y, Kuroda S and Takikawa M 1994 *International Electron Devices Meeting,* December 11–14, 1994, San Francisco, CA, USA, p. 903
[6] Dumka D C, Tserng H Q, Kao M Y, Beam E A and Saunier P 2003 *IEEE Electron Dev. Lett.* **24** 135
[7] Chen K J, Enoki T, Maezawa K, Arai K and Yamamoto M 1996 *IEEE Trans. Electron Dev.* **43** 252
[8] Kim S and Adesida I 2006 *IEEE Electron Dev. Lett.* **27** 873
[9] Ma X H, Yu H Y, Quan S, Yang L Y, Pan C Y, Yang L, Wang H, Zhang J C and Hao Y 2011 *Chin. Phys. B* **20** 027303
[10] Cai Y, Zhou Y G, Lau K M and Chen K J 2006 *IEEE Trans. Electron Dev.* **53** 2207
[11] Cai Y, Cheng Z Q, Tang C W, Lau K M and Chen K J 2006 *IEEE Trans. Electron Dev.* **53** 2223
[12] Li H, Tang C W and Lau K M 2008 *IEEE Electron Dev. Lett.* **29** 561
[13] Huang J, Guo T Y, Zhang H Y, Xu J B, Fu X J, Yang H and Niu J B 2010 *Chin. Phys. Lett.* **27** 118502
[14] Kim D H and Alamo J A 2008 *IEEE International Electron Devices Meeting*, December 15–17, 2008, San Francisco, CA, USA, p. 1
[15] Cai Y, Zhou Y G, Chen K J and Lau K M 2005 *IEEE Electron Dev. Lett.* **26** 435