Temperature-dependent bias-stress-induced electrical instability of amorphous indium-gallium-zinc-oxide thin-film transistors*

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The time and temperature dependence of threshold voltage shift under positive-bias stress (PBS) and the following recovery process are investigated in amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistors. It is found that the time dependence of threshold voltage shift can be well described by a stretched exponential equation in which the time constant τ is found to be temperature dependent. Based on Arrhenius plots, an average effective energy barrier $E_{\tau\text{stress}} = 0.72$ eV for the PBS process and an average effective energy barrier $E_{\tau\text{recovery}} = 0.58$ eV for the recovery process are extracted respectively. A charge trapping/detrapping model is used to explain the threshold voltage shift in both the PBS and the recovery process. The influence of gate bias stress on transistor performance is one of the most critical issues for practical device development.

Keywords: amorphous indium gallium zinc oxide, thin-film transistors, positive bias stress, trapping model, interface states

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1. Introduction

Recently, thin-film transistors (TFTs) based on amorphous oxide semiconductors have received a great deal of interest as a potential backplane technology for next generation display applications. In particular, amorphous indium-gallium-zinc-oxide (a-IGZO), first proposed by Hosono *et al.* in 2004[1] and intensively developed across the world ever since,[2–7] is regarded as the most promising oxide material for making TFT channels. Compared with traditional semiconductors such as amorphous silicon (a-Si) and recently developed organic channel materials, a-IGZO has shown readily apparent advantages including high electron mobility, good uniformity, low processing temperature and high optical transparency to visible light.[1,8]

For practical TFT applications, instability suffering from conditions such as gate-bias stress and visible-light illumination must be minimized. Although there have been some reports on the instability behaviors of a-IGZO TFTs,[9–12] the underlying mechanisms responsible for electrical instability, which are likely strongly dependent on detailed processing parameters, are still controversial. In the present work, the effect of positive-bias stress (PBS) on threshold voltage instabilities of a-IGZO TFTs as well as the following recovery behavior when the devices are left unbiased are studied as a function of time. The threshold voltage shift occurring in both the PBS and the recovery process is found to be strongly temperature dependent. The corresponding effective energy barriers are extracted and compared with the related data in the literature. The experimental results support a conclusion that charge trapping/detrapping between the gate insulator and the a-IGZO channel is the major mechanism for PBS instability.

2. Experiment

The a-IGZO TFTs tested in this work are fabricated on heavily doped n-type silicon substrate, which serves as the back gate. A 200-nm SiO_2 gate insulator layer is first deposited on the wafer's front side by plasma enhanced chemical vapor deposition at 300 °C. A 50-nm a-IGZO active layer is then deposited by dc sputtering at room temperature. The ceramic IGZO target used is composed of In_2O_3:Ga_2O_3:ZnO = 1:1:1 in mole ratio and the oxygen content of the Ar+O_2 mixture gas is maintained at 15% during sputtering. Afterward, the active region is defined by photolithography and wet chemical etching. Next, a Ti/Au (30 nm/70 nm) bi-layer is deposited by e-beam evaporation and patterned as the source/drain contact electrodes. The effective channel region is formed as 100-μm in width and 20-μm in length. Finally, all device samples are subjected to thermal annealing at 300 °C in air for 1 h.

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To study the electrical instability behaviors of a-IGZO TFTs, the influence of PBS on threshold voltage shift and the following recovery process after PBS are examined as a function of time. Positive gate bias stress of 30 V is applied with both the source and the drain electrodes of the TFT grounded. At selected times, the bias stress is interrupted and the transfer characteristics of the TFT are quickly measured with $V_{DS} = 0.1$ V. All electrical stress and I–V measurements are conducted in darkness by using a Keithley 2612 SourceMeter. The recovery process is monitored by measuring the transfer curves at fixed times after 3000 s PBS at 30 V. To further investigate the temperature dependent electrical instability, the same measurements are repeated at different ambient temperatures ranging from 30 °C to 90 °C.

3. Results and discussion

Figure 1 shows the evolution of transfer curves of the a-IGZO TFT as a function of PBS time. The curves continuously shift in the positive direction. After 3000 s PBS, the amount of threshold voltage shift reaches about 3.58 V. Here the threshold voltage (V_{th}) of the TFT is defined as the gate voltage (V_{GS}) value where the drain current (I_{DS}) rises to 10 nA in a transfer curve. In spite of the large threshold voltage shift (ΔV_{th}), the subthreshold swing (SS) of the TFT remains almost constant at about 0.58±0.07 V/dec, while there is also no apparent variation of field-effect mobility (μ_{FE}) with a nearly constant value of ~10.5±0.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$.

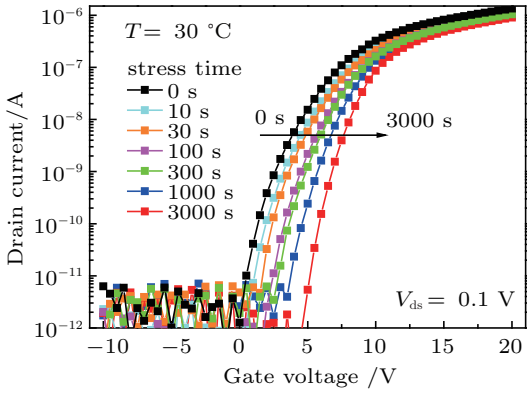


Fig. 1. (color online) Transfer characteristics of the a-IGZO TFT under PBS stress as a function of stress time.

The amount of ΔV_{th} as a function of time measured at various temperatures is shown in Fig. 2(a). It is found that the time dependence of ΔV_{th} can be fitted with a stretched-exponential equation[9]

$$\Delta V_{th} = \Delta V_{tho} \left\{ 1 - \exp\left[-(t/\tau)^{\beta} \right] \right\}, \quad (1)$$

where τ denotes a time constant, β is a stretched-exponential exponent, and ΔV_{tho} is the ΔV_{th} at infinite stressing time. The fitting curves are also shown (solid) in Fig. 2(a). Through numerical fitting, a value of 1.8×10^6 s for τ at 303 K is deduced. It is further found that τ is strongly temperature dependent and decreases at higher temperatures, indicating that the stress-induced instability behavior is thermally activated.

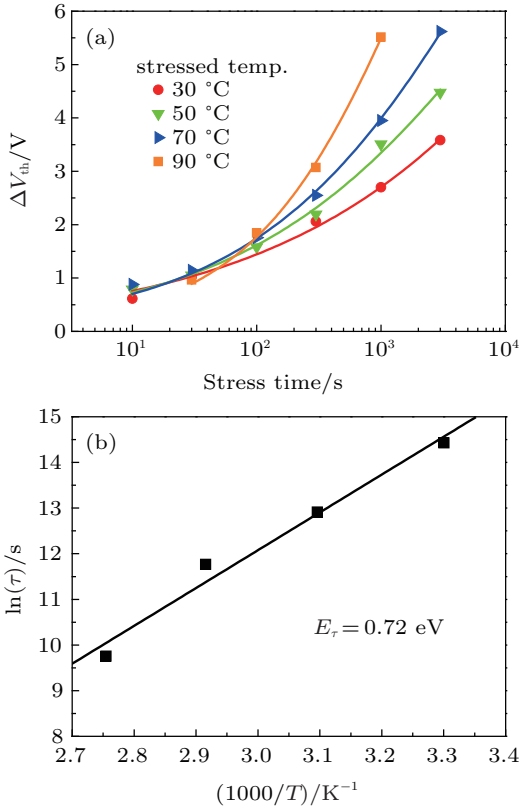


Fig. 2. (color online) (a) Time dependence of V_{th} shift at different stress temperatures. The measured data are well fitted with a stretched-exponential equation. (b) Stress time constant lnτ as a function of reciprocal temperature.

Figure 2(b) shows the evolution of lnτ as a function of reciprocal temperature. As it is a typical thermally activated process, the data points can be linearly fitted by using the following equation:[9]

$$\tau = \tau_0 \exp\left(E_\tau / k_B T\right), \quad (2)$$

where E_τ is the average effective energy barrier, τ_0 is a prefactor, T is the absolute temperature and k_B is the Boltzmann constant. The good linear dependency of the data points indicates that the thermally activated process is governed by a consistent effective energy barrier E_τ. An E_τ of ~0.72 eV is derived for the PBS process, which must be related to the microscopic nature of the trap sites.

In applications such as active matrix displays, the TFT would be switched on and off occasionally. The generated V_{th} shift by PBS relaxes in the off-state. Thus, the recovery behavior after stress is also important for investigation. Figure 3 shows the recovery behavior of the TFT at 70 °C after 3000 s PBS at 30 V. It is clear that the transfer curves shift negatively

toward the initial state while their subthreshold slopes remain almost the same.

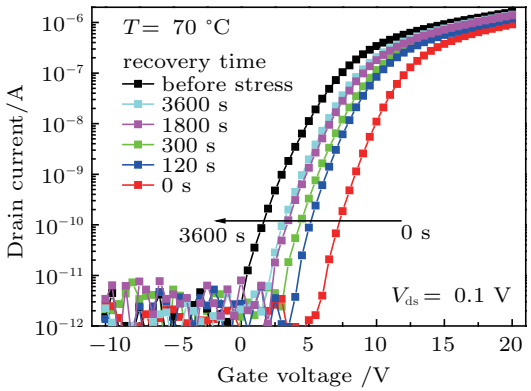


Fig. 3. (color online) Transfer characteristics of the a-IGZO TFT at 70 °C as a function of recovery time after 3000 s PBS at 30 V.

Figure 4(a) shows the time dependence of the $V_{\rm th}$ shift during the recovery process at various temperatures. Still, the data can be fitted with the stretched-exponential equation

$$\Delta V_{\rm th} = \Delta V_{\rm th_max} \exp\left[-(t/\tau)^{\beta}\right], \tag{3}$$

where $\Delta V_{\rm th_max}$ is the $\Delta V_{\rm th}$ right before the relaxation begins. A value of 3.0×10^4 s for time constant τ at 303 K is derived, which is two orders of magnitude smaller than the time constant for the PBS process. Based on an Arrhenius plot and numerical fitting similar to that shown in Fig. 4(b), an average effective energy barrier E_τ of 0.58 eV is calculated for the recovery process, which is smaller than the effective energy barrier of the PBS process, indicating the recovery process is less temperature sensitive.

Previous studies on oxide semiconductor TFTs have concluded that there are two main mechanisms responsible for electrical instability.[13–16] One is carrier trapping at defect states, and the other is point defect generation, which would consequently change the subthreshold swing.[15,16] In the present case, there is no apparent change of SS and $\mu_{\rm FE}$, indicating that during the PBS and the following recovery process, creation of additional defect states is negligible. Thus, the PBS-induced $V_{\rm th}$ shift must be caused by the trapping of electrons at the existing interfacial trapping states, which partially screens the applied gate bias and makes the effective gate voltage smaller. As the electron trapping process is reversible, it can be easily understood that the recovery of the transfer curves without gate bias stress must be due to electron detrapping from interfacial states.

Based on the above, the carrier trapping mechanisms under PBS stress can be described as follows: under high positive gate bias, the Fermi level along the device channel moves above the mobility edge, and carriers within a-IGZO channel accumulate at the semiconductor/gate insulator interface.[17] As temperature increases, the Fermi level moves up further due to the enhanced dopant ionization effect and meanwhile, more carriers are thermally activated above the Fermi level. As a result, the rate for carriers to overcome the effective energy barrier and to be trapped at the interfacial states is enhanced, leading to a decreased characteristic time constant τ at higher temperatures.

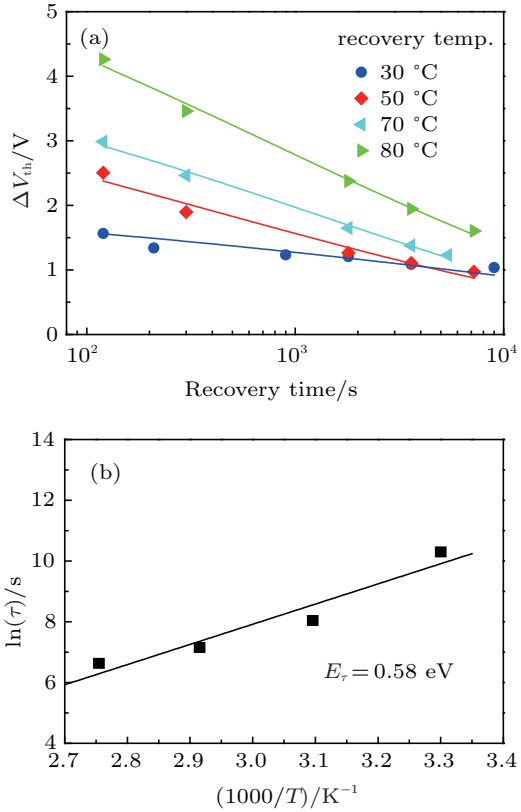


Fig. 4. (color online) (a) Time dependence of $V_{\rm th}$ shift at different recovery temperatures. The measured data are well fitted with a stretched-exponential equation. (b) Recovery time constant $\ln\tau$ as a function of reciprocal temperature.

The time constants and activation energies extracted in this work are summarized in Table 1 along with similar parameters reported in the literature. Compared with the past reports, the device fabricated in this work features larger time constants and higher activation energies of electrical instability in both the PBS and the recovery process. The relatively better device stability is likely caused by the application of a slightly higher oxygen partial pressure of $O_2/(O_2+Ar)$ =15% during the a-IGZO deposition process. The high oxygen partial pressure during sputtering deposition usually enables the a-IGZO film to have a lower concentration of oxygen vacancies and possibly better interface quality. Further comparative reliability study of a-IGZO TFTs deposited and annealed at different oxygen partial pressures will be conducted in future work. Here it should be noted that the overall time constants of the performance shift of a-IGZO TFTs are still much smaller than those of a-Si:H and microcrystalline Si TFTs (see Table 1), indicating that the interface quality of the current a-IGZO TFTs is still poor and has to be significantly improved.

Table 1. Summary of characteristic time constant E_τ and effective energy barrier E_τ of PBS-induced electrical instability for a-IGZO TFTs, as well as for Si-based TFTs. The key processing parameters of the a-IGZO TFTs are also listed.

Active layer/gate dielectric/post annealing in air	Operation condition	τ@RT/s	E_τ/eV	Ref.
IGZO 15%P_{O_2}, SiO_2[a], annealed @300 °C	stress	1.8×10^6	0.72	this work
	recovery	3×10^4	0.58	
IGZO 6.7%P_{O_2}, SiO_2[a], annealed @330 °C	stress	7×10^5	0.38	Ref. [11]
	recovery	7×10^2	0.23	
IGZO 0%P_{O_2}, SiO_2[a], annealed @200 °C	stress	1.2×10^5		Ref. [10]
	recovery	4×10^2		
IGZO 0%P_{O_2}, SiO_2[a], no annealing	stress	1.4×10^3		Ref. [10]
	recovery	4×10^4		
IGZO 0%P_{O_2}, SiO_2[b], annealed @200 °C	stress	3×10^5	0.68	Ref. [10]
IGZO 0%P_{O_2}, SiO_2[b], annealed @300 °C	stress	2×10^4	0.53	Ref. [9]
IGZO 0%P_{O_2}, SiO_2[b], annealed @300 °C	stress	2×10^4		Ref. [18]
	recovery	3×10^5		
Amorphous silicon	stress	8×10^7	0.98	Ref. [19]
	recovery	5×10^9	1.1	
Microcrystalline silicon	stress	10^{12}	1.07	Ref. [20]

Note: the notation P_{O_2} means the oxygen partial pressure during a-IGZO deposition. [a]grown by PECVD; [b]grown by thermal oxidation.

The corresponding schematic energy band diagrams of charge trapping and detrapping processes are presented in Fig. 5. Figure 5(a) shows that during the PBS process, electrons accumulate at the channel/dielectric interface. Then through thermionic-field emission, electrons need to overcome an average effective energy barrier of 0.72 eV to be injected into the trap states at the near interface of the gate insulator. In detail, the thermionic-field emission process must include thermal activation, subsequent tunneling and then possible relaxation to the lower energy interface states. Figure 5(b) shows that during the un-biased recovery process, the trapped electrons could be thermally activated and emitted back into a-IGZO channel. The extracted E_τ of 0.58 eV is the average effective energy barrier that the trapped electrons need to overcome.

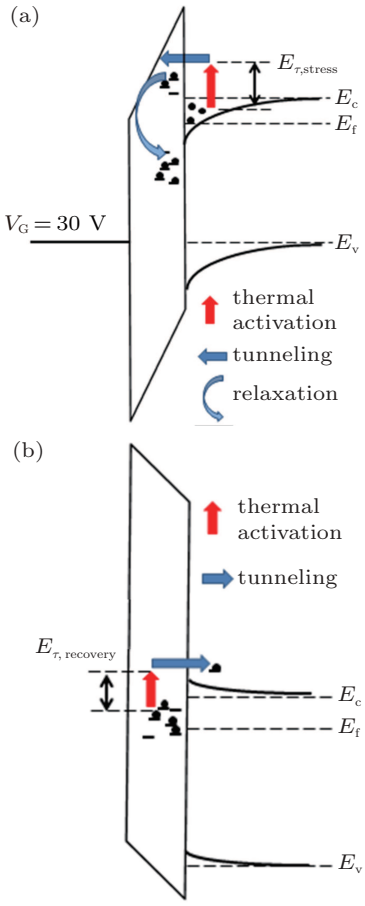


Fig. 5. (color online) Schematic energy band diagram of (a) the stress process and (b) the recovery process. Here, E_c is the conduction band minimum, E_f is the Fermi level, and E_v is the valence band maximum.

4. Conclusion

In summary, the effect of positive gate bias stress on a-IGZO TFTs and the following recovery process are investigated as a function of time and at various temperatures. It is found that the time dependence of the V_{th} shift can be described by a stretched exponential equation. Effective energy barriers of 0.72 eV for the stress process and 0.58 eV for the recovery process are extracted. Interfacial carrier trapping and detrapping are confirmed as the major mechanisms for the threshold voltage shift during the PBS and the recovery process.

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