Threshold switching uniformity in In_2Se_3 nanowire-based phase change memory*

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The uniformity of threshold voltage and threshold current in the In_2Se_3 nanowire-based phase change memory (PCM) devices is investigated. Based on the trap-limited transport model, amorphous layer thickness, trap density, and trap depth are considered to clarify their influences upon the threshold voltage and threshold current through simulations.

Keywords: phase change memory, nanowire, trap-limited model, threshold voltage

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1. Introduction

One of the most promising candidates of storage class memory (SCM)[1–4] is the phase change memory (PCM) for its excellent endurance, long retention, faster write speed and scaling capability.[5–8] PCM operates on the principle of threshold switching associated with the reversible phase change between the crystalline and amorphous states.[9,10] The switching threshold voltage and current are not constant values and have a variation in different programming cycles. The uniformity of the threshold voltage and threshold current[11,12] is extremely important for the PCM operation since they mark the boundary between the read and programming regime of the memory, especially for the future ultra-low voltage devices.[13,14] Uniformity of threshold switching is both affected by device-to-device process induced variability and intra-device programming induced variability. Many studies have been done on the physics of threshold switching[15,16] and the trap-limited transport model[22,23] is currently widely used to explain most of the intra-device programming characteristics including threshold switching phenomenon. However, there have been a limited number of reports which provided clear explanations of the relationship between different localized states and the uniformity of threshold switching. In order to understand the physics behind the threshold switching uniformity, factors related to the localized states such as amorphous thickness, trap density, and trap depth should be investigated to explain the influences on the uniformity.

PCM in the form of nanowire[17–20] allows the size of the centralized phase change region to be controlled, which offers a better method to investigate the threshold uniformity mechanism. Among the phase change materials, In_2Se_3 is more promising since it exhibits higher resistivity than GeTe or $Ge_2Sb_2Te_5$ and its resistivity can be varied by a factor of 10^5 which enables the multilevel applications.[21] Besides, the programming power for the RESET operation of the nanowire-based In_2Se_3PCM is only tens of microwatts compared to the milliwatt power levels required by the conventional thin-film-based PCM.[18] In this paper, we focused on the intra-device threshold parameters characterization and analysis in nanowire-based In_2Se_3PCM. The experimental data were collected from the same nanowire device to avoid the device-to-device process induced variability on the threshold switching. First, the RESET operation was accomplished to get the amorphous state. Then we extracted threshold voltage V_{th} and threshold current I_{th} from multiple I–V measurement and the Weibull cumulative distribution was used to study the uniformity issue. Based on the trap-limited transport model, simulations were used to clarify three factors (amorphous thickness U_a, trap density N_t, and trap depth E_t) influences on the V_{th} and I_{th}.

2. Device structure and threshold switching uniformity

In_2Se_3 nanowires was synthesized[18] using vapor–liquid–solid technique with a diameter of 30 nm. The electrodes material was Pt and the insulator material was SiO_2. As is shown in Fig. 1, conventional PCM[7] consists of a top electrode and a bottom electrode, the phase change material layer is sandwiched between the two electrodes. The nanowire-based PCM consists of a top electrode and a bottom electrode with the phase change material nanowire placed between the two electrodes, which is surrounded by dielectric material. Different from the conventional thin-film-based phase change memory, the active part of the phase change material is in the middle of the nanowire.

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Table 1. Parameters used in the simulation.

Parameters	Values	Parameters	Values	Parameters	Values
Nanowire width	30 nm	BE thickness	30 nm	Pt thermal conductivity	71.6 $W\cdot m^{-1}\cdot K^{-1}$
TE width	70 nm	SiO_2 electrical resistivity	1×10^{14} $\Omega\cdot m$	Pt thermal capacity	2.8×10^{6} $J\cdot m^{-3}\cdot K^{-1}$
BE width	70 nm	SiO_2 thermal conductivity	1.4 $W\cdot m^{-1}\cdot K^{-1}$	In_2Se_3 electrical resistivity	670 $\Omega\cdot m$
Nanowire length	200 nm	SiO_2 thermal capacity	3.1×10^{6} $J\cdot m^{-3}\cdot K^{-1}$	In_2Se_3 thermal capacity	0.27 $J\cdot g^{-1}\cdot K^{-1}$
TE thickness	30 nm	Pt electrical resistivity	1.06×10^{-7} $\Omega\cdot m$	In_2Se_3 thermal conductivity	50 $W\cdot m^{-1}\cdot K^{-1}$

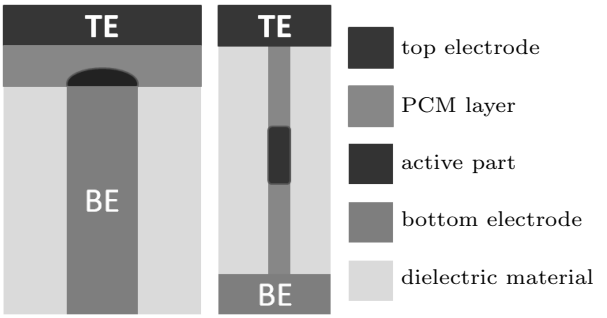


Fig. 1. Schematic diagram of a conventional thin-film-based phase change memory device and NWs PCM.

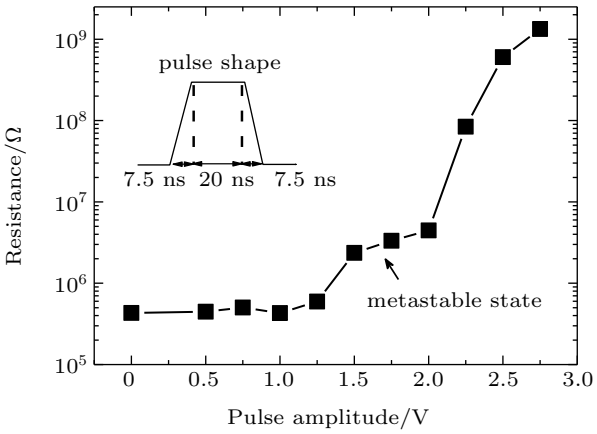


Fig. 2. Measured resistance with increasing RESET pulse amplitude for the cell in the initial crystalline state.

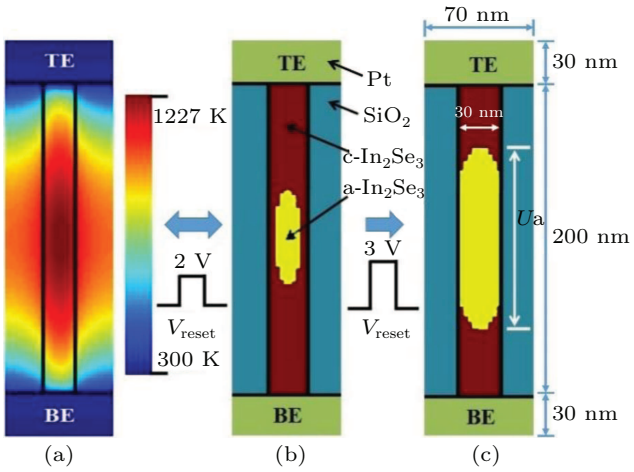


Fig. 3. (color online) (a) Simulated temperature distribution in a nanowire-based memory device with 2-V RESET pulses and (b) the corresponding phase distribution. (c) Amorphous thickness U_a grows as the RESET pulse amplitude increases to 3 V.

Figure 2 shows the measured resistance as a function of the variable RESET pulse amplitudes. Resistance for the initial crystalline state remains low until RESET pulse amplitude is close to 2.75 V, when PCM turns from low resistance state (LRS) to the high resistance state (HRS). ANSYS was used to simulate the temperature and amorphous distribution after the RESET operation. The corresponding parameters are listed in Table 1. Figure 3(a) shows the simulated temperature distribution within a nanowire-based memory device during 2-V RESET pulse. From the results, we can see that the highest temperature region is in the middle of the nanowire structure, which is 1227 K above the melting point ($T_m = 953$ K[21]) of In_2Se_3 material. Figure 3(b) shows the corresponding formed amorphous region (a-In_2Se_3). In nanowire-based PCM, LRS is usually considered as a complete crystalline region through the whole nanowire and HRS is related to a certain formed amorphous region inside the nanowire. When the RESET pulse amplitude increases from 2 V to 3 V, the thickness U_a of centralized amorphous region grows from around 50 nm to 100 nm, as illustrated in Figs. 3(b) and 3(c).

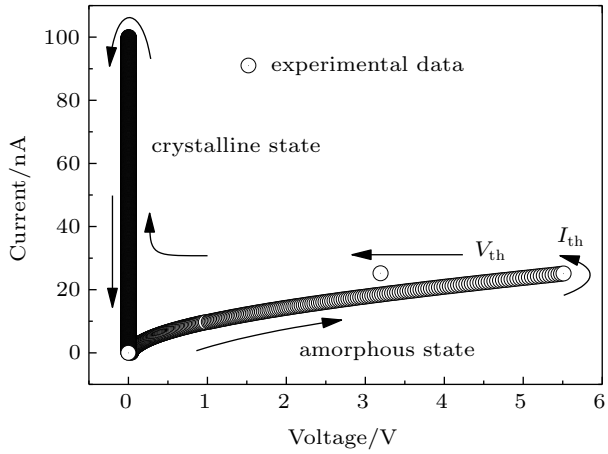


Fig. 4. Measured *I–V* characteristics of amorphous state and crystalline state.

Figure 4 shows the measured *I–V* characteristics of amorphous state and crystalline state. The amorphous state and crystalline state have large resistance contrast below the threshold voltage V_{th} and shows electronic threshold switching behavior at V_{th} with the corresponding threshold current I_{th}. Threshold is defined as the point where the amorphous state is turned into the crystalline state inside the nanowire. In order to investigate the uniformity of the threshold voltage and

current in In_2Se_3 nanowire-based PCM, multiple RESET operations are accomplished first to obtain the amorphous states and the I–V characteristics are measured to collect the values of threshold voltage V_{th} and threshold current I_{th}. The extracted values of V_{th} and I_{th} are shown in Fig. 5.

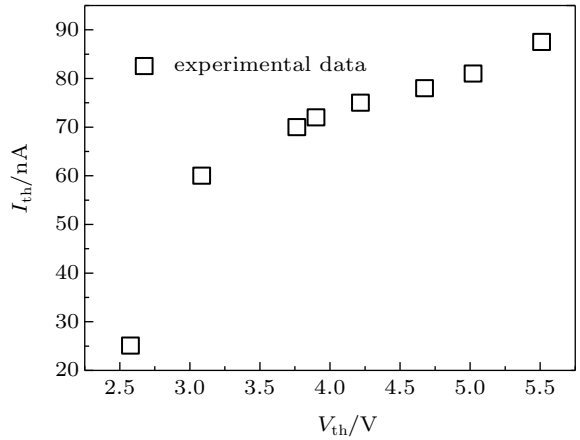


Fig. 5. The extracted threshold voltage V_{th} and threshold current I_{th} from multiple I–V measurements.

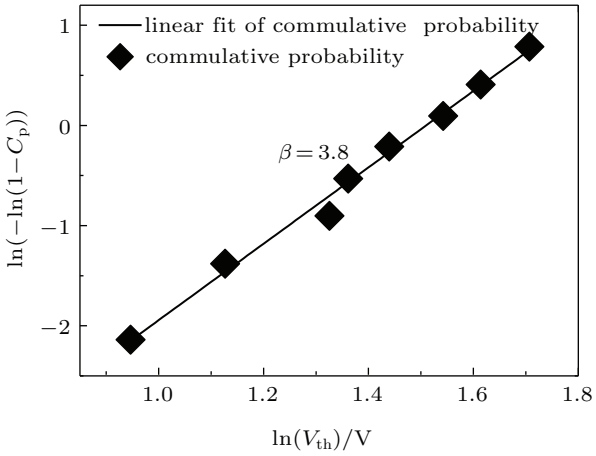


Fig. 6. Experimental data for the Weibull cumulative distribution of the extracted threshold voltage.

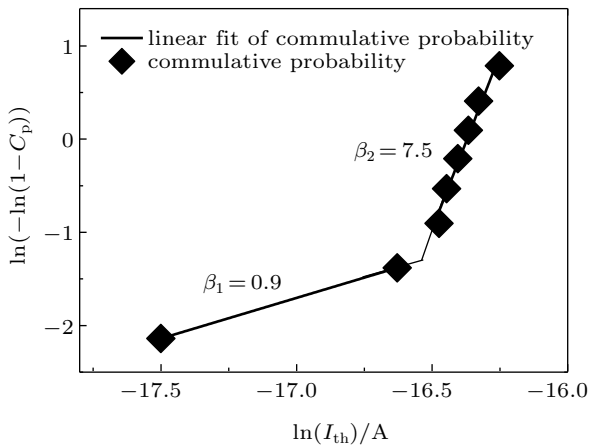


Fig. 7. Experimental data for the Weibull cumulative distribution of the extracted threshold current.

Weibull cumulative distribution is introduced to describe the uniformity of the extracted V_{th} and I_{th}. Figure 6 shows a single slope of the V_{th} cumulative probability linear fitting with the value $\beta = 3.8$. However, two separated I_{th} cumulative probability linear fitting slopes are observed in Fig. 7 with values $\beta_1 = 0.9$ and $\beta_2 = 7.5$, respectively. The larger slope means that the distribution of the threshold is more centralized and the uniformity is better, while the smaller slope means that the uniformity is worse. Compared to that of the threshold voltage, the uniformity issue of the threshold current seems to be more complicated, and the mechanism behind this phenomenon will be discussed in the following section.

3. Trap-limited transport model

According to the trap-limited transport model[22,23] proposed in the conduction in the amorphous state, carriers are thermally emitted from one trap to the conduction band and then captured by another trap which is commonly referred as the Poole–Frenkel transport. When a voltage is applied, the potential barrier to be overcome is decreased in the direction parallel to the electrostatic force as shown in Fig. 8. Figure 9 shows the carriers and traps distributions in the sub-threshold region, the trap filling obeys to the equilibrium conditions. High electrical field condition in the amorphous state can lead to a non-equilibrium distribution of carriers and injection of electrons into high energy states requires a certain distance U_{OFF}, given by[22]

$$U_{OFF} = \frac{E_t}{qF_{OFF}}, \tag{1}$$

where q is the elementary charge, E_t is the trap depth, and F_{OFF} is the electric field in the OFF layer, given by

$$F_{OFF} = \frac{2KT}{q\Delta z}\sinh^{-1}\left[\frac{t_0 I}{2qA\Delta z N_t(1+\gamma)}\,e^{(E_C-E_F)/KT}\right], \tag{2}$$

where A is the area of the contact, t_0 is the characteristic attempt-to-escape time for the trapped electron, γ is the non-equilibrium term, N_t is the trap density, I is the current. As for the ON layer, the distance U_{ON} can be expressed by

$$U_{ON} = U_a - U_{OFF}, \tag{3}$$

where U_a is the total amorphous layer thickness. The related electric field in the ON layer can be written as

$$F_{ON} = \frac{2KT}{q\Delta z}\sinh^{-1}\left[\frac{t_0 I}{2qA\Delta z N_t}\,e^{(E_C-E_F)/KT}\right]. \tag{4}$$

The non-uniformity of the electric field is essential to account for the threshold voltage switching. The voltage across the device is given by

$$V_{app} = U_{OFF}F_{OFF} + U_{ON}F_{ON}. \tag{5}$$

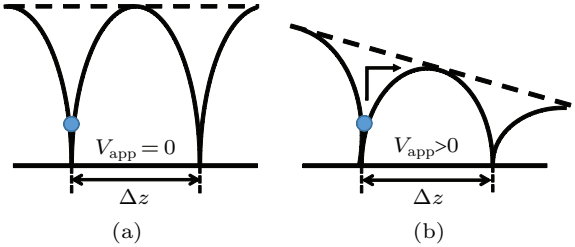


Fig. 8. (color online) (a) Schematic diagram showing the electron trapped in the localized states at the trap depth E_t. The inter-trap spacing is Δz. (b) When applying an electric field, the barrier height is decreased.

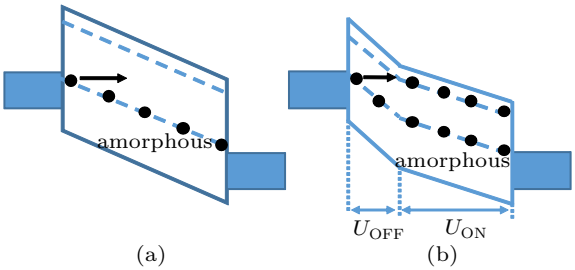


Fig. 9. (color online) Schematic diagram for the low-current (a) and high-current (b) potential profile and energy distribution of electrons in the amorphous state.

4. Influence of threshold switching uniformity

According to the trap-limited transport model discussed above, electrons transfer via thermal emission over the potential barrier from one trap to the conduction band and then are captured by another trap in the amorphous state. Amorphous layer thickness U_a is one of the key factors in the conduction mechanism.[24] The trap depth E_t determines the activation energy the carriers need to hop from one trap to another and the value can be decreased by applying an external voltage.[25] Especially, the different trap depths in the ON and OFF layers have a direct influence on the switching phenomenon, thus the switching voltage V_{th} and current I_{th}. Besides, the trap density N_t is another useful parameter which determines the trap distribution and spacing.[26] The three parameters (U_a, N_t, and E_t) have a major relationship to the uniformity of V_{th} and I_{th} and each parameter should be investigated separately to clarify its contribution.

As for the parameter U_a, a series of *I*–*V* characteristic simulations with input Gaussian distribution parameters U_a are accomplished firstly. Then, the Weibull cumulative distribution is used to study the amorphous layer thickness influence on the switching uniformity issues. The same analysis method can be applied to analyzing N_t and E_t.

The simulated results are illustrated in Figs. 10–12. The insets show the simulated *I*–*V* characteristics for the amorphous state using the Gaussian distribution parameters U_a, N_t, and E_t, respectively. As is shown in the inset in Fig. 10, although the amorphous layer thicknesses are different, all the *I*–*V* curves have the same switching I_{th} while a variation of the V_{th}. The V_{th} Weibull cumulative distribution is shown with the linear fitting of only one slope with $\beta = 4.7$. From the inset in Fig. 11, contrary to U_a, the variation of trap density N_t has no effect on the V_{th} but slight effect on the I_{th}. The linear fitting of I_{th} Weibull cumulative distribution shows only one

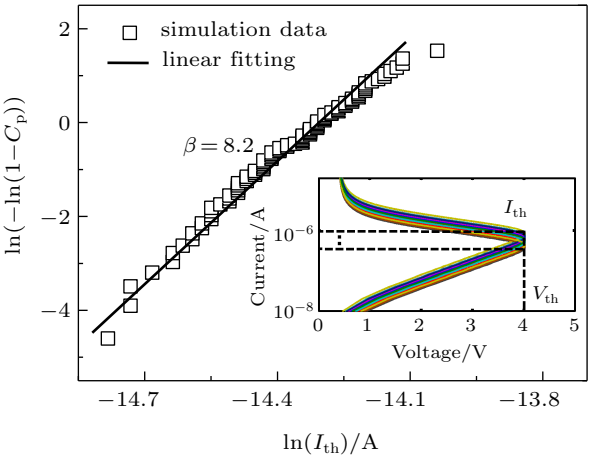


Fig. 11. (color online) Weibull cumulative distributionof I_{th} with linear fit (slope $\beta = 8.2$). The inset shows *I*–*V* characteristics for the amorphous state using the Gaussian distribution data of the trap density N_t.

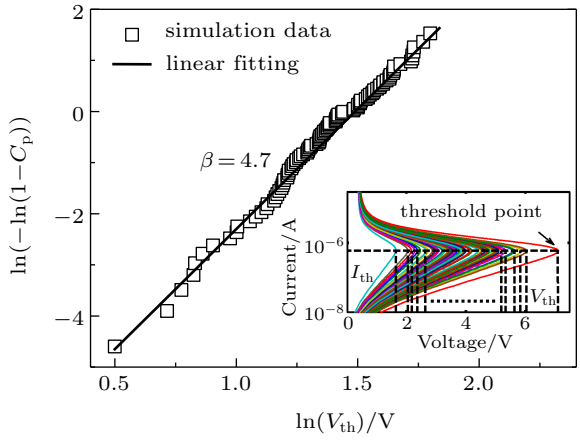


Fig. 10. (color online) Weibull cumulative distribution of V_{th} with linear fit (slope $\beta = 4.7$). The inset shows *I*–*V* characteristics for the amorphous state using the Gaussian distribution data of the amorphous layer thickness U_a.

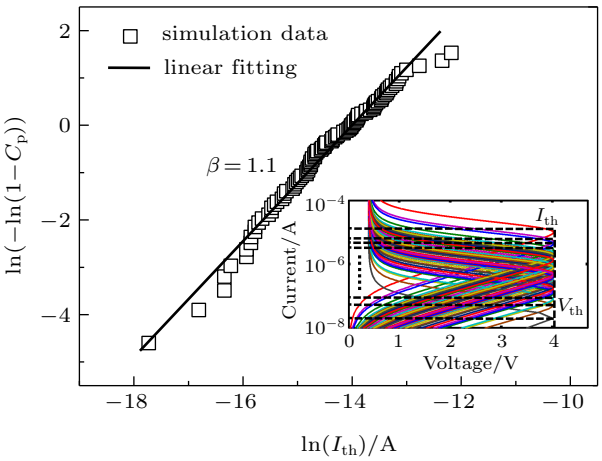


Fig. 12. (color online) Weibull cumulative distribution of I_{th} with linear fit (slope $\beta = 1.1$). The inset shows *I*–*V* characteristics for the amorphous state using the Gaussian distribution data of the trap depth E_t.

slope with $\beta = 8.2$. Similar to N_t, the variation of E_t has the same effect on the V_{th} and I_{th}, but with a smaller slope $\beta = 1.1$ (see Fig. 12). Based on the simulation results, we can make a conclusion that amorphous thickness U_a is the basic factor that leads to the uniformity of V_{th}. Both the two factors (trap density N_t and trap depth E_t) can directly change the critical threshold electrical field that determines the I_{th} which contributes little to V_{th}. The two slope values $\beta = 8.2$ and $\beta = 1.1$ indicate that the variation of E_t contributes more to the uniformity of I_{th}. The simulation results also have a clear explanation of the experimental data in Figs. 6 and 7.

5. Conclusion

In this paper, the extracted threshold voltage V_{th} and current I_{th} of the nanowire-based In_2Se_3 PCM were collected and the Weibull cumulative distribution was studied to investigate the threshold uniformity characteristics. Based on the trap limited model, factors (amorphous layer thickness U_a, trap density N_t, and trap depth E_t) were used to clarify their influences upon the switching parameters V_{th} and I_{th}. We conclude that the uniformity of V_{th} is mainly caused by the variation of the amorphous thickness which has little effect on the I_{th}. On the contrary, uniformity of the threshold current is largely induced by the trap density and trap depth while the latter influence is more sensitive. Our conclusion is of great use for designing the devices with a certain range of maximum programming voltage and current, especially for the low voltage devices.

References

[1] Burr G W, Kurdi B N, Scott J C, Lam C H, Gopalakrishnan K and Shenoy R S 2008 *IBM Journal of Research and Development* **52** 449

[2] Lam C H 2010 *Solid-State and Integrated Circuit Technology*, November 1–4, 2010, Shanghai, China, p. 1080

[3] Freitas R F and Wilcke W W 2008 *IBM Journal of Research and Development* **52** 439

[4] Marinella M 2013 *Aerospace Conference*, March 2–9, 2013, Big Sky, USA, p. 1

[5] Burr G W, Breitwisch M J, Franceschini M, Garetto D, Gopalakrishnan K and Jackson B 2010 *Journal of Vacuum Science & Technology* **28** 223

[6] Wong H S P, Raoux S, SangBum K, Jiale L, Reifenberg J P and Rajendran B 2010 *IEEE Proc.* **98** 2201

[7] Lai S and Lowrey T 2001 *Electron Devices Meeting*, December 2–5, 2001, Washington, DC, USA, p. 36.5.1

[8] Raoux S, Burr G W, Breitwisch M J, Rettner C T, Chen Y C and Shelby R M 2008 *IBM Journal of Research and Development* **52** 465

[9] Pirovano A, Lacaita A L, Benvenuti A, Pellizzer F, Hudgens S and Bez R 2003 *Electron Devices Meeting*, December 8–10, 2003, Washington, DC, USA, p. 29.6.1

[10] Russo U, Ielmini D, Redaelli A and Lacaita A L 2008 *IEEE Trans. Electron Devices* **55** 506

[11] Redaelli A, Pirovano A, Pellizzer F, Lacaita A L, Ielmini D and Bez R 2004 *IEEE Electron Dev. Lett.* **25** 684

[12] Redaelli A, Pirovano A, Benvenuti A and Lacaita A L 2008 *J. Appl. Phys.* **103** 111101

[13] Youngdon C, Ickhyun S, Mu-Hui P, Hoeju C, Sanghoan C and Beakhyoung C 2012 *Solid-State Circuits Conference Digest of Technical Papers*, February 19–23, 2012, San Francisco, USA, p. 46

[14] Kang D H, Ahn D H, Kwon M H, Kwon H S, Kim K B and Lee K S 2004 *Jpn. J. Appl. Phys.* **43** 5243

[15] Pirovano A, Lacaita A L, Benvenuti A, Pellizzer F and Bez R 2004 *IEEE Trans. Electron Devices* **51** 452

[16] Ovshinsk Sr 1968 *Phys. Rev. Lett.* **21** 1450

[17] Xuhui S, Bin Y, Ng G, Meyyappan M, Sanghyun J and Janes D B 2008 *IEEE Trans. Electron Devices* **55** 3131

[18] Bin Y, Xuhui S, Sanghyun J, Janes D B and Meyyappan M 2008 *IEEE Trans. Nanotechnol.* **7** 496

[19] Jie L, Bin Y and Anantram M P 2011 *IEEE Electron Dev. Lett.* **32** 1340

[20] Bo J, Jungsik K, Daegun K, Meyyappan M and Jeong-Soo L 2013 13*th IEEE Conference on Nanotechnology*, Auguest 5–8, 2013, Beijing, China, p. 849

[21] Yu B, Ju S, Sun X, Ng G, Nguyen T D, Meyyappan M and Janes D B 2007 *Appl. Phys. Lett.* **91** 133119

[22] Ielmini D and Zhang Y 2007 *J. Appl. Phys.* **102** 054517

[23] Shih Y H, Lee M H, Breitwisch M, Cheek R, Wu J Y and Rajendran B 2009 *Electron Devices Meeting*, December 7–9, 2009, Baltimore, USA, p. 31.7.1

[24] SangBum K, Byoung-Jae B, Yuan Z, Jeyasingh R G D, Youngkuk K and In-Gyu B 2011 *IEEE Trans. Electron Devices* **58** 1483

[25] Ielmini D and Zhang Y 2006 *Electron Devices Meeting*, December 11–13, 2006. San Francisco, USA, p. 1

[26] Jeyasingh R G D, Kuzum D and Wong H S P 2011 *IEEE Trans. Electron Devices* **58** 4370