An ultra-low specific on-resistance trench LDMOS with a U-shaped gate and accumulation layer*

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An ultra-low specific on-resistance ($R_{on,sp}$) oxide trench-type silicon-on-insulator (SOI) lateral double-diffusion metal–oxide semiconductor (LDMOS) with an enhanced breakdown voltage (BV) is proposed and investigated by simulation. There are two key features in the proposed device: one is a U-shaped gate around the oxide trench, which extends from source to drain (UG LDMOS); the other is an N pillar and P pillar located in the trench sidewall. In the on-state, electrons accumulate along the U-shaped gate, providing a continuous low resistance current path from source to drain. The $R_{on,sp}$ is thus greatly reduced and almost independent of the drift region doping concentration. In the off-state, the N and P pillars not only enhance the electric field (E-field) strength of the trench oxide, but also improve the E-field distribution in the drift region, leading to a significant improvement in the BV. The BV of 662 V and $R_{on,sp}$ of 12.4 mΩ·cm^2 are achieved for the proposed UG LDMOS. The BV is increased by 88.6% and the $R_{on,sp}$ is reduced by 96.4%, compared with those of the conventional trench LDMOS (CT LDMOS), realizing the state-of-the-art trade-off between BV and $R_{on,sp}$.

Keywords: trench, U-shaped gate, specific on-resistance, breakdown voltage

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1. Introduction

In order to increase the breakdown voltage (BV) for a conventional high voltage lateral double-diffusion metal–oxide semiconductor (LDMOS), it is necessary to reduce the drift region doping concentration (N_d) and increase the drift region length (L_d). For a high voltage LDMOS, the specific on-resistance ($R_{on,sp}$) is mostly determined by the N_d and L_d, resulting in the silicon (Si) limit of $R_{on,sp} \propto BV^{2.5}$.[1–3] The reduced surface field (RESURF) technology (including single/double/triple RESURF) is widely used to improve the trade-off between the $R_{on,sp}$ and BV. However, it is useless for reducing the cell pitch and thus restricts further reduction of the $R_{on,sp}$.[4–7] A dielectric trench inserted in the drift region for LDMOS not only improves the BV, but also dramatically reduces the $R_{on,sp}$ by shortening the device cell pitch.[8–11] However, a conventional deep trench is not suitable for high voltage application (e.g. $BV > 600$ V) because of its weakened RESURF effect and a corresponding low N_d. Therefore, the enhanced bulk field (ENBULF) concept is proposed to improve the BV and reduce the $R_{on,sp}$.[12] Unfortunately, the N_d is still the key limit of the $R_{on,sp}$ for existing MOSFETs with RESURF and trench technologies. The extended gate is used to enhance the conductance in the drift region in the on-state without compromise in the off-state BV.[13] However, it has an intrinsic high leakage current from gate to drain under the high gate–source voltage. Moreover, as a planar LDMOS, it is also helpless for reducing the cell pitch, which restricts the decrease of the $R_{on,sp}$.

In this paper, an SOI trench LDMOS with a U-shaped gate is proposed to realize a significant trade-off between $R_{on,sp}$ and BV. The current transports through the electron accumulation layer from source to drain. Consequently, the $R_{on,sp}$ greatly decreases and exhibits less dependence on the N_d. This current transport mode is different from that of the existing MOSFETs. In the off-state, the depleted N/P pillars enhance the E-field strength of the trench oxide and the drift region, leading to a higher BV. Thus, an ultra-low $R_{on,sp}$ and high BV are obtained.

2. Device structure and mechanism

Figure 1(a) shows the schematic cross-section view of a UG LDMOS. An oxide trench is built into the drift region, and a U-shaped gate surrounding the trench extends from source to drain. In the U-shaped gate semiconductor, the P-pillar is adjacent to the P$^+$ region under the gate electrode, extending to the bottom of the trench. One side of the N-pillar touches the P-pillar at the trench bottom, and the other side contacts the PN junction (D_R) connected to the drain electrode (D). The D_R is reversely biased to sustain the gate–drain voltage (V_{GD}) in the on-state. In Fig. 1(a), T_{si}, T_{ox}, T_t, and T_{dox} are the thickness values of the active region, the buried oxide (BOX) layer, the trench, and the gate oxide layer, respectively. W_t and W are the widths of the trench and the device respectively.

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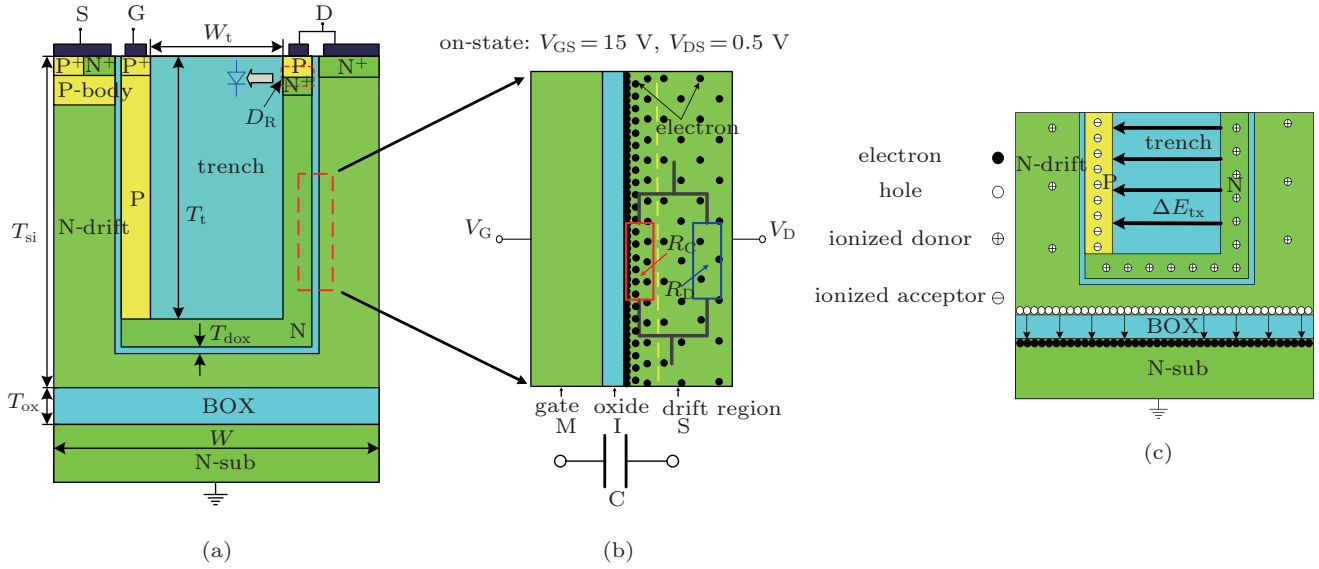


Fig. 1. (color online) (a) Schematic cross-sectional view of the UG LDMOS. (b) Working mechanism of the gate structure in on-state. (c) Charges distribution in the off-state.

Figure 1(b) shows the operation mechanism of the gate structure (marked with the dashed rectangle in Fig. 1(a)) in the on-state. It indicates the electron distribution and the equivalent resistances of the drift region. Meanwhile, the equivalent metal–insulator–semiconductor (MIS) capacitance between the U-shaped gate structure and the drift region is also demonstrated. When $V_{GS} > V_{DS}$, electrons accumulate along the sidewall of the U-shaped gate oxide caused by the MIS structure mentioned above. Further, electrons flow through the inversion channel and the accumulation layer at $V_{GS} > V_{th}$ (V_{th}: threshold voltage), forming a continuous ultra-low resistance path. The V_{GD} is sustained by the reversely biased D_R in Fig. 1(a).

The on-resistance of the drift region (R) consists of two resistances connected in parallel in Fig. 1(b): the accumulation layer resistance (R_C) and the resistance R_D determined by the doping concentration. In general, $R_C \ll R_D$ and thus $R \approx R_C$. Additionally, the P-pillar has an assisted depletion effect on the N-drift region in the off-state, allowing a higher N_d and a lower R_D. Therefore, the total drift region resistance is significantly reduced.

Figure 1(c) shows the charge distribution in the off-state for the UG LDMOS. The off-state operation mechanism is given as follows.

First, the lateral BV (BV_{lat}) is sustained mainly by the oxide trench. It can be given by

$$BV_{lat} \approx E_{tx} \cdot W_t, \tag{1}$$

where E_{tx} is the horizontal E-field strength in the oxide trench. The fully depleted N/P pillars beside the oxide trench provide an additional E-field ΔE_{tx} as shown in Fig. 1(c). As a result, the E_{tx} and the BV_{lat} are enhanced.

Second, the vertical BV (BV_{ver}) is sustained by the Si layer (V_{SD}) and the BOX layer (V_I) under the drain. These can be written as

$$BV_{ver} = V_{SD} + V_I, \tag{2a}$$

$$V_I = E_I \cdot T_{ox}, \tag{2b}$$

$$E_I \varepsilon_I = E_S \varepsilon_S + q\sigma_{in}, \tag{2c}$$

where E_I and E_S are the E-field strengths of the BOX and the Si at the Si/BOX interface respectively; ε_S and ε_I are their relative permittivities of Si and BOX; σ_{in} is the charge density at the BOX interface. Note that holes and electrons are induced at the interface of the BOX, as illustrated in Fig. 1(c). V_I and BV_{ver} are improved.

Third, the voltage sustained by the BOX layer is equal to that sustained by the Si layer under the source (V_{SS}). Because both the source and substrate are grounded, equation (2a) can also be expressed by

$$BV_{ver} = V_{SD} + V_{SS}. \tag{3}$$

3. Results and discussion

The electric characteristics are investigated with simulator MEDICI. The device structure parameters used in the simulation are given as follows: $W = 15.0$ μm, $W_t = 9.0$ μm, $T_{si} = 25.0$ μm, $T_{ox} = 1.0$ μm, $T_t = 21.0$ μm, and $T_{dox} = 0.1$ μm.

Figures 2(a) and 2(b) show the two-dimensional (2D) flow line distributions of the UG LDMOS and CT LDMOS in the on-state, respectively. In the UG LDMOS, a high-density electron accumulation layer is induced beside the U-shaped gate. As a result, the current density through the accumulation layer is very high and the current herein

achieves 88.7% of the whole current (by integral verification) in Fig. 2(c). Additionally, owing to the charge compensation between the N-drift region and the P-pillar, the optimal N_d of 2.2×10^{15} cm^{-3} is higher for the UG LDMOS. However, the N_d of 3.4×10^{14} cm^{-3} is very low in the CT LDMOS because the RESURF effect is weakened by a deep trench. The current determined by the N_d is improved (ΔI_{D1}), (although the cross section of the current in CT LDMOS is slightly wider than that in UG LDMOS, i.e. $J_1J_3' > J_1J_2$). The simulation shows that the $R_{on,sp}$ is sharply reduced from 346.6 mΩ·cm^2 to 12.4 mΩ·cm^2.

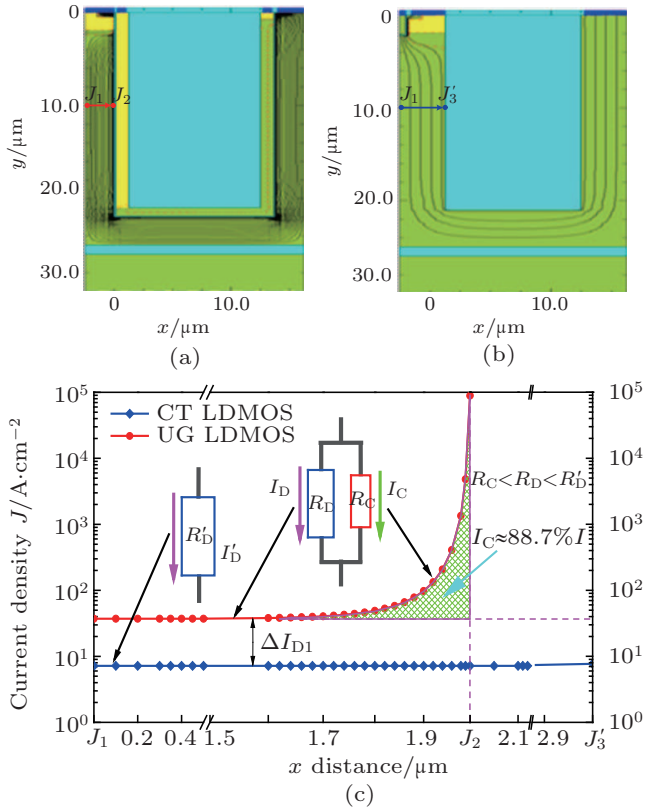


Fig. 2. (color online) Flow line distributions of (a) UG LDMOS (12.4 mΩ·cm^2) and (b) CT LDMOS (346.6 mΩ·cm^2) (5×10^{-8} A·μm^{-1}/contour) with the optimal doping concentration of the drift region. (c) Current density distributions under the source ($y = 10.0$ μm).

Figure 3 shows the equi-potential contours at breakdown. The voltage drop along the trench surface (i.e., the $D \to A$ direction) is equal to that around the trench (i.e., along the $D \to C \to B \to A$ direction), which represents that the oxide trench folds the drift region and thus increases the effective drift region length. In the UG LDMOS, as the N/P pillars enhance the E-field strength in the oxide trench (along $D \to A$) and optimize the E-field strength around the trench (along $D \to C \to B \to A$), the equi-potential contours in the trench region and the drift region are uniform compared with those of the CT LDMOS. The double-headed arrows in Fig. 3 indicate the voltage drops in Si under the source and drain. Owing to the N/P pillars, V_{SS} increases from 233 V to 340 V and V_{SD} from 118 V to 322 V. According to Eq. (3), the BV of the UG LDMOS increases to 662 V compared with the 351 V of the CT LDMOS at the same cell pitch of 15 μm.

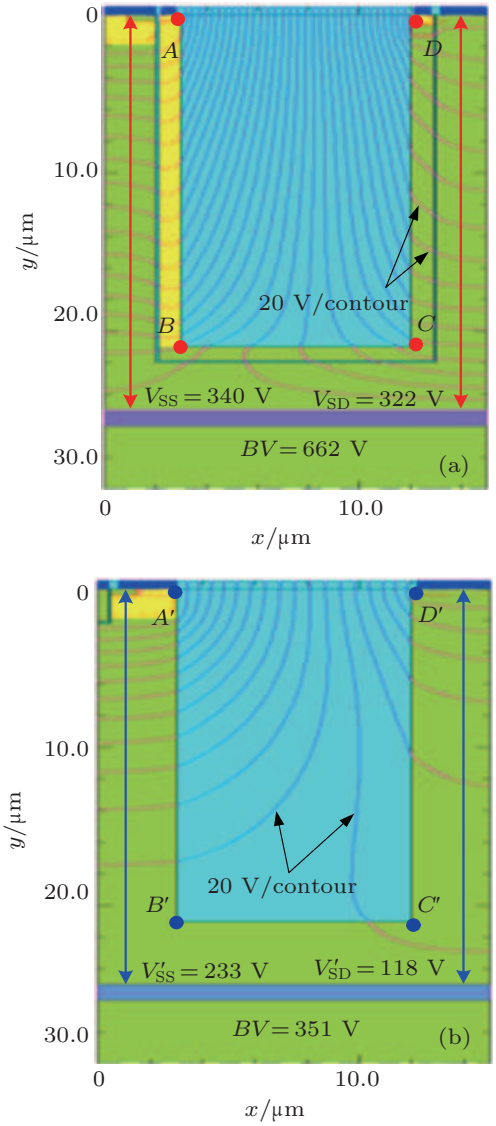


Fig. 3. (color online) Equi-potential contours at breakdown voltage for (a) UG LDMOS (662 V) and (b) CT LDMOS (351 V).

Figure 4(a) provides the E-field distributions around the trench. The N/P pillars in the UG LDMOS introduce two new E-field peaks at the bottom of the trench (points B and C), which improve the E-field in the drift region. However, the E-field strength is low near the trench bottom (e.g., points B' and C') for the CT LDMOS. Figure 4(b) shows the horizontal E-field (E_{tx}) distributions at the surface and bulk of the oxide trench. The surface field of UG LDMOS increases to 8.3×10^5 V/cm from 4.9×10^5 V/cm of the CT LDMOS, with an additional E-field $\Delta E_{tx} \approx 3.4\times10^5$ V/cm. Meanwhile, in the bulk ($y = 10$ μm), the E-field strength increases by about 3.4×10^5 V/cm. Therefore, the BV_{lat} is considerably improved as indicated in Eq. (1).

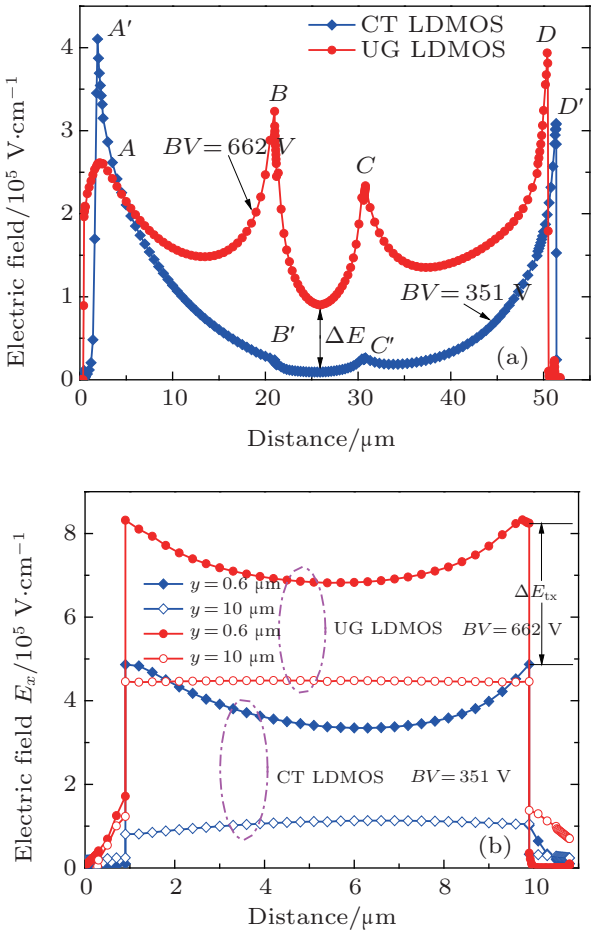


Fig. 4. (color online) (a) Electric field distributions around the trench for UG LDMOS and CT LDMOS. (b) Horizontal electric field distributions at the surface ($y = 0.6$ μm) and bulk ($y = 10.0$ μm) of the trench in UG LDMOS and CT LDMOS.

The E-field and potential distributions under the drain and source are shown in Fig. 5(a). The N/P pillars improve the E-field distribution of the UG LDMOS, leading to higher voltages sustained by the drift regions under source (V_{SS}) and drain (V_{SD}). The BV_{ver} is thus considerably improved as shown in Eq. (3). Figure 5(a) also illustrates Eq. (2a) and $V_I = V_{SS}$. Meanwhile, the top interface potential of the BOX layer is clamped, and thus the potential drop across the BOX remains a constant of $V_I = V_{SS} = 340$ V. As a result, lots of holes and electrons are adaptively induced at the top and bottom interfaces of the BOX. The potential distributions along the top surface of the BOX layer are independent of the T_{ox} before the dielectric breakdown. Figure 5(b) illustrates the E-field strengths of the BOX layer at breakdown with the different T_{ox} values. More than 5×10^{18} cm^{-3} holes and electrons accumulate at the opposite interfaces of the BOX layer. The charge density is adaptive to maintain the constant V_I value at the different T_{ox} values. According to Eq. (2c) mentioned above, the E-field distributions of the BOX layer (E_I) are enhanced adaptively with different values of T_{ox}. The E-field of the BOX layer increases from 170 V/ μm to 678 V/ μm with T_{ox} decreasing from 2.0 μm to 0.5 μm.

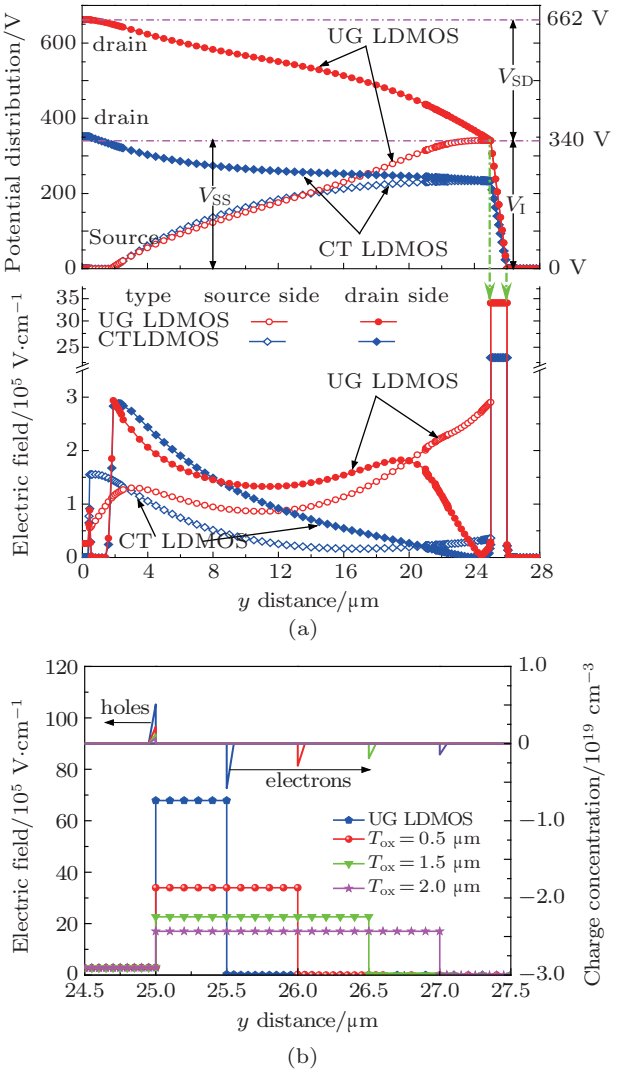


Fig. 5. (color online) (a) Electric field and potential distributions under drain and source. (b) Electric fields of the BOX layer at breakdown with different values of T_{ox} ($x = 14.0$ μm).

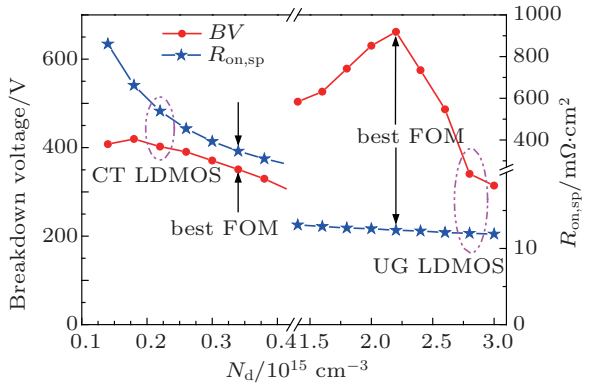


Fig. 6. (color online) Influence of drift region doping on BV and $R_{on,sp}$.

Figure 6 reveals the influences of N_d on BV and $R_{on,sp}$. For the CT LDMOS, the $R_{on,sp}$ increases by 206.8% (from 280.5 mΩ·cm^2 to 860.5 mΩ·cm^2) when N_d decreases by 66.7% (from 4.2×10^{14} cm^{-3} to 1.4×10^{14} cm^{-3}). However,

the $R_{on,sp}$ of the UG LDMOS increases only by 9.2% (from 11.9 mΩ·cm^2 to 13.1 mΩ·cm^2) when N_d decreases by 53.3% (from 3.0×10^{15} cm^{-3} to 1.4×10^{15} cm^{-3}). Therefore, for the UG LDMOS, the $R_{on,sp}$ is not only extremely low but also almost independent of the N_d. It means that the highest figure of merit (FOM) (FOM = $BV^2/R_{on,sp}$) is obtained at the highest BV for the UG LDMOS. Consequently, the N_d is chosen to obtain the highest BV without influence on the $R_{on,sp}$ for the UG LDMOS. However, the optimal N_d of the CT LDMOS is chosen by taking the trade-off between the $R_{on,sp}$ and the BV into account. This is an important advantage of the UG LDMOS over the CT LDMOS. Moreover, the BV of the UG LDMOS is superior to that of the CT LDMOS.

Table 1. Optimized characteristics for the UG LDMOS, CT LDMOS, ENBULF LDMOS, and TLDMOS.

Device types	N_d/cm^{-3}	BV/V	$R_{on,sp}$/mΩ·cm^2	FOM/(MW/cm^2)
UG LDMOS	2.2×10^{15}	662	12.4	35.3
CT LDMOS	3.4×10^{14}	351	346.6	0.36
ENBULF LDMOS[12]	2.4×10^{15}	684	48.5	9.6
TLDMOS[11]	1.7×10^{15}	840	60.2	11.7

Table 1 summarizes the optimized characteristics of N_d, BV, $R_{on,sp}$, and FOM for the UG LDMOS, CT LDMOS, ENBULF LDMOS (Ref. [12]), and the latest TLDMOS (Ref. [11]). It reveals that simple trench technology cannot achieve optimal trade-off between the BV and the $R_{on,sp}$ in the case of high voltage application because of the weakened RESURF effect.

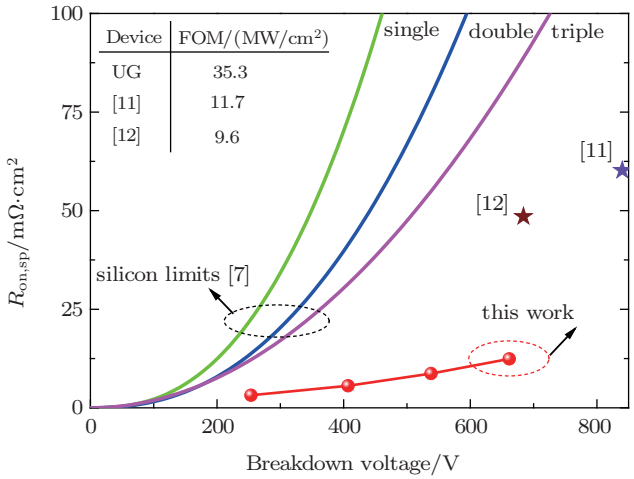


Fig. 7. (color online) A comparison of $R_{on,sp}$ versus BV for UG LDMOS among different RESURF effects, ENBULF LDMOS, and the latest TLDMOS.

Figure 7 shows a comparison of the $R_{on,sp}$ versus BV among the UG LDMOS, different RESURF LDMOSFETs (including single/double/triple RESURF) in Ref. [7], ENBULF LDMOS and the latest TLDMOS. Apparently, the $R_{on,sp}$ of the UG LDMOS is far lower than those of the others. The UG LDMOS obtains a state-of-the-art trade-off between $R_{on,sp}$ and BV at different voltage levels.

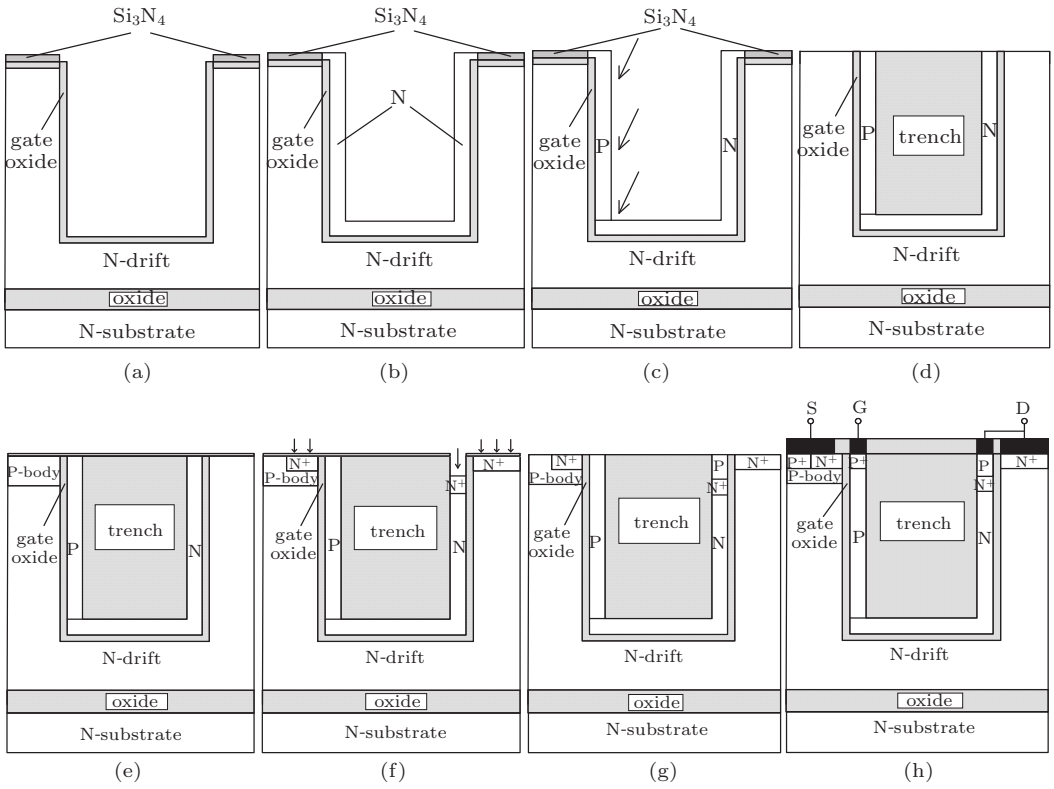


Fig. 8. Key steps of the UG LDMOS: (a) etch trench and form the gate oxide layer, (b) form the N-pillar, (c) form the P-pillar, (d) form the trench, (e) form the P-body, (f) form the N$^+$ region of the D_R, N$^+$ source, and drain region, (g) form the P-type region of the D_R, (h) form the body contact region, the gate contact region, and electrodes.

Figure 8 shows the feasible key process steps to fabricate a prototype UG LDMOS: (a) etch the SOI material (with an oxide layer and an Si_3N_4 shielding layer) and then thermally grow to form the gate oxide layer; (b) deposit a certain doped N-type polysilicon, chemical–mechanical planarization (CMP) and etch the polysilicon to form the N-pillar; (c) angled ion implant to form the P-pillar; (d) fill the trench with SiO_2 followed by CMP, and then remove the Si_3N_4 layer and the oxide layer; (e) implant to form the P-body and then thermally grow an oxide layer; (f) etch the N-pillar and implant to form the N^+ region of the D_R, N^+ source /drain region; (g) deposit the P-type region on N^+ to form D_R followed by CMP; (h) implant to form the body contact region, the gate contact region, and deposit to form the electrodes.

4. Conclusions

An ultra-low specific on-resistance LDMOS with a U-shaped gate is proposed and investigated by simulation. With the U-shaped gate around the oxide trench, the proposed structure can introduce a high-density electron accumulation layer and provide a low-resistance current path in the on-state. The $R_{on,sp}$ is sharply reduced and less dependent on the doping concentration of the drift region. With the N/P pillars at the sidewalls of the oxide trench, not only can the UG LDMOS increase the BV but also reduce the $R_{on,sp}$. As a result, $BV = 662$ V and $R_{on,sp} = 12.4$ mΩ·cm^2 are obtained at a cell pitch of 15 μm. The proposed UG LDMOS realizes the state-of-the-art trade-off between BV and $R_{on,sp}$, compared with the conventional oxide trench LDMOS, RESURF LDMOS, ENBULF LDMOS, and the latest TLDMOS.

References

[1] Tatsuhiko Fujihira and Yasushi Miyasaka 1998 *IEEE ISPSD* p. 423
[2] Fan Y H, Luo X R, Wang P, Zhou K, Zhang B and Li Z J 2013 *Chin. Phys. Lett.* **30** 088503
[3] Duan B X and Yang Y T 2011 *IEEE Trans. Electron Dev.* **58** 2057
[4] Adriaan W Ludikhuize 2000 *IEEE ISPSD* p. 11
[5] Disney D R, Paul A K, Darwish M, Baseckiand R and Rumennik V 2001 *IEEE ISPSD* p. 399
[6] Huang H M, Wang Y W and Chen X B 2011 *IEEE ASIC* p. 547
[7] Md Mash-Hud Iqbal, Florin Udrea and Ettore Napoli 2009 *IEEE ISPSD* p. 247
[8] Yue L, Zhang B and Li Z J 2012 *IEEE Electron. Dev. Lett.* **33** 1174
[9] Son W S, Sohn Y H and Choi S Y 2004 *Solid-State Electron.* **48** 1629
[10] Varadarajan K R, Chow T P, Wang J, Liu R and Gonzalez F 2007 *Proc. IEEE ISPSD* p. 233
[11] Xia C, Cheng X H, Wang Z J, Xu D W, Cao D, Zheng L, Shen L Y, Yu Y H and Shen D S 2014 *IEEE Trans. Electron Dev.* **61** 3477
[12] Zhang W T, Qiao M, Wu L J, Ye K, Wang Z, Wang Z G, Luo X R, Zhang S, Su W, Zhang B and Li Z J 2013 *IEEE ISPSD* p. 329
[13] Vestling L, Edholm B, Olsson J, Tiensuu S and Soderbarg A 1997 *Proc. IEEE ISPSD* p. 45