Novel substrate trigger SCR-LDMOS stacking structure for high-voltage ESD protection application

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A novel substrate trigger semiconductor control rectifier-laterally diffused metal–oxide semiconductor (STSCR-LDMOS) stacked structure is proposed and simulated using the transimission line pulser (TLP) multiple-pulse simulation method in a 0.35-μm, 60-V biploar-CMOS-DMOS (BCD) process without additional masks. On account of a very low holding voltage, it is susceptible to latch-up-like danger for the semiconductor control rectifier-laterally diffused metal–oxide semiconductor (SCR-LDMOS) in high-voltage electro-static discharge (ESD) protection applications. Although the conventional stacking structure has achieved strong latch-up immunity by increasing holding voltage, excessive high trigger voltage does not meet requirements for an ESD protection device. The holding voltage of the proposed stacked structure is proportional to the stacking number, whereas the trigger voltage remains nearly the same. A high holding voltage of 30.6 V and trigger voltage of 75.4 V are achieved.

Keywords: electrostatic discharge, high holding voltage, latch-up, STSCR-LDMOS

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1. Introduction

The popularity of the power integrated circuit (PIC) brings a lot of problems that need to be solved for electro-static discharge (ESD) protection in high-voltage circuits.[1–4] To achieve a high breakdown voltage, the power device structure is implemented as an ESD device.[5] The conventional laterally diffused metal–oxide semiconductor (LDMOS) used as an output driver is always vulnerable to ESD.[6,7] An effective method to solve this problem is to use a semiconductor control rectifier-laterally diffused metal oxide semiconductor (SCR-LDMOS);[8] however, its low holding voltage and latch-up immunity are challenging issues for its application.[9] Increasing the holding voltage is an effective way to achieve latch-up immunity of the ESD protection device.[10] Using a stacked device structure can achieve a high holding voltage. The simple stacked device structure, however, also brings an excessively high trigger voltage. A promising technique to reduce the trigger voltage is to use a substrate trigger silicon controlled rectifier (SCR).[11] The stacked substrate trigger SCR, which is triggered by an RC trigger circuit,[12] is only used for low-voltage ESD protection application.[13]

In this paper, a high holding voltage substrate trigger semiconductor control rectifier-laterally diffused metal–oxide semiconductor (STSCR-LDMOS) stacking structure is proposed and simulated in a 0.35-μm, 60-V biploar-CMOS-DMOS (BCD) process. The holding voltage can be increased by increasing the stacked number of the cells whereas the trigger voltage keeps as low as that of one single cell. A high holding voltage of 30.6 V with a low trigger voltage of 75.4 V can be simultaneously achieved without an additional process and mask.

2. Device design and operation mechanism

A conventional stacked SCR-LDMOS structure and the proposed stacked STSCR- LDMOS structure are respectively shown in Figs. 1(a) and 1(b), and the unit-SCR-LDMOS and unit-STSCR-LDMOS are respectively shown in the two dashed boxes in Figs. 1(a) and 1(b). The unit-SCR-LDMOS includes two parasitic transistors P_2 and N_2, which comprises a parasitic SCR. Compared with the unit-SCR-LDMOS structure, the unit-STSCR-LDMOS structure is added with a p-type heavy doping region in the p-body, as a p-trig terminal. The operating principle of the unit-STSCR-LDMOS structure is as follows. When current is injected from the p-trig terminal, the voltage on the resistance R_{p2} will trigger parasitic transistor N_2, and the current of N_2 will flow through the resistance R_{n2}, which will trigger parasitic transistor P_2. Finally, N_2 and P_2 form positive feedback, that is, parasitic SCR is triggered. In addition, adding the p-trigger electrode increases the size of the p-body and base width of parasitic transistor N_2, which will reduce the magnification β of parasitic transistor N_2 and weaken the effect of positive feedback between transistors N_2 and P_2. Therefore, the holding voltage of the unit-STSCR-LDMOS is higher than that of the unit-SCR-LDMOS. A comparison of the holding voltage is listed in Table 1.

The conventional SCR-LDMOS stacking structure is the direct stacking of the unit-SCR-LDMOSs, while the proposed STSCR-LDMOS stacking structure is not only the stacking of the unit-STSCR-LDMOS, but also connected with the resistance which is used to trigger the stacking structure. As shown in Fig. 1(b), the trigger resistance R_1 connects with two p-trig terminals, the trigger resistance R_2, and two gates. A high voltage N-well isolates the unit-STSCR-LDMOS from

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the others, so the proposed stacking structure does not require an additional process nor a mask. In order to improve the holding voltage, more than two stages of stacked STSCR-LDMOS may be required in practical applications.

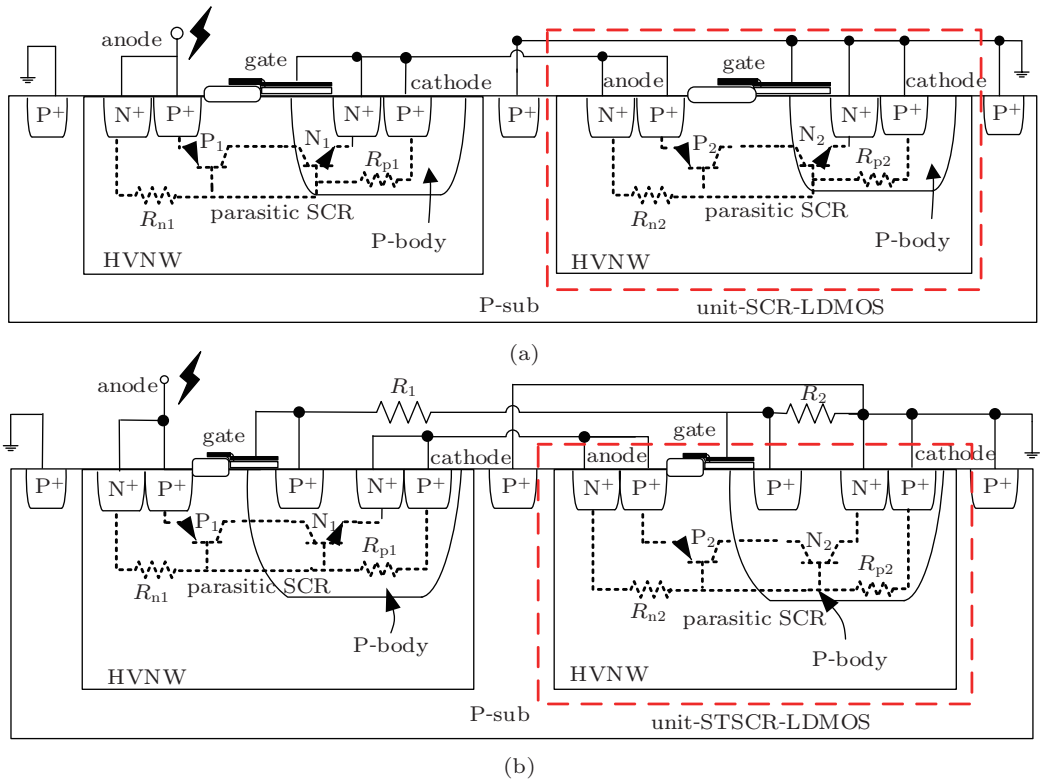


Fig. 1. (color online) Schematic cross-sectional views of (a) the conventional SCR-LDMOS stacking structure and (b) the proposed STSCR-LDMOS stacking structure.

Table 1. Comparison of holding voltage.

	SCR-LDMOS	STSCR-LDMOS
Holding voltage of one stacking structure	6.4 V	6.9 V
Holding voltage of two stacking structures	13.3 V	14.2 V
Holding voltage of three stacking structures	18.7 V	20.1 V

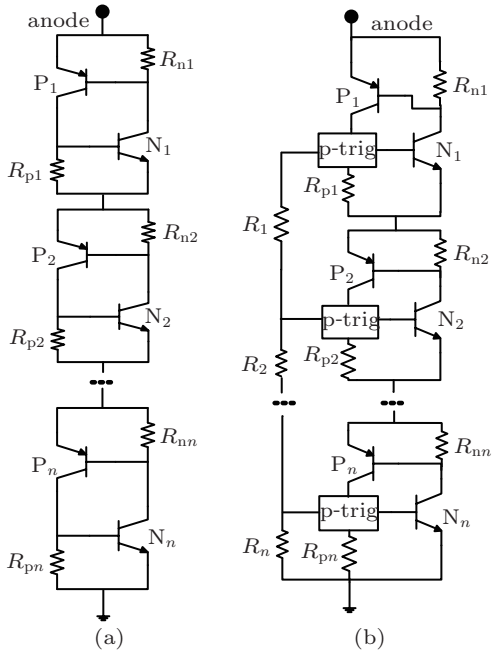


Fig. 2. Equivalent circuits for (a) conventional SCR-LDMOS stacking structure and (b) proposed STSCR-LDMOS stacking structure.

The equivalent circuits of the conventional and proposed stacking structure are shown in Figs. 2(a) and 2(b). Under ESD stress, each SCR-LDMOS needs to be triggered by breakdown for the conventional SCR-LDMOS stacking structure, so the trigger voltage of which is the sum of that of each SCR-LDMOS. For the proposed STSCR-LDMOS stacking structure, except for the first unit-STSCR-LDMOS, the trigger voltages of the others are all very small because their trigger modes each are the current injection from the p-trig terminal, rather than the breakdown of the internal junction. Parasitic transistor P_1 which has been triggered will provide the trigger current for other STSCR-LDMOSs by the trigger resistances R_1, R_2, and R_n. Then each STSCR-LDMOS will be triggered and discharge the ESD current. Therefore, the trigger voltage of the proposed STSCR-LDMOS stacking structure depends mainly on the breakdown voltage of parasitic transistor P_1, that is, the trigger voltage of the first STSCR-LDMOS. In addition, the holding voltage of the proposed stacking structure

is the sum of that of each unit cell. In normal operation, the stacking structure is in the off-state, and will not affect the normal work of the internal circuit because the working voltage is less than the trigger voltage of STSCR-LDMOS.

3. Device simulations and analysis

The simulation model of the ESD protection device has attracted extensive attention.[14–16] To analyze the performance of the proposed stacking structure, a novel simulation method, TLP multiple-pulse simulation is used by Ding *et al*.[17] Because of the many advantages of this method, it is necessary to introduce the simulation method here.

This method is similar to the actual TLP test. A series of current pulses with increasing amplitude, 10 ns of rise time, 100 ns of duration time, is applied to both ends of the simulation device. Then a series of voltage pulses will be obtained by the transient simulation of each current pulse. Figure 3(a) shows the voltage pulse of the conventional SCR-LDMOS, where the curves of the voltage pulse are marked with different letters. Each current pulse and the average of 70%∼90% of the corresponding voltage will constitute a point of the TLP *I*–*V* curve, by linking the series of points into a line, thereby obtaining a TLP *I*–*V* curve. Figure 3(b) shows the TLP *I*–*V* curve extracted from Fig. 3(a). Each point is marked with a letter which corresponds to the letter of Fig. 3(a). The device parameters are listed in Table 2.

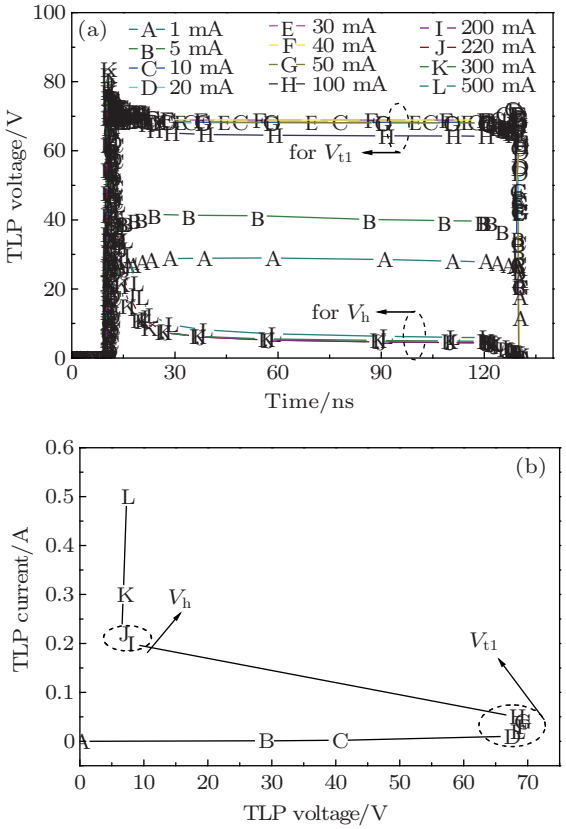


Fig. 3. (color online) (a) A series of voltage responses obtained by the transient simulation; (b) simulated TLP *I*–*V* curve.

Table 2. Device parameters used in the simulation.

Device parameters	SCR-LDMOS	STSCR-LDMOS
HVNW length	12.5 μm	15 μm
Spacing between two HVNW	7 μm	7 μm
Device width	100 μm	100 μm
Total area of three stacking structures	5950 μm^2	6700 μm^2
Substrate concentration	5×10^{14} cm^{-3}	5×10^{14} cm^{-3}
HVNW concentration	2×10^{15} cm^{-3}	2×10^{15} cm^{-3}
P-body concentration	1×10^{17} cm^{-3}	1×10^{17} cm^{-3}
Trigger resistance	no	50/100/200/300/400/500 Ω

Figure 4(a) shows the simulated TLP *I*–*V* curves of the conventional stacked SCR-LDMOS structure with the stacking number increasing from 1 to 3 by using the method of TLP multiple-pulse simulation. The trigger voltage increases from 70.7 V to 208.2 V and the holding voltage increases from 6.4 V to 18.7 V. The holding voltage increasing with the stacking number is consistent with our expected result. However, the trigger voltage is also proportional to the stacking number, which is undesired for HV ESD.

Figure 4(b) shows the simulated TLP *I*–*V* curve of the proposed stacked STSCR-LDMOS structure with the stacking number increasing from 1 to 4, and trigger resistance being 100 Ω. There are twice the snapback phenomena. At the first time the parasitic transistor P_1 is triggered, the breakdown voltage increases only from 70.2 V to 71.6 V when the stacking number increases from 1 to 4. At the second time the transistor P_1 provides an adequate trigger current for the stacked STSCR-LDMOS structure, all of the parasitic SCRs will be triggered, and the trigger voltage of the second snapback increases from 66.7 V to 79.7 V when the stacking number increases from 2 to 4. Therefore, the trigger voltage of the STSCR-LDMOS stacking structure increases from 70.2 V to 79.7 V and the holding voltage increases from 6.9 V to 25.4 V when the stacking number increases from 1 to 4.

Therefore, the novel STSCR-LDMOS stacking structure has a high holding voltage which is the sum of that of the unit

cell and a low trigger voltage, which depends mainly on the trigger voltage of the first STSCR-LDMOS. A high holding voltage ensures that the novel STSCR-LDMOS stacking structure has strong latch-up immunity. A low trigger voltage ensures that the stacking structure can be triggered quickly under ESD stress. Therefore, the proposed stacked STSCR-LDMOS structure is attractive to high-voltage ESD protection applications. Increasing the magnification β of parasitic transistor P_1 can reduce the holding voltage of transistor P_1, and reduce the second snapback trigger voltage of the stacking structure, which may reduce the trigger voltage of the stacking structure. The second snapback trigger current increases from 10 mA to 100 mA when the stacking number increases from 2 to 4, which is also conducible to noise immunity.

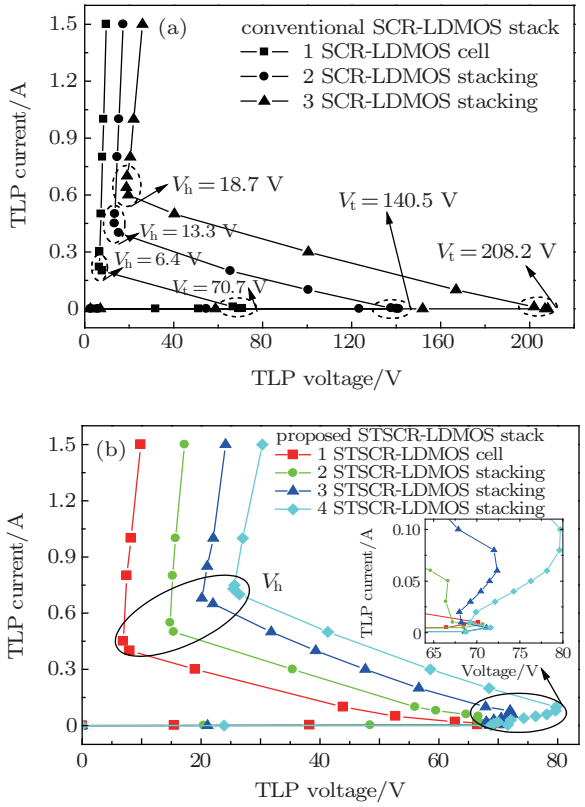


Fig. 4. (color online) Simulated TLP I–V characteristics of (a) the conventional SCR- LDMOS stacking structure, (b) the proposed STSCR-LDMOS stacking structure with $R_1 = R_2 = R_n = 100$ Ω.

Trigger resistances R_1, R_2, and R_n have an important influence on the trigger voltage of the proposed stacked STSCR-LDMOS structure. Figure 5 shows the trigger voltage characteristics of the proposed STSCR-LDMOS stacking structure. The greater the trigger resistance, the faster the trigger voltage increases with the stacking number, because the big trigger resistance will result in the trigger voltage of the second snapback increasing quickly, as shown in Fig. 4(b). The trigger voltage increases from 70.1 V to 75.36 V when the trigger resistance is 50 Ω. However, the trigger voltage increases from 70.43 V to 122.95 V when the trigger resistance is 500 Ω. In addition, the trigger resistance has little influence on the trigger voltage for one STSCR-LDMOS. The trigger voltage, however, will increase with increasing the trigger resistance and the stacking number for two or more STSCR-LDMOS.

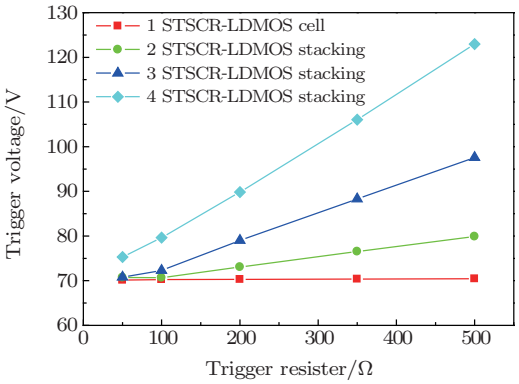


Fig. 5. (color online) Trigger voltage characteristics of the proposed STSCR-LDMOS stacking structure.

Trigger resistances R_1, R_2, and R_n also have an important influence on the holding voltage of the proposed stacking structure. Figure 6 shows the holding voltage characteristics of the proposed STSCR-LDMOS stacking structure. The holding voltage increase is proportional to the stacking number, for example, it increases from 7.57 V to 30.6 V when the trigger resistance is 50 Ω. The holding voltage remains nearly the same when the trigger resistance is greater than 200 Ω. However, it increases with reducing the trigger resistance when resistance is less than 200 Ω. The reason is that the current flowing from the p-trig terminal of the first STSCR-LDMOS, after the stacking structure has been triggered, increases gradually with reducing the trigger resistance.

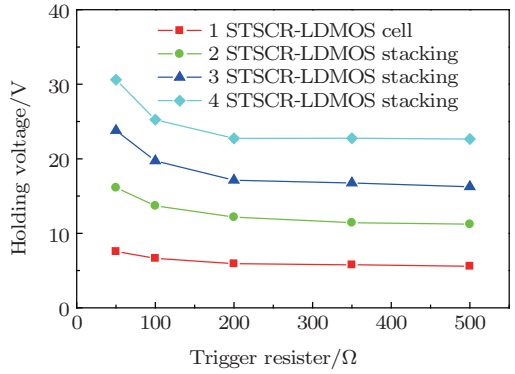


Fig. 6. (color online) Holding voltage characteristics of the proposed STSCR-LDMOS stacking structure.

Figure 7 shows the current characteristics of the p-trig terminal of the first STSCR-LDMOS when the TLP current pulse is 800 mA. The increasing of the current of the p-trig terminal means that the base current of N_1 will decrease, which leads to the decrease of the collector current of N_1. Therefore, the effect of positive feedback between P_1 and N_1 is weakened, which results in the decrease of the magnification of the parasitic SCR. Finally, the holding voltage of the first STSCR-

LDMOS will increase, that is, the holding voltage of the proposed stacking structure increases.

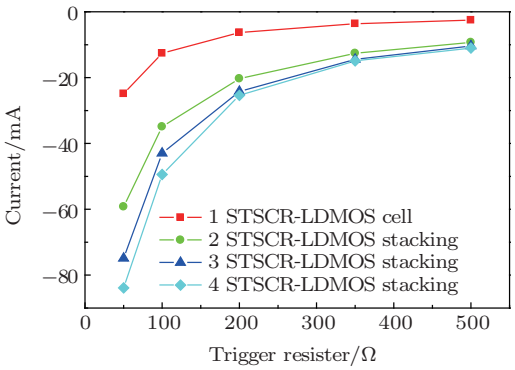


Fig. 7. (color online) Current characteristics of the p-trig terminal of the first STSCR-LDMOS.

According to the above analysis, trigger resistances R_1, R_2, and R_n have an important influence on the trigger voltage and holding voltage of the proposed stacked STSCR-LDMOS structure. The selection of resistance will determine the performance of the stacking structure. When the resistance is greater than 200 Ω, the excessively high trigger voltage cannot meet the requirements for the ESD protection device. When the resistance is less than 50 Ω, although the holding voltage of the proposed stacking structure increases, the current from the p-trig terminal of the first STSCR-LDMOS increases rapidly, which may produce a large amount of heat in the place where the breakdown of the first STSCR-LDMOS takes place, causing the failure current to decrease. Therefore, the best choice of the resistance should be in the range from 50 Ω to 200 Ω.

4. Conclusions

A novel stacked STSCR-LDMOS structure is proposed and simulated in a 0.35-μm, 60-V BCD process. The holding voltage can be adjusted by the number of stacking units, whereas the trigger voltage is determined mainly by the first STSCR-LDMOS. In this paper we discuss and prove that the best trigger resistance is in the range from 50 Ω to 200 Ω. A holding voltage of 30.6 V and a trigger voltage of 75.4 V are both achieved when the trigger resistance is 50 Ω. The high holding voltage and low trigger voltage of the proposed STSCR-LDMOS stacking structure make it very fascinating for high voltage ESD protection.

References

[1] Ker M D and Lin K H 2004 *IEEE J. Electron Dev. Lett.* **25** 640
[2] Liu Z W, Liou J J, Dong S R and Han Y 2010 *IEEE J. Electron Dev. Lett.* **31** 845
[3] Liu Y D, Du L, Sun P and Chen W H 2012 *Acta Phys. Sin.* **61** 137203 (in Chinese)
[4] Wang Y, Jia S, Chen Z J and Ji L J 2006 *Chin. Phys.* **15** 2297
[5] Fan H, Jiang L L and Zhang B 2013 *IEEE Trans. Dev. Mater. Reliability* **13** 50
[6] Markus P J M, Wolfgang W, Stephan M, Heinrich W, Andreas S and Wolfgang F 2000 *IEEE Trans. Electron Dev.* **47** 2128
[7] Chen W Y and Ker M D 2010 *IEEE J. Electron Dev. Lett.* **31** 159
[8] Zhang P, Wang Y, Jia S and Zhang X 2011 *IEEE EDSSC*, November 15–17, Tianjin, China, pp. 1–4
[9] Walker A J, Puchner H, and Dhanraj SP D 2009 *IEEE Trans. Electron Dev.* **56** 1753
[10] Ma F, Zhang B, Han Y, Zheng J F, Song B, Dong S R and Liang H L 2013 *IEEE J. Electron Dev. Lett.* **34** 1178
[11] Ker M D and Chen T Y 2003 *IEEE J. Solid-State Circuits* **38** 1380
[12] Wang Y, Jia S, Sun L, Zhang G G, Zhang X and Ji L J 2007 *Acta Phys. Sin.* **56** 7242 (in Chinese)
[13] Ker M D and Hsu K C 2002 *IEEE ISCAS* **5** V-529
[14] Zhu Z W, Hao Y, Zhang J F, Fang J P and Liu H X 2006 *Acta Phys. Sin.* **55** 5878 (in Chinese)
[15] Wu X P, Yang Y T, Gao H X, Dong G and Chai C C 2013 *Acta Phys. Sin.* **62** 047203 (in Chinese)
[16] Zhang B, Chai C C and Yang Y T 2010 *Acta Phys. Sin.* **59** 8063 (in Chinese)
[17] Ding K B and Huang D H 2013 *Acta Electron. Sin.* **41** 1016 (in Chinese)