Influences of fringing capacitance on threshold voltage and subthreshold swing of a GeOI metal-oxide-semiconductor field-effect transistor*

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Models of threshold voltage and subthreshold swing, including the fringing-capacitance effects between the gate electrode and the surface of the source/drain region, are proposed. The validity of the proposed models is confirmed by the good agreement between the simulated results and the experimental data. Based on the models, some factors impacting the threshold voltage and subthreshold swing of a GeOI metal-oxide-semiconductor field-effect transistor (MOSFET) are discussed in detail and it is found that there is an optimum thickness of gate oxide for definite dielectric constant of gate oxide to obtain the minimum subthreshold swing. As a result, it is shown that the fringing-capacitance effect of a short-channel GeOI MOSFET cannot be ignored in calculating the threshold voltage and subthreshold swing.

Keywords: GeOI metal-oxide-semiconductor field-effect transistor, fringing capacitance, subthreshold swing, threshold voltage

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1. Introduction

In order to maintain the scaling trend of complementary metal oxide semiconductor (CMOS) circuits in accordance with Moore's law, it is suitable to replace the conventional SiO_2/Si system with innovative device structures and new materials. The recent development of high-κ gate dielectrics suitable for Ge substrate and the high carrier mobility of Ge make GeOI metal-oxide-semiconductor field-effect transistor (MOSFET) has become a potential candidate for a new generation of CMOS technology. However, the use of high-κ gate dielectrics makes the fringing-capacitance effects of short-channel MOSFET more significant.[1–3] Bansal *et al.*[2] and Feng *et al.*[4] studied the fringing capacitance only between the right/left edge of gate electrode and the surface of source/drain region. Kumar *et al.*[5] studied the fringing capacitance only between the bottom of the gate electrode and the surface of source/drain region. Feng *et al.*[4] and Kumar *et al.*[5] also studied the influence of fringing capacitance on threshold voltage of MOSFET. However, they did not consider the edge-effect in capacitance of non-parallel plate capacitor when using the conformal mapping transformation. All of these models only considered the effect of some fringing capacitance on the threshold voltage, and they have ignored the fringing capacitance between the top of the gate electrode and the surface of the source/drain region. Moreover, the influence of the fringing capacitance on the subthreshold swing of MOSFET is hardly involved.

In this work, all kinds of fringing capacitance between the gate electrode and the surface of source/drain region and the edge-effect in capacitance of non-parallel plate capacitor are considered to build models of both the threshold voltage and the subthreshold swing. Our simulated results are in good agreement with the experimental data.

2. Device structure and model

The fringing-capacitance model of the GeOI MOSFET is shown in Fig. 1, where C_1 is the fringing capacitance between the bottom of the gate electrode and the surface of source/drain region, C_2 is the fringing capacitance between the right/left edge of gate electrode and the surface of the source/drain region including the edge effect in capacitance of non-parallel plate capacitor, C_3 is the fringing capacitance between the top of the gate electrode and the surface of the source/drain region, L is the channel length, and L_a is the width of the source/drain region.

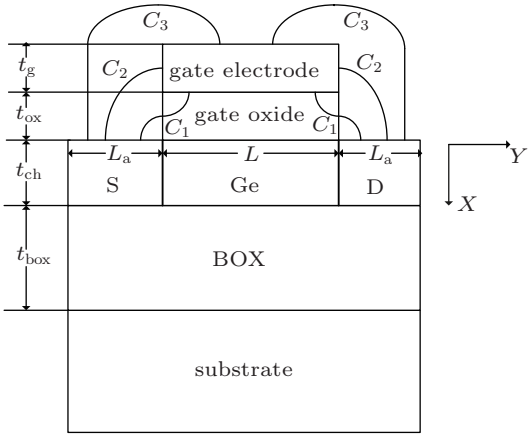


Fig. 1. Schematic fringing-capacitance model of a GeOI MOSFET.

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2.1. Fringing capacitance

Fringing capacitance C_1 can be expressed as[5]

$$C_1 = \frac{2k_{ox}k_s}{\pi(k_{ox}-k_s)L_a}\ln\left(\frac{k_{ox}}{k_s}\right), \tag{1}$$

where k_{ox} is the dielectric constant of the gate oxide and k_s is the dielectric constant of the spacer. Here, C_{2i} is defined as the fringing capacitance between the right/left edge of gate electrode and the surface of source/drain region without the edge effect in the capacitance of the non-parallel plate capacitor, which can be expressed as[4]

$$C_{2i} = \frac{2k_s}{\pi L_a}\cosh^{-1}\left(\frac{t_{ox}+t_g}{t_{ox}}\right), \tag{2}$$

where t_{ox} is the thickness of gate oxide and t_g is the thickness of gate electrode. The C_{2fi} is defined as the fringing capacitance generated by the edge effect in the capacitance of the non-parallel plate capacitor. It can be calculated by Schwarz–Christoffel transformation[6] and expressed as

$$C_{2fi} = \frac{k_s}{\pi L_a}\left(\ln\left(1+2\ln\left(\frac{t_{ox}+t_g}{t_{ox}}\right)\right)+1\right). \tag{3}$$

Therefore, C_2 can be written as

$$C_2 = C_{2i}+C_{2fi}, \tag{4}$$

and C_3 can be obtained by conformal mapping transformation by assuming that the length of the parallel plate capacitor on top of the gate electrode is equal to L_a,

$$C_3 = \frac{k_s}{\pi L_a}\ln\left(1+\frac{L_a}{t_{ox}+t_g}\right). \tag{5}$$

Thus, the total fringing capacitance C_{of} between the gate electrode and the surface of source/drain region is the sum of C_1, C_2, and C_3.

2.2. Threshold voltage

Kumar *et al.*[5] assumed that the charge distribution induced in the source and drain regions due to the fringing electric field is uniform, with the charge densities of source and drain regions Q_s and Q_d given, respectively, by

$$Q_s = (C_1+C_2+C_3)(V_{bi}-V_g+V_{fb}), \tag{6}$$

$$Q_d = (C_1+C_2+C_3)(V_d+V_{bi}-V_g+V_{fb}), \tag{7}$$

where V_{bi} is the built-in potential of source/drain-channel junction, V_g is the gate voltage, V_{fb} is the flat-band voltage of the front gate, and V_d is the drain voltage. The surface potential due to this uniform charge distribution along the channel can be expressed as

$$\Delta\phi_s(y) = \frac{1}{2}\int_0^{L_a}\int_{-w/2}^{w/2}\frac{Q_s\,dy_1\,dy_2}{4\pi k_{ch}\sqrt{(y+y_1)^2+(y_2)^2}} + \frac{1}{2}\int_0^{L_a}\int_{-w/2}^{w/2}\frac{Q_d\,dy_1\,dy_2}{4\pi k_{ch}\sqrt{(y+y_1)^2+(y_2)^2}}, \tag{8}$$

where k_{ch} is the the dielectric constant of channel. According to Young's model,[7] the surface potential of a GeOI MOSFET without fringing capacitance can be expressed as

$$\phi_s(y) = Ae^{\lambda y}+Be^{-\lambda y}+C, \tag{9}$$

where

$$\lambda = \sqrt{\alpha},\quad A = \frac{(V_{bi}-C)(e^{\lambda L}-1)+V_d e^{\lambda L}}{e^{2\lambda L}-1},$$

$B = V_{bi}-C-A$, $C = -\beta/\alpha$, and α, β can be written as

$$\alpha = \frac{2\left(1+\frac{C_{ox}}{C_{ch}}+\frac{C_{ox}}{C_{box}}\right)}{t_{ch}^2\left(1+2\frac{C_{ch}}{C_{box}}\right)}, \tag{10}$$

$$\beta = -\frac{qN_{ch}}{k_{ch}}-\frac{2}{t_{ch}^2\left(1+2\frac{C_{ch}}{C_{box}}\right)} \times\left[V_{sub}-V_{fbsub}+\left(\frac{C_{ox}}{C_{ch}}+\frac{C_{ox}}{C_{box}}\right)(V_g-V_{fb})\right], \tag{11}$$

where C_{ox} is the gate oxide capacitance, C_{ch} is the channel capacitance, C_{box} is the buried oxide capacitance, t_{ch} is the channel thickness, N_{ch} is the channel doping concentration, V_{sub} is the substrate voltage, and V_{fbsub} is the flat-band voltage of the back gate. The threshold voltage V_{th1} without considering the fringing capacitance is defined as $\phi_{s\max} = 2\varphi_f$ ($\phi_{s\max}$ is the maximum surface potential occurred at $y_{max} = L/2$ and φ_f is the Fermi potential) for small V_d, and can be written as

$$V_{th1} = V_{fb}-\frac{t_{ch}^2(1+2C_{ch}/C_{box})}{2(C_{ox}/C_{ch}+C_{ox}/C_{box})} \times\left[\frac{(D-2\varphi_f)\alpha}{E}+\frac{qN_{ch}}{k_{ch}}+\frac{2(V_{sub}-V_{fbsub})}{t_{ch}^2(1+2C_{ch}/C_{box})}\right], \tag{12}$$

with

$$D = \left(\frac{V_{bi}}{e^{\lambda L}+1}+\frac{V_d e^{\lambda L}}{e^{2\lambda L}-1}\right)(e^{\lambda L/2}-e^{-\lambda L/2}) + V_{bi}e^{-\lambda L/2}, \tag{13}$$

$$E = 1-e^{-\lambda L/2}-\frac{e^{\lambda L/2}-e^{-\lambda L/2}}{e^{\lambda L}+1}. \tag{14}$$

When the fringing capacitance is considered, the surface potential $\phi_s'(y)$ can be modified as

$$\phi_s'(y) = \phi_s(y)+\Delta\phi_s(y). \tag{15}$$

Thus, the threshold voltage with the fringing capacitance V_{th2} can be gotten by setting $\phi_{s\max}' = 2\varphi_f$,

$$V_{th2} = \frac{2\varphi_f-F}{\frac{E}{\alpha}\frac{2(C_{ox}/C_{ch}+C_{ox}/C_{box})}{t_{ch}^2(1+2C_{ch}/C_{box})}-\frac{MC_{of}}{4\pi k_{ch}}}, \tag{16}$$

where

$$F = D + \frac{MC_{\rm of}}{8\pi k_{\rm ch}}(V_{\rm d} + 2V_{\rm bi} + 2V_{\rm fb}) + \frac{E}{\alpha}\frac{qN_{\rm ch}}{k_{\rm ch}} + \frac{E}{\alpha}\frac{2(V_{\rm sub} - V_{\rm fbsub})}{t_{\rm ch}^2(1 + 2C_{\rm ch}/C_{\rm box})} - \frac{E}{\alpha}\frac{2V_{\rm fb}(C_{\rm ox}/C_{\rm ch} + C_{\rm ox}/C_{\rm box})}{t_{\rm ch}^2(1 + 2C_{\rm ch}/C_{\rm box})}, \quad (17)$$

$$M = \int_0^{L_{\rm a}} \int_{-w/2}^{w/2} \frac{{\rm d}y_1\,{\rm d}y_2}{\sqrt{(y + y_1)^2 + (y_2)^2}}. \quad (18)$$

2.3. Subthreshold swing

The charges induced in the source and drain regions introduce an additional surface potential in the channel region and impact the subthreshold swing. The subthreshold swing can be expressed as

$$S = \ln(10)/\left(\frac{{\rm d}(\ln I_{\rm D})}{{\rm d}V_{\rm g}}\right) = \ln(10)/\left(\frac{{\rm d}(\ln I_{\rm D})}{{\rm d}\phi_{\rm s}}\frac{{\rm d}\phi_{\rm s}}{{\rm d}V_{\rm g}}\right), \quad (19)$$

$$\frac{{\rm d}(\ln I_{\rm D})}{{\rm d}\phi_{\rm s}} = \left(\frac{q}{KT} - \frac{({\rm d}/{\rm d}\phi_{\rm s})(-{\rm d}\phi_{\rm s}/{\rm d}x)}{-{\rm d}\phi_{\rm s}/{\rm d}x}\right) = \left(\frac{q}{KT} - {\rm tomd}\right), \quad (20)$$

with

$${\rm tomd} = \frac{k_{\rm ox}}{k_{\rm ch}t_{\rm ox}E_{\rm s}}, \quad (21)$$

where K is the Boltzmann constant, tomd is an intermedium variable, and $E_{\rm s}$ is the electric field at the channel surface and can be written as

$$E_{\rm s} = \frac{k_{\rm ox}}{k_{\rm ch}}\frac{\phi_{\rm s} - V_{\rm g} + V_{\rm fb}}{t_{\rm ox}}. \quad (22)$$

It is worth pointing out that the use of high-κ gate dielectrics would give rise to the problem of carrier-mobility degradation due to the coupling of soft optical phonon modes in high-κ to the inversion channel charge carriers,[8,9] i.e., phonons scatter electrons in channel, which, however, is not involved in the above models and will be investigated in detail in our next-step work for the GeOI MOSFET.

3. Results and discussion

Based on the above model, the threshold voltages and subthreshold swings with/without the fringing-capacitance effect are simulated and compared with the experimental data,[10,11] as shown in Fig. 2. It can be seen that the subthreshold swing considering all of the fringing capacitance is closer to the experimental data than the other two simulated results (the inversion electron density is considered when solving the Poisson equation of Young's model), and the threshold voltage considering all the fringing capacitance is also more accurate than the other two models, especially for $L < 70$ nm, indicating that all fringing capacitance including $C_{\rm 2fi}$ and C_3 must be considered to accurately simulate the threshold voltage and subthreshold swing of a small GeOI MOSFET.

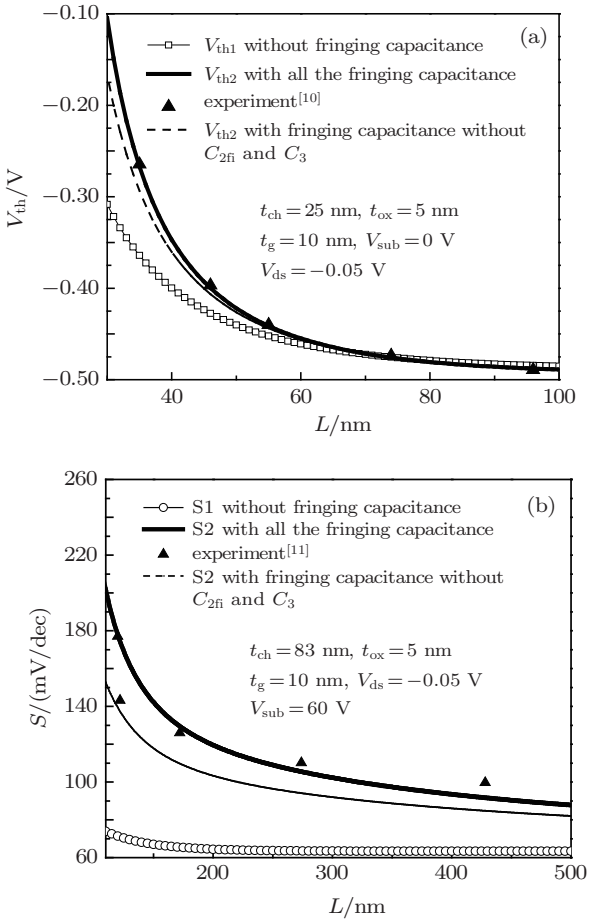


Fig. 2. Simulated and experimental threshold voltages (a) and subthreshold swing with/without the fringing-capacitance effect (b).

The $\Delta V_{\rm th}$ is defined as the difference between the threshold voltages with/without the fringing capacitance to further evaluate the influences of the fringing capacitance on the threshold voltage. Figures 3(a)–3(c) show the influences of channel length L, gate electrode thickness $t_{\rm g}$, and gate oxide thickness $t_{\rm ox}$ on $\Delta V_{\rm th}$, respectively. As can be seen from Fig. 3, the effect of the fringing capacitance on threshold voltage is enhanced as the channel length shrinks due to the shortened distance between the middle of the channel and the fringing field in the source/drain region; $\Delta V_{\rm th}$ is increased with increasing $t_{\rm g}$ due to the increased fringing capacitance C_2, as shown in the inset in Fig. 3(b). Although C_3 is also decreased with increasing $t_{\rm g}$, C_3 is much smaller than C_2 and the total fringing capacitance $C_{\rm of}$ is dominated by C_2. Similarly, as gate oxide thickness decreases, $\Delta V_{\rm th}$ is increased, as shown in Fig. 3(c). In other words, a thinner gate electrode and thicker gate oxide can alleviate the effects of the fringing capacitance on the threshold voltage of GeOI MOSFET.

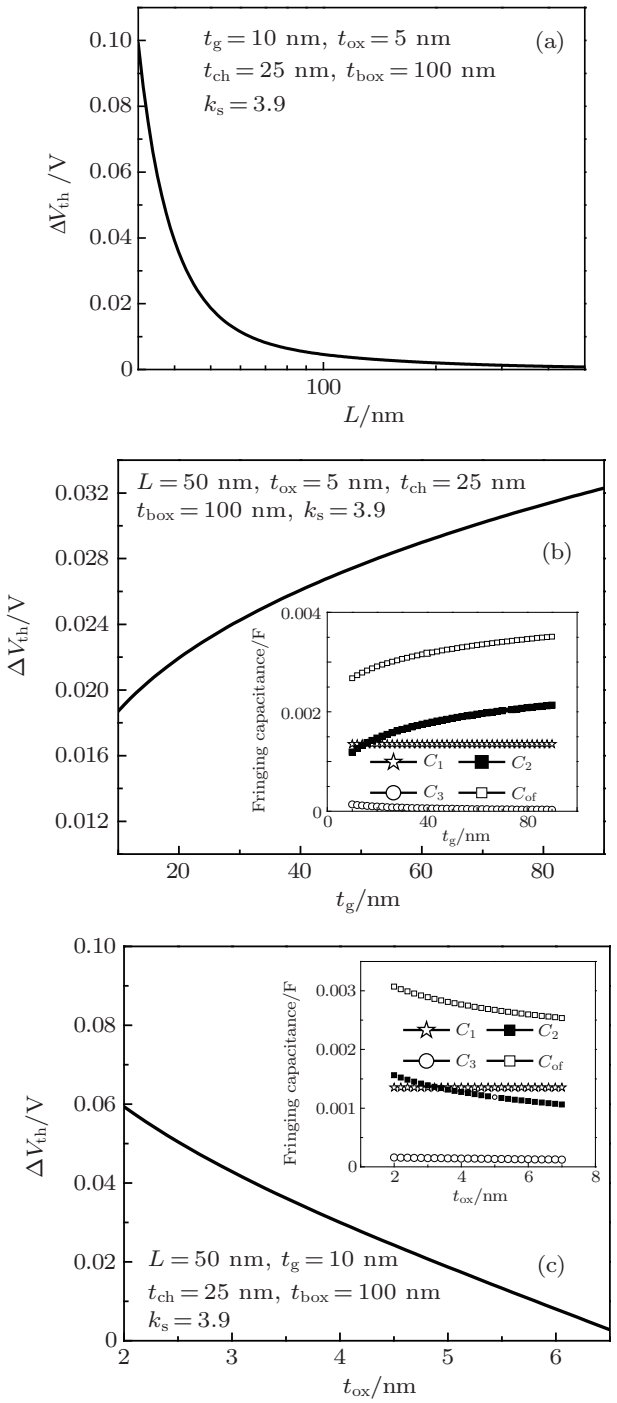


Fig. 3. Influences of the fringing capacitance on threshold voltage for different (a) channel lengths, (b) gate electrode thickness, (c) gate oxide thickness. The insets show variation of fringing capacitance as a function of (b) gate electrode thickness, (c) gate oxide thickness.

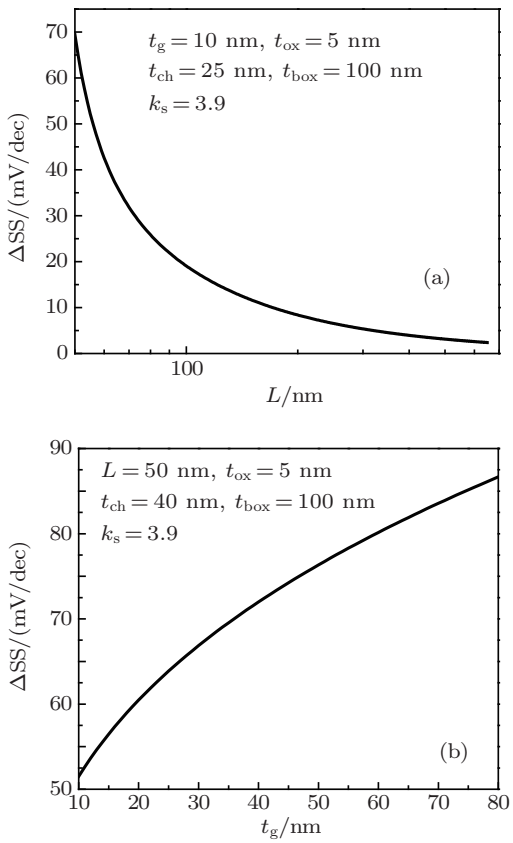


Fig. 4. Influences of the fringing capacitance on subthreshold swing for different (a) channel lengths and (b) gate electrode thicknesses.

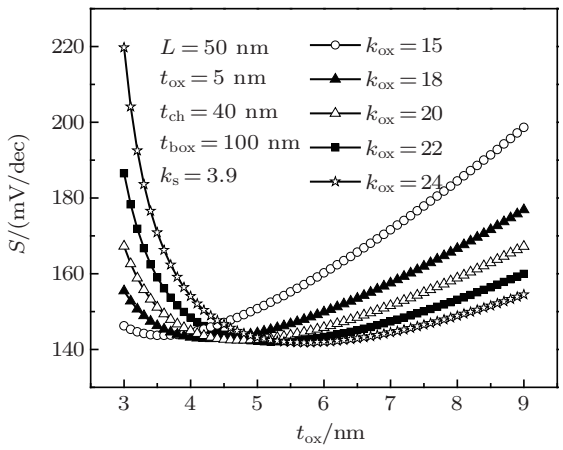


Fig. 5. Variation of subthreshold swing with fringing capacitance as a function of gate oxide thickness under different dielectric constants of gate oxide.

The ΔSS is defined as the difference between the subthreshold swings with/without the fringing capacitance. Figures 4(a) and 4(b) depict the changes of ΔSS with the Ge channel length and gate electrode thickness, respectively. It can be seen from Fig. 4(a) that the influence of the fringing capacitance on subthreshold swing is weakened as the channel length increases because the potential in the channel induced by the fringing field is decreased. ΔSS is increased with increasing t_g, as shown in Fig. 4(b), due to the same reason as ΔV_{th} in Fig. 3(b).

Figure 5 shows the change of the subthreshold swing with t_{ox} for different dielectric constants of gate oxide when fringing capacitance is considered. In simulation, the subthreshold current controlled by ϕ_s remains the same for different t_{ox} and k_{ox}, and so the gate voltage V_g is assumed to be $V_g = V_{th2} + 0.05$ to make the MOSFET in the subthreshold region with $\phi_s = -0.49$. It is found from Fig. 5 that as t_{ox} increases, the subthreshold swing is decreased first and it then increased. This happens because when V_{th2} is decreased, E_s is increased due to the same ϕ_s for different t_{ox}, so that tomd and $d\phi_s/dV_g$ are decreased as t_{ox} increases, and thus the

subthreshold swing as a function of t_{ox} exhibits a parabolic curve. In addition, It can be seen that the minimum subthreshold swing occurs at different t_{ox} for different k_{ox}. Therefore, there is an optimal t_{ox} for definite k_{ox} to obtain the best subthreshold behaviors, e.g., t_{ox} is in the range of 3.6–5.7 nm for $15 \leq k_{ox} \leq 24$. Moreover, it can be observed that the larger the k_{ox} is, the smaller the change of subthreshold swing with t_{ox} beyond the optimal t_{ox}, which permits a wider-range for the choice of the gate oxide thickness.

4. Summary

Various kinds of fringing capacitance between the gate electrode and the surface of source/drain region are considered to build models of the threshold voltage and subthreshold swing of GeOI MOSFET. Good agreement between the simulated results and experimental data is obtained, confirming the validity of the proposed models. The simulated results show that the fringing-capacitance effect cannot be ignored for a short-channel GeOI MOSFET, and the thin gate electrode can alleviate the impacts of fringing capacitance on threshold voltage and subthreshold swing, and there is an optimal thickness of gate oxide for the definite dielectric constant of the gate oxide for achieving the best subthreshold behaviors.

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