Charge trapping in surface accumulation layer of heavily doped junctionless nanowire transistors*

Ma Liu-Hong(马刘红), Han Wei-Hua(韩伟华)†, Wang Hao(王 昊), Yang Xiang(杨 香), and Yang Fu-Hua(杨富华)‡

Engineering Research Center for Semiconductor Integration Technology, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, *China*

(Received 5 May 2015; revised manuscript received 21 August 2015; published online 20 October 2015)

We investigate the conductivity characteristics in the surface accumulation layer of a junctionless nanowire transistor fabricated by the femtosecond laser lithography on a heavily n-doped silicon-on-insulator wafer. The conductivity of the accumulation region is totally suppressed when the gate voltage is more positive than the flatband voltage. The extracted low field electron mobility in the accumulation layer is estimated to be 1.25 $cm^2 \cdot V^{-1} \cdot s^{-1}$. A time-dependent drain current measured at 6 K predicts the existence of a complex trap state at the Si–SiO_2 interface within the bandgap. The suppressed drain current and comparable low electron mobility of the accumulation layer can be well described by the large Coulomb scattering arising from the presence of a large density of interface charged traps. The effects of charge trapping and the scattering at interface states become the main reasons for mobility reduction for electrons in the accumulation region.

Keywords: junctionless nanowire transistors, trap, femtosecond laser lithography, electron mobility

PACS: 81.07.Gf, 73.63.–b, 73.40.–c, 85.30.Tv **DOI:** 10.1088/1674-1056/24/12/128101

1. Introduction

Recent years have witnessed the rapid downscaling of field effect transistors, causing many adverse issues such as short channel effect. In particular, it becomes exceedingly arduous to form abrupt p–n junctions between the source/drain and channel as the gate length is reduced down to 10 nm or even less. Recently, a unified heavily-doped nanowire resistor, called a "junctionless nanowire transistor (JNT)", has captured great attention as a promising candidate for the further continuation of Moore's law because of the excellent gate control ability and simplified fabrication process.[1–4] The channel is fully depleted in subthreshold operation. Threshold voltage is reached when the central region of the nanowire becomes neutral. The depletion region decreases as the gate voltage further increases.[5] The flatband voltage is defined as the applied gate voltage which enforces flat bands at the insulator–semiconductor interface. The JNT has a bulk neutral conduction path less affected by the transverse electric field from the gate than by the surface accumulation layer separated by the flatband voltage (V_{fb}). The accumulation carriers are confined to a very thin layer along the silicon–gate oxide interface by the electric field originating from the gate electrode. Owing to the large surface-to-bulk aspect ratio, the trapping and detrapping of the surface defects at the Si–SiO_2 interface become crucial in the nanowire transistor. It has been reported that Coulomb scattering introduced by charged interface traps can become a dominant mechanism of mobility degradation for metal–oxide–semiconductor field-effect transistors (MOSFETs) in low field regime.[6] In the accumulation region of JNTs, the charges trapped at the interface might work as the Coulomb scattering centers for carriers in the channel. The carrier mobility might be degraded by the trapped charges at the interface due to the reduced distance between the carrier in the accumulation layer and the Coulomb scattering center. Many of the research studies on JNTs have focused on the neutral channel region. However, relatively little work has been done to analyze the accumulation layer of the silicon nanowire channel. The present work aims at analyzing the electrical properties of JNT in the linear accumulation region under the condition of the silicon surface with the influence of interface traps.

The key to fabricating the JNTs is the formation of a ultranarrow channel to ensure the full depletion of carriers in the channel under zero gate voltage. Therefore, it is important to achieve the line size on the order of tens of nanometers. For decades, photolithography has been the predominant method for MOSFET fabrication. Since costs for lithographic equipment and mask sets keep rising with every technology generation, alternative cheaper patterning techniques are earnestly required. The femtosecond laser lithography has a host of advantages including no mask, three dimensions, high resolution and rapid prototyping, which make the lithography an attractive method of fabricating the nanostructures.[7,8] In

*Project supported by the National Natural Science Foundation of China (Grant Nos. 61376096, 61327813, and 61404126) and the National Basic Research Program of China (Grant No. 2010CB934104).

†Corresponding author. E-mail: weihua@semi.ac.cn

‡Corresponding author. E-mail: fhyang@semi.ac.cn

© 2015 Chinese Physical Society and IOP Publishing Ltd

this approach, the focused femtosecond laser beam is used to directly write the desired image into the photoresist without lithographic masks. Furthermore, previous theoretical and experimental results have shown that femtosecond laser with two-photon or multiphoton absorption has a potential to exceed the diffraction limit due to the nonlinear effect.[9–11] The development of this novel maskless lithography has a tremendous potential for opening a new nanomanufacturing market in the future. In the present work, we demonstrate the fabrication of n-type single-channel JNT on a silicon-on-insulator (SOI) substrate by two-photon absorption process. Two dry etching processes are implemented to transfer the desired image from the negative photoresist SCR500 onto the top silicon layer. Suppressed conductivity and degraded electron mobility are observed in the accumulation region, due to the generation of new important scattering mechanisms especially Coulomb scattering arising from the charged defects at the Si–SiO_2 interface.

2. Device fabrication

Figure 1 shows the schematic diagrams of the fabrication process of JNTs. The devices were fabricated on a (100)-oriented SOI substrate with a top Si thickness of 55 nm. After thermally growing 15-nm silicon dioxide, the SOI wafer was uniformly and heavily doped by phosphorus ion implantation with a dose of 5×10^{13} cm^{-2}, leading to a uniform concentration of 1×10^{19} cm^{-3}. It was followed by the deposition of 50-nm SiO_2 on top of Si. The SiO_2 layer was chosen to minimize the interference effect of femtosecond laser and eliminate the silicon surface damage directly induced by direct laser scanning.[12] Afterwards, two laser beams with optimized wavelengths and powers were used to pattern a nanowire connecting two pads.[13] The laser beams focused by an objective lens were scanned into the substrate covering negative photoresist by adjusting the position of the translational stage. The desired image was transferred from negative photoresist onto the top silicon layer by two-step inductively coupled plasma (ICP) etching processes as presented in Figs. 1(c)–1(f). First, the deposited SiO_2 layer was etched with photoresist as a hard mask, and the top silicon layer was etched with SiO_2 as a mask. After rinsing in the HF solution, the Si nanowire was suspended by corroding the buried oxide layer. The scanning electron microscope (SEM) image presented in the insert of Fig. 2(a) shows that the width of the nanowire channel is 47 nm on average and the length of nanowire is about 500 nm. After removing the SiO_2 mask by 5% HF, the sample was oxidized in dry oxygen at 900 °C for 1 h, resulting in the formation of a Si core with a height of 28 nm (T_{si}) and a width of 27 nm (W_{si}). The thickness of SiO_2 gate dielectric formed by thermal oxidation is about 22 nm. A 200-nm-thick poly-silicon was then deposited by low-pressure chemical vapor deposition on the gate oxide layer. The poly-silicon was doped by arsenic ion implantation at a dose of 2×10^{15} cm^{-2}, leading to a doping level of approximately 1×10^{20} cm^{-3} after annealing at 1000 °C for 10 s. The gate electrode pads were fabricated by evaporating a 20-nm-thick Ti film to form a Ni/Si ohmic contact, and then 300-nm-thick Al film is used for final metallization via conventional optical lithography.

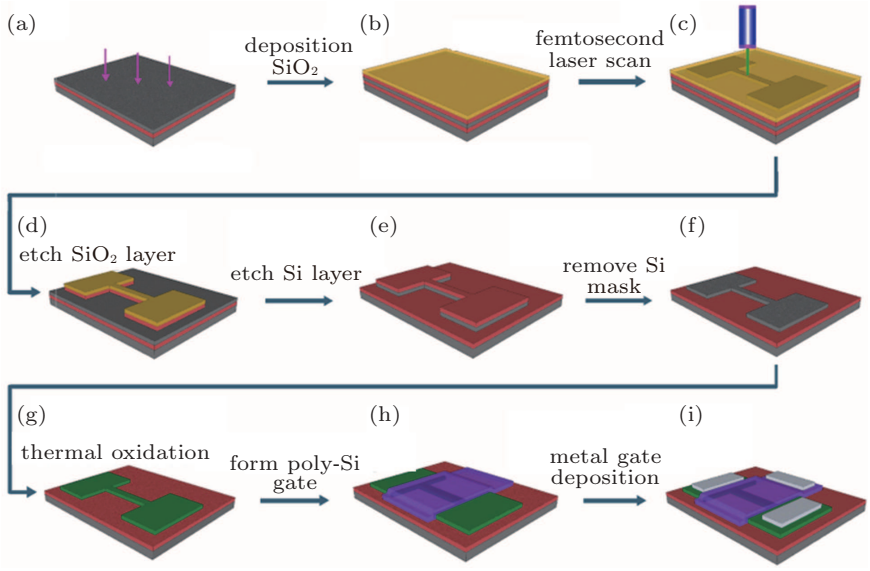


Fig. 1. (color online) Schematic diagrams of the fabrication process for JNTs.

3. Results and discussion

The device is placed in a vacuum chamber which can be cooled down to ∼ 6 K with the help of Lakershore-340 temperature controller. The electrical characteristics of the transistor are investigated by Agilent B1500 semiconductor parameter analyzer. Figure 2(a) shows the drain current and volt-

age (I_{DS}–V_{GS}) characteristic curves of the JNT measured at room temperature. The threshold voltage V_{th} is approximately 0.62 V. As can be seen in the logarithmic scale of Fig. 2(a), I_{DS} is almost independent of V_{GS} beyond the flatband voltage V_{fb} whose value is determined in Fig. 2(b). It suggests that the electron mobility is relatively low in higher V_{GS}. In addition, it should be noted that I_{DS} is only tens of nA, which is totally suppressed.

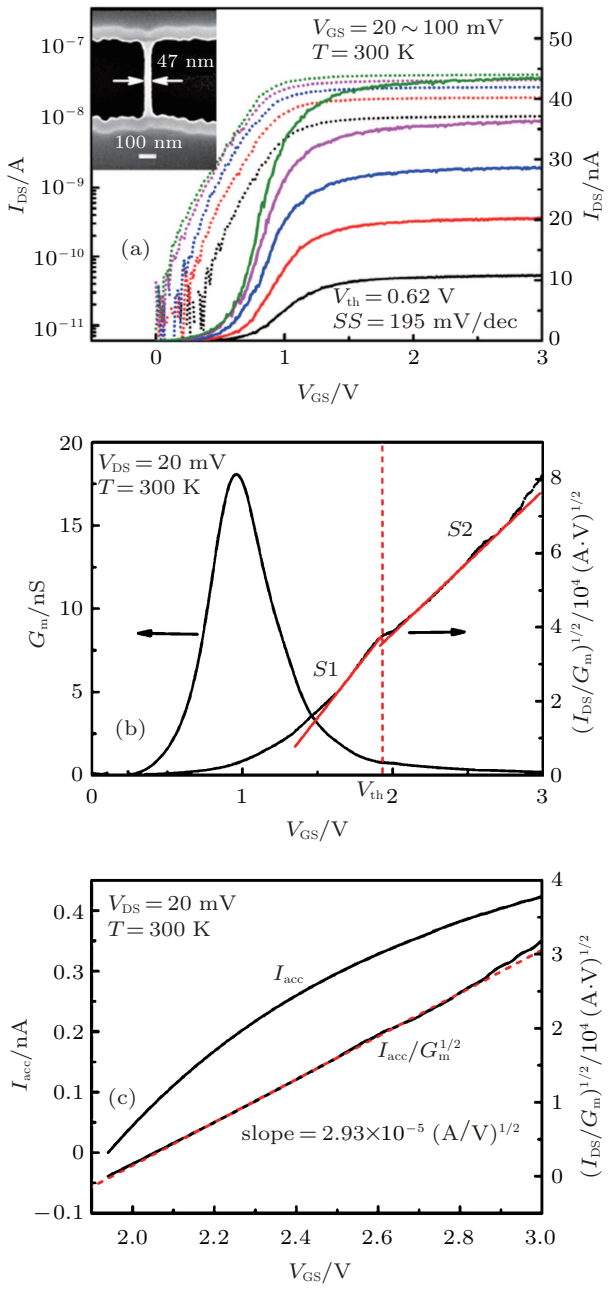


Fig. 2. (color online) Electrical performances of JNT measured at room temperature. (a) I_{DS}–V_{GS} curves for V_{DS} values ranging from 20 mV to 100 mV in steps of 20 mV in both linear and logarithmic scale. The insert shows the SEM image of the nanowire after removing the SiO_2 mask. (b) The transconductance G_m as a function of V_{GS} at $V_{DS} = 20$ mV and the corresponding $I_{DS}/\sqrt{G_m}(V_{GS})$ for the device. (c) The drain current of accumulation layer I_{acc} and corresponding Y-function at $V_{DS} = 20$ mV.

Low field mobility represents the upper limit of carrier mobility for a given device. The Y-function ($Y(V_{GS}) = I_{DS}/\sqrt{G_m}$) method,[14] which eliminates the influence of mobility degradation factor and series resistance, is used for accurately extracting the low field mobility of MOSFET. In this approach, the value of carrier mobility is related to the slope of Y-function. Figure 2(b) exhibits the transconductance G_m and the total Y-function of JNT. It is worth emphasizing that there are two kinds of slopes $S1$ and $S2$ in Y-function. Based on the operation principle of JNT, two conduction mechanisms can make a distinction by the flatband voltage V_{fb} between the bulk natural channel and the additional surface accumulation channel.[15] In particular, the neutral conduction path, created in the center of the silicon body, is free of perpendicular fields. Thereby, the majority carriers can flow through the neutral conduction path without the influence of surface effects under the flatband condition. While above V_{fb}, a large number of electrons accumulate at the surface accumulation channel. Under this condition, the carrier mobility of the accumulation layer is seriously degenerated with increasing V_{GS} under the influence of surface effect. Those two kinds of slopes in Fig. 2(b) on the Y-function just manifest two different types of conduction mechanisms separated by V_{fb}. Hence, V_{fb} can be extracted from the slope turning point of Y-function. As can be seen from Fig. 2(b), the value of flatband voltage is approximately 1.93 V. The voltage spacing between V_{th} and V_{fb} is relatively large due to high doping concentration.[16] For the accumulation operation, the total current within the linear regime can be modeled as[17]

$$I_{DS}(V_{DS}) = \frac{W}{L}\frac{\mu_{acc}}{1+\theta_0(V_{GS}-V_{fb})} \times C_{ox}(V_{GS}-V_{fb})V_{DS} + I_{bulk}, \quad (1)$$

where W, L, μ_{acc}, θ_0, and C_{ox} represent the effective channel width, channel length, accumulation channel mobility, mobility attenuation factor and oxide capacitance per unit area, respectively. The first term on the right-hand side of Eq. (1) represents the accumulation current I_{acc} and the second term represents the bulk current in flatband conduction, which can be written as $I_{bulk} = W_{Si}/L \times q\mu_{bulk}N_dT_{Si}V_{DS}$. Here μ_{bulk} is the bulk channel mobility and N_d is the doping concentration. To obtain accurate and low field electron mobility of the accumulation layer, the bulk current I_{bulk} in flatband conduction should be subtracted from the total current I_{DS}. Y-function of accumulation current can be expressed as $Y_{acc} = I_{acc}/\sqrt{G_m}$, where the transconductance G_m denotes $\partial I_{acc}/\partial V_{GS}$.

Figure 2(c) shows the I_{acc} separated by I_{DS}–I_{bulk} at V_{fb} and Y_{acc} of the accumulation channel at $V_{DS} = 20$ mV. It should be noted that Y_{acc} as a function of V_{GS} shows only one single slope now. Finally, the low field mobility of the accumulation channel extracted from the square of Y_{acc} slope is $\mu_{acc} = 1.25$ cm^2·V^{-1}·s^{-1}. The effective channel width W equals $2(W_{Si} + T_{Si})$, and the channel length approximately

equals the nanowire length of 500 nm. The slope of $S2$ in Fig. 2(b) is a combined result of the bulk conduction and the accumulation conduction.

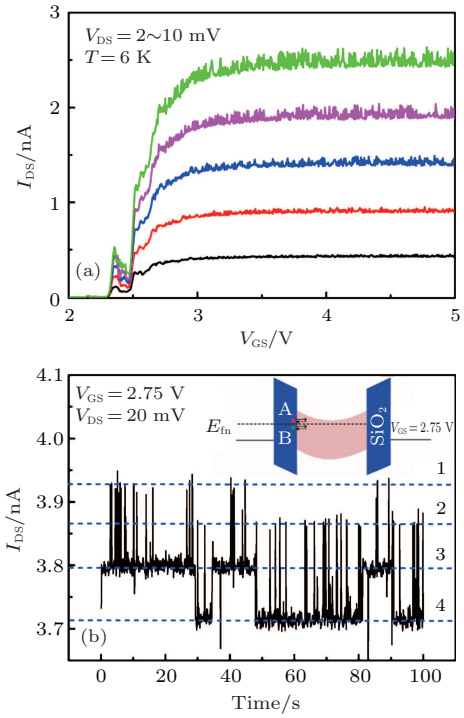


Fig. 3. (color online) Electrical performance of n-type JNT at low temperature of 6 K. (a) I_{DS}–V_{GS} curves for different V_{DS} values from 2 mV to 10 mV in steps of 2 mV. (b) Time domain current levels. Typical segment of a full 100-s I_{DS} versus time trace at $V_{GS}=2.75$ V and $V_{DS}=20$ mV. Four current levels observed at 6 K are ascribed to the capture and emission of electrons from two different traps.

To further investigate the degradation mechanisms behind this low value of low field mobility, we measure the low temperature electrical properties of JNT. Figure 3(a) shows I_{DS}–V_{GS} curves with V_{DS} values ranging from 2 mV to 10 mV at a temperature of 6 K. Obvious current jumps are observed. The amplitudes of those current jumps increase with increasing V_{DS}. Typical time dependence of the drain current at $V_{DS}=20$ mV, measured in steps of 0.1 s for a total time interval of 100 s, is indicated in Fig. 3(b). The applied gate bias is 2.75 V. We could observe multiple current levels. It has been argued that this phenomenon could be due to the trapping and detrapping behavior of multiple traps, which will cause more dramatic conduction fluctuations of the drain current. The high current level corresponds to the empty trap state, while the low current level is related to the electrons captured by the traps. The observed four-level fluctuations show that two single-charge-state traps located within $\sim 2k_BT$ of the Fermi level in the channel contribute to the current jumps.[18] The insert in Fig. 3(b) illustrates the band diagram for $V_{GS}=2.75$ V with two types of interface traps. Figure 4 manifests the histograms of the time domain random telegraph signals of the JNT at different V_{GS} values of 2.4 V, 2.65 V, 2.75 V, and 2.9 V. The drain bias is constant at 20 mV. Complex current levels are observed as the gate voltage increases, strongly suggesting the existence of multiple types of traps. Four current levels observed at 2.4 V are ascribed to capture and emission of electrons from the other two different traps within $\sim 2k_BT$ range just like the situation of 2.75 V, while two current levels at 2.65 V and 2.95 V are due to the other two single level traps.[19] The femtosecond laser gives rise to non-direct damage to the top silicon layer because of the deposition of 50-nm SiO_2. In general, the traps at Si–SiO_2 interface may be induced by etching procedure.

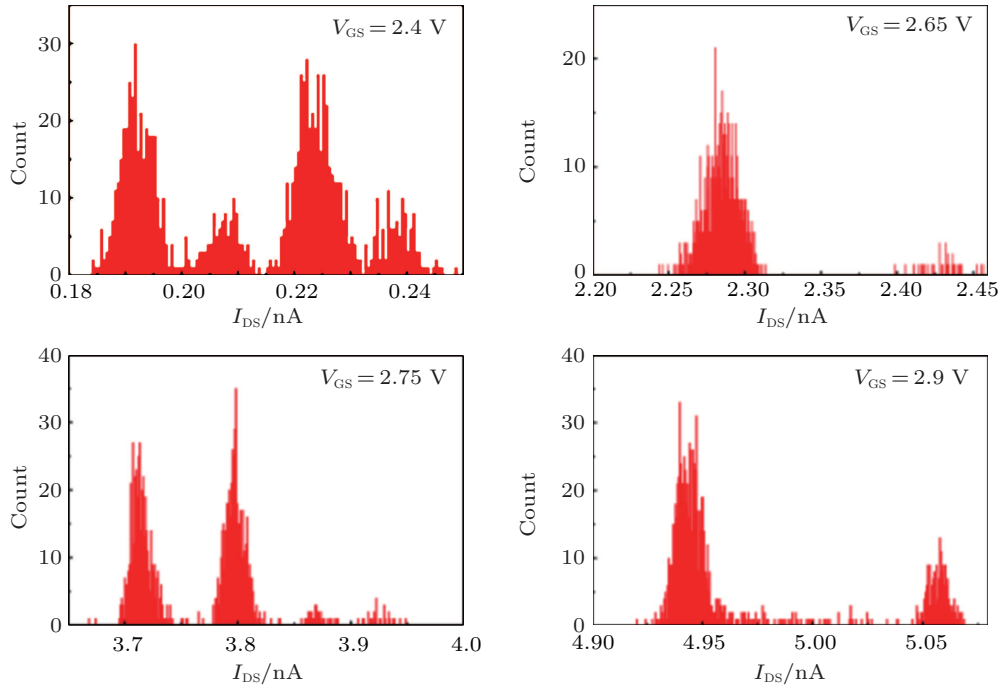


Fig. 4. (color online) Histogram of time-domain data of JNT measured at 6 K with $V_{DS}=20$ mV.

The charged traps can influence the electrical performance at large gate overdrives especially above flatband voltage, where we notice a current saturation with increasing V_{GS}. This can be easily explained by the increase of Coulomb scattering of the charged traps at the increased gate voltage. As previously stated, the squeezing of the carriers toward the Si–SiO_2 interfaces induces a reduced distance between the carriers of the accumulation layer and the charged traps as Coulomb scattering centers. The interface traps cause the increase of Coulomb scattering, which will eventually reduce the drive current. Furthermore, the influence of surface roughness scattering on electron mobility is very weak above V_{fb} because of the low perpendicular electric field of the accumulation layer in JNT compared with the scenario of inversion transistor. Actually, the extracted accumulation electron mobility in Ref. [17] is much higher without the influence of charged traps, inferring that charged trap scattering is the dominant scattering mechanism in this experiment. Hence, the charged traps have a detrimental influence on the performances of the device with a degenerated mobility in accumulation layer and the reduction of the gate-control ability.[20] Furthermore, one may consider that a large density of charged traps may form clusters of charges with high probability. In some cases, those charges of clusters work as a potential barrier, for electrons may form localized states, making electrons of the accumulation layer arduously transported through the channel. At room temperature, there will be additional charged traps activated by thermal energy around the Si–SiO_2 surface. The flatband voltage is influenced by charges that are trapped in the insulator-semiconductor interface or within the gate dielectric. Thus, more positive gate voltage should be used to reach the flatband condition than the previous theoretical value under the condition of the same doping concentration.[21] The above-mentioned results suggest that the carrier transport is trap-limited in the accumulation layer.

4. Conclusions

In this work, the JNTs each with a physical channel cross-section area of 27 nm×28 nm are fabricated by femtosecond laser lithograph. The low field mobility is found to be totally suppressed above the flatband voltage, due to the increased Coulomb scattering induced by charged traps at the Si–SiO_2 interface. The Coulomb scattering introduced by charged traps becomes the dominated scattering mechanism of electron transport in accumulation region. Our result shows that charged interface traps play a significant role in degrading the mobility of JNT especially in the accumulation layer above flatband voltage. Those findings clearly highlight the drastic influence of the large density of charged traps on the mobility degradation for the accumulation layer of JNTs.

Acknowledgment

The authors thank professor Duan Xuan-Ming, Dr. Chen Shu, Mrs. Li Yan, and Mr. Wang De-Song for their technical support in device fabrication.

References

[1] Colinge J P, Lee C W, Afzalian A, Akhavan N D, Yan R, Ferain I, Razavi P, O'Neill B Blake A, White M, Kelleher A M, McCarthy B and Murphy R 2010 *Nat. Nanotechnol.* **5** 225
[2] Lee C W, Nazarov A N, Ferain I, Akhavan N D, Yan R, Razavi P, Yu R, Doria R T and Colinge J P 2010 *Appl. Phys. Lett.* **96** 102106
[3] Ionescu A M 2010 *Nat. Nanotechnol.* **5** 178
[4] Colinge J P, Lee C W, Ferain I, Akhavan N D, Yan R, Razavi P, Yu R, Nazarov A N and Doria R T 2010 *Appl. Phys. Lett.* **96** 073510
[5] Colinge J P, Kranti A, Yan R, Lee C W, Ferain I, Yu R, Akhavan N D and Razavi P 2011 *Solid-State Electron.* **65–66** 33
[6] Arnold E and Alok D 2001 *IEEE Trans. Electron Dev.* **48** 1870
[7] Nakata Y, Okada T and Maeda M 2002 *Appl. Phys. Lett.* **81** 4239
[8] Zhang Y L, Chen Q D, Xia H and Sun H B 2010 *Nanotoday* **5** 435
[9] Borowiec A and Haugen H K 2003 *Appl. Phys. Lett.* **82** 4462
[10] Tanaka T, Sun H B and Kawata S 2002 *Appl. Phys. Lett.* **80** 312
[11] Kawata S, Sun H B, Tanaka T and Takada K 2001 *Nature* **412** 697
[12] Carvalho E J, Alves M A R, Braga E S and Cescato L 2006 *Microelectron. J.* **37** 1265
[13] Du Y, Cao H, Yan W, Han W, Liu Y, Dong X, Zhang Y, Jin F, Zhao Z and Yang F 2012 *Appl. Phys. A* **106** 575
[14] Ghibaudo G 1988 *Electron. Lett.* **24** 543
[15] Joo M K, Mouis M, Jeon D Y, Barraud S Park1 S J, Kim G T and Ghibaudo G 2014 *Semicond. Sci. Technol.* **29** 045024
[16] Trevisoli R D, Doria R T, de Souza M and Pavanello M A 2011 *Semicond. Sci. Technol.* **26** 105009
[17] Jeon D Y, Park S J, Mouis M, Joo M K, Barraud S, Kim G T and Ghibaudo G 2014 *Appl. Phys. Lett.* **104** 263510
[18] Salfi J, Paradiso N, Roddaro S, Heun S, Nair S V, Savelyev I G, Blumin M, Beltram F and Ruda H E 2011 *ACS Nano* **5** 2191
[19] Liu F, Wang K L, Li C and Zhou C 2006 *IEEE Trans. Nanotechnol.* **5** 441
[20] Poli S, Pala M G and Poiroux T 2009 *IEEE Trans. Electron Dev.* **56** 1191
[21] Jeon D Y, Park S, Mouis M, Berthomé M, Barraud S, Kim G T and Ghibaudo G 2013 *Solid-State Electron.* **90** 86