Investigation of trap states in Al_2O_3 InAlN/GaN metal–oxide–semiconductor high-electron-mobility transistors

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In this paper the trapping effects in $Al_2O_3/In_{0.17}Al_{0.83}N$/GaN MOS-HEMT (here, HEMT stands for high electron mobility transistor) are investigated by frequency-dependent capacitance and conductance analysis. The trap states are found at both the Al_2O_3/InAlN and InAlN/GaN interface. Trap states in InAlN/GaN heterostructure are determined to have mixed de-trapping mechanisms, emission, and tunneling. Part of the electrons captured in the trap states are likely to tunnel into the two-dimensional electron gas (2DEG) channel under serious band bending and stronger electric field peak caused by high Al content in the InAlN barrier, which explains the opposite voltage dependence of time constant and relation between the time constant and energy of the trap states.

Keywords: InAlN, trapping, frequency-dependent conductance, metal–oxide–semiconductor high-electron-mobility transistors

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1. Introduction

III-nitride metal–oxide–semiconductor HEMTs (MOS-HEMTs) (here, HEMT stands for high electron mobility transistor) are highly preferable to the Schottky-gate HEMTs due to their ability to effectively suppress gate leakage current and enhance the breakdown voltage.[1–3] However, trap states at the interface introduced by gate dielectrics cause reliability problems, such as drain saturation current decreasing and threshold voltage drifting. So it is required to study the trap states in Schottky AlGaN/GaN and AlGaN/GaN MOS-HEMTs.[4–7] Recently, attention has shifted to trap states in high Al barrier AlGaN/GaN heterostructure.[8–10] High Al content is an effective method to enhance the breakdown performance due to the wider band-gap and higher critical breakdown field, yet the immature material growth would introduce trap states into the surface, interface, or bulk material.[11] A comparison of the trap state between the two kinds of HEMTs reveals the inherent mechanism of the trapping/detrapping process. Meanwhile, lattice-matched InAlN/GaN, as another high Al barrier heterostructure, has always been a reasonable substitute for AlGaN/GaN HEMTs because its strong spontaneous polarization and strain-free in heterostructure are necessary qualities for high frequency and power electronics applications.[12–14] However, the trap analysis of InAlN/GaN HEMT with high Al content is still a comparatively less explored area.

In this work, the trapping effect of a thin barrier $In_{0.17}Al_{0.83}N$/GaN lattice matched HEMT is investigated using frequency-dependent conductance measurements. To suppress the large off-state leakage current, a Al_2O_3 gate insulator grown by atomic layer deposition (ALD) is fabricated on the semiconductor interface. Three trap states are observed at two interfaces, which shows the complicity of the high-Al and gate-oxide of the interfaces of the GaN HEMT.

2. Experimental method

The InAlN/GaN heterostructure was grown on a sapphire substrate by the PMOCVD method at Xidian University.[15] The epitaxial layer shown in Fig. 1 contains a 12-nm lattice-matched $In_{0.17}Al_{0.83}N$ barrier layer, a 1.2-nm AlN interlayer, and a 1.6-μm GaN buffer layer. Hall effect measurements at room temperature show that the sheet carrier density is 1.7×10^{13} cm^{-2}, the two-dimensional electron gas (2DEG) mobility is 1180 $cm^2/V\cdot s$, and the sheet resistance is 306 Ω/sq. The epitaxial layer was first fabricated by Cl_2 plasma mesa isolation using reactive ion etching (RIE). Ohmic contacts consisting of Ti/Al/Ni/Au were annealed in N_2 ambient

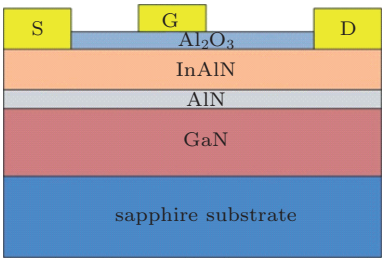


Fig. 1. (color online) Cross-section of the Al_2O_3/InAlN/AlN/GaN MOS-HEMT.

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at 830 °C for 30 s at second step. The Ohmic contact resistance was confirmed to be 0.8 Ω·mm. Then, a 12-nm Al_2O_3 film was deposited at 300 °C by the ALD method, which acts as a gate dielectric. Finally, Si_2N_3 was deposited on the whole active area as a passivation layer by the plasma enhanced chemical vapor deposition (PECVD) method.

3. Results and discussion

Figure 2 shows the variations of the representative capacitance–voltage (C_m–V) with swept voltage, which were obtained with a Keithley 4200SCS semiconductor analyzer at room temperature. Two kinds of capacitance dispersions appear as the frequency varies from 10 kHz to 1 MHz, one transition happens around −5 V, which corresponds to the strong accumulation of 2DEG in the GaN channel, and the other happens around −1 V, which corresponds to the capacitance transition of the MOS structure, indicating that the trap states exist at both the InAlN/GaN interface and the Al_2O_3/InAlN interface.

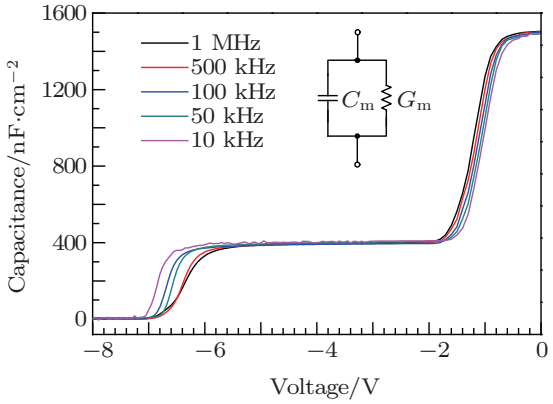


Fig. 2. (color online) C_m–V characteristics at given frequencies.

In order to analyze the dynamic capacitance dispersion, the variations of parallel trap conductance with frequency at different voltages are measured. The trap conductance G_{surf}/ω is calculated based on measured conductance G_m and capacitance C_m (the measurement circuit is shown in the inset of Fig. 2) through the following relation:

$$\frac{G_{surf}}{\omega} = \frac{\omega C_0^2 G_m}{\omega^2 (C_m - C_0)^2 + G_m^2}, \tag{1}$$

where $\omega = 2\pi f$ is the radial frequency and $C_0 = 50$ pF represents the static-state capacitance of the MOS-HEMT. The voltage range is set to be −1.4 V–0.8 V according to the capacitance dispersion region in Fig. 2.

Figure 3 shows the trap conductance dispersions with the devices biased in the accumulation region. Given that the 2DEG channel is saturated under high voltage and no electrons are captured at the InAlN/GaN interface, only the traps at the Al_2O_3/InAlN interface can be released and detected by the ac signal. The density of trap states (D_T) and the time constant (τ_T) can be evaluated by fitting the experimental G_p/ω to a function of ω according to equation in the inset of Fig. 3. The measured data (symbols) and fitted curves (lines) are obtained to be in good agreement with each other under the assumption of a continuum of trap levels.

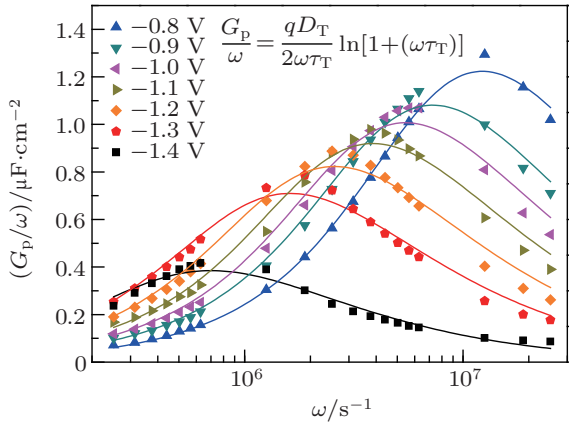


Fig. 3. (color online) Experimental (symbols) and fitting (lines) G_p/ω versus radial frequency near the accumulation region. The inset shows the equation that is used to evaluate the trap density and time constant.

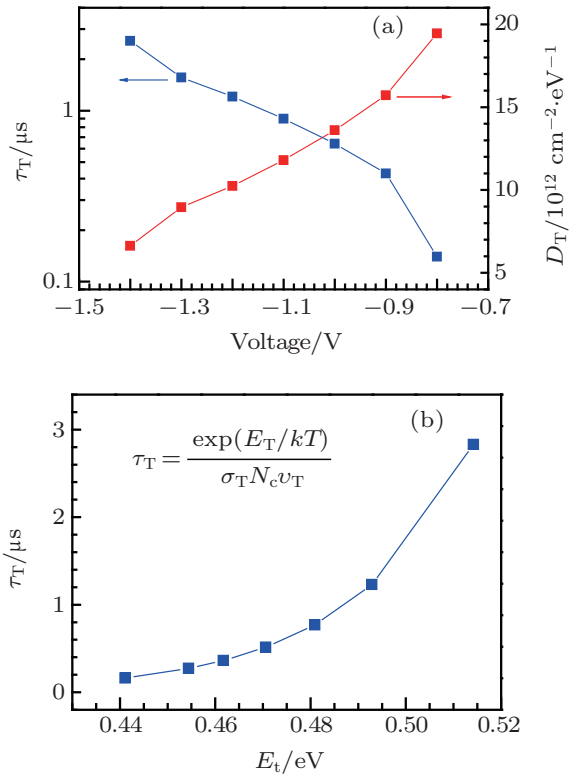


Fig. 4. (color online) (a) Time constant of trap states as a function of gate voltages. (b) Trap state density as a function of energy E_t.

Figure 4(a) shows that the time constant of trap at Al_2O_3/InAlN interface decreases exponentially from 2.83 μs to 0.16 μs with the increase of voltage. As the voltage increases, the Fermi level rises, so that more fast (shallow) traps can be detected by the measurement. The trap density at Al_2O_3/InAlN interface changes with τ_T according to a linear law from 0.60×10^{13} eV^{-1}·cm^{-2} to 1.89×10^{13} eV^{-1}·cm^{-2}.

E_t (equals E_c–E_{surf}) representing the trap level below conduction band (CB) is estimated to be within a range from 0.44 eV to 0.51 eV according to the equation in the inset of Fig. 4(b). Room temperature $T = 300$ K, capture cross section $\sigma_T = 4 \times 10^{-13}$ cm^{-2}, effective density of states in the conduction band $N_c = 2.2 \times 10^{18}$ T$^{3/2}$·cm^{-3}, and average thermal velocity of the carriers $\upsilon_T = 2.6 \times 10^7$ cm/s for GaN are used for the calculation.[4] There are no deep traps compared with the results from other AlGaN/GaN articles in which E_t is up to 0.5 eV. This is partially due to the Al_2O_3/InAlN interface (no GaN cap layer) without Ga, because the easy formation of Ga–O bonds gives rise to massive interface traps.[16]

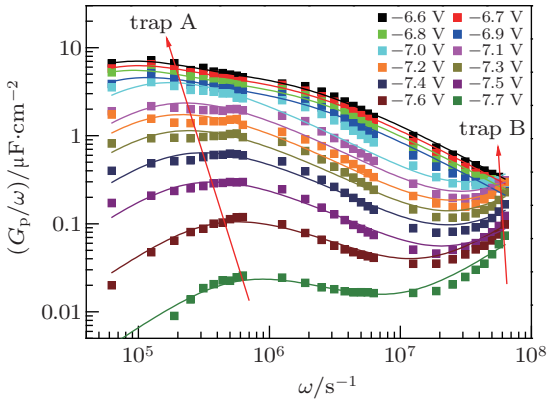


Fig. 5. (color online) Experimental (symbols) and fitting (lines) G_p/ω versus radial frequency near the threshold voltage.

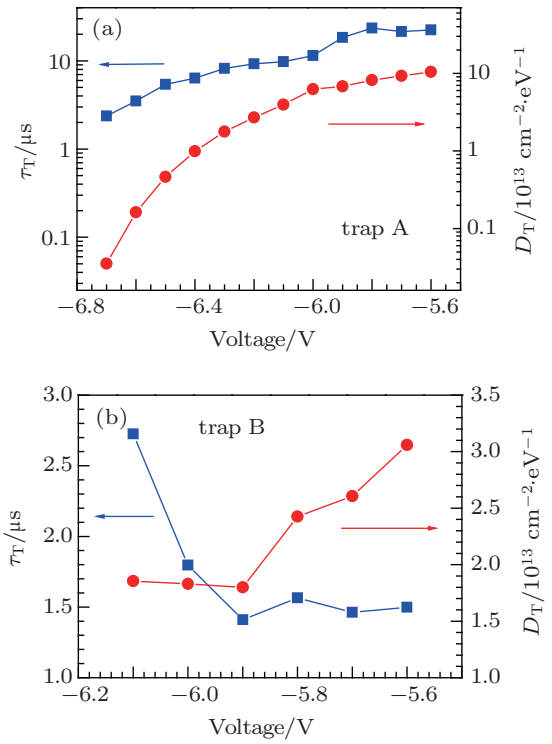


Fig. 6. (color online) Time constants of trap states as a function of gate voltage in both trap states.

Figure 5 gives the trap conductance dispersions near the threshold voltage. The trap states at InAlN/GaN interface are mainly responsible for the conductance dispersion as the heterostructure is charged by the capacitance transition. We assume that part of the density of trap states is introduced by the subsequent high temperature annealing process due to the lack of a GaN cap layer.[10] Meanwhile, in Fig. 6, the time constants of the two kinds of traps show opposite features. In other reports involving with the trap states of low Al content structures, time constant decreases with increasing voltage. However, in this work, where the Al content is up to 83% in the InAlN barrier layer, the time constant of trap B decreases from 2.8 μs to 1.4 μs as the voltage increases, while the time constant of trap A increases from 2.37 μs to 22.4 μs. We believe that there are mixed de-trapping mechanisms in trap A and that the electron tunneling is the main reason for the dependence of the time constant on the abnormal voltage.

The electron tunneling effect can be explained by using the one-dimensional simulation of the band diagram and polarization electric field shown in Fig. 7, which is derived from the self-consistent solutions of Schrödinger and Poisson's equations. Another structure with 12-nm $Al_{0.30}Ga_{0.70}N$ barrier is also simulated for comparison. Commonly, the electron emission from trap states to the conduction band level is considered to be the cause of the dynamic capacitance dispersion. As voltage increases, E_F at interface approaches to CB and the shallower trap states exhibit decreased emission time τ_E (equal to trap time constant).[9]

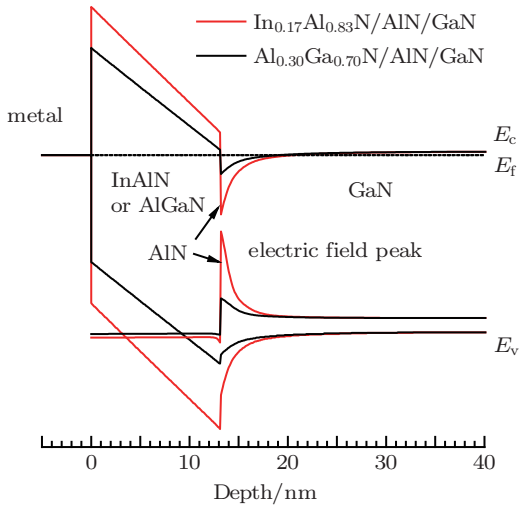


Fig. 7. (color online) Simulated band diagram and polarization electric field of $In_{0.17}Al_{0.83}N$/AlN/GaN and $Al_{0.30}Ga_{0.70}N$/AlN/GaN structures.

However, in a high Al content barrier, more serious band bending and stronger electric field peak exist at the interface and barrier, so electrons captured in trap states could possibly tunnel into the 2DEG channel, making the de-trapping process different. The time constant is mainly determined by the tunneling of electrons other than the emission to CB.[9] Thus, the rising of voltage reduces the electric field in the barrier layer, resulting in a longer tunneling time, which leads to an

increased time constant of trap A. Moreover, the τ_T–E_t relations of the two traps show a strong correlation in Fig. 8. The E_t of trap B, varying from 0.441 eV to 0.458 eV, is just below the E_t of trap A. Since trap B is closer to the conduction band than trap A, the de-trapping process of trap B is possibly caused by voltage changing, and the electrons in the deeper trap A may be de-trapped by the tunneling effect, which proves to be a different de-trapping mechanism of two kinds of traps.

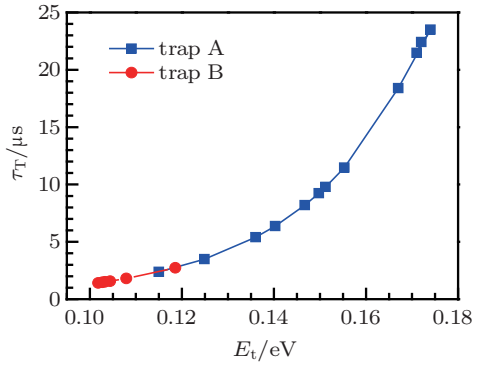


Fig. 8. (color online) Time constants as a function of energy in both trap states.

4. Conclusions

In this paper, we report on a detailed analysis of trap states in ALD Al_2O_3/$In_{0.17}Al_{0.83}N$/GaN MOS-HEMT. Trap densities, trap energies, and time constants are determined by frequency-dependent capacitance and conductance measurements. The trap states are found at both Al_2O_3/InAlN and InAlN/GaN interfaces, and the trap states in InAlN/GaN heterostructure are determined to have two different de-trapping mechanisms. The electrons captured in the trap states are likely to tunnel into the 2DEG channel under serious band bending and stronger electric field peak caused by high Al content in the $In_{0.17}Al_{0.83}N$ barrier, which explains the opposite voltage dependence of the time constant. Furthermore, strong correlations in τ_T–E_t of both traps can also be explained as the transition from normal electron emission to electron tunneling of the de-trapping process. More experimental data that can reveal the inherent mechanism of the traps states process are necessary for further research.

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