Influence of ultra-thin TiN thickness (1.4 nm and 2.4 nm) on positive bias temperature instability (PBTI) of high-*k*/metal gate nMOSFETs with gate-last process*

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The positive bias temperature instability (PBTI) degradations of high-*k*/metal gate (HK/MG) nMOSFETs with thin TiN capping layers (1.4 nm and 2.4 nm) are systemically investigated. In this paper, the trap energy distribution in gate stack during PBTI stress is extracted by using ramped recovery stress, and the temperature dependences of PBTI (90 °C, 125 °C, 160 °C) are studied and activation energy (E_a) values (0.13 eV and 0.15 eV) are extracted. Although the equivalent oxide thickness (EOT) values of two TiN thickness values are almost similar (0.85 nm and 0.87 nm), the 2.4-nm TiN one (thicker TiN capping layer) shows better PBTI reliability (13.41% at 0.9 V, 90 °C, 1000 s). This is due to the better interfacial layer/high-*k* (IL/HK) interface, and HK bulk states exhibited through extracting activation energy and trap energy distribution in the high-*k* layer.

Keywords: positive bias temperature instability (PBTI), HK/MG, E_a, trap energy distribution

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1. Introduction

As device dimensions shrink, high-*k* materials are being implemented by Si-CMOS technologies to alleviate the rapid gate current increase associated with aggressive oxide thickness scaling.[1] Owing to the continuous scaling of metal–oxide–semiconductor field-effect transistor (MOSFET), high-*k* gate dielectric materials are expected to replace traditional SiO_2 in future complementary metal–oxide–semiconductor (CMOS) generation for low power circuits.[2] However, due to an extra interfacial layer and complicated band structure,[3] the reliability issues of CMOS devices with high-*k*/metal gate structure are becoming increasingly complicated and important, especially bias temperature instability (BTI).[4]

The TiN layer acts as a capping layer for high-*k* gate dielectric in the CMOS integration process. In particular, the positive bias temperature instability (PBTI) reliability of a device with TiN layer, as one of the major reliability issues, shows the dependence of the thickness of the TiN layer.[5] In this paper, the electrical characteristics and BTI degradations of high-*k*/metal gate MOSFETs with thin TiN capping layers (1.4 nm and 2.4 nm) are systemically studied. The PBTI differences and physical mechanisms are analyzed by extracting activation energy[6] and energy distribution of the trap in the high-*k* layer.

2. Experiment

In this work, nMOSFETs were used as the test devices, which are shown in Fig. 1 with Hf-based dielectric stacks and different ultra-thin ALD TiN thickness values (1.4 nm and 2.4 nm). The equivalent oxide thickness (EOT) values of 1.4-nm TiN and 2.4-nm TiN were 0.85 nm and 0.87 nm, respectively. The gate width and length of transistor were 0.5 μm and 0.5 μm respectively. The test mode was the measurement-stress-measurement mode. The test was executed separately at constant temperatures of 60 °C, 90 °C, 125 °C, and 160 °C in a range of stress gate voltages (V_G). The source and substrate

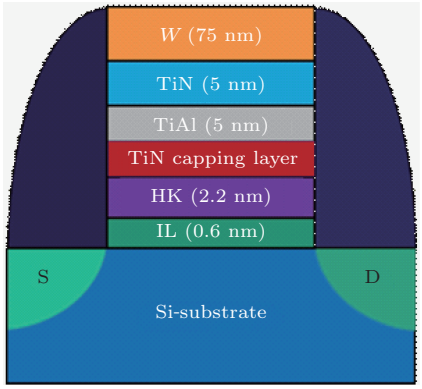


Fig. 1. (color online) Structure of the nMOSFET tested in this work, the red layer is TiN capping layer.

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were grounded.

The nMOSFET was stressed at $V_{gstr} = 0.9$ V for 1000 s. After stress, V_g was changed to $V_{discharge,1}$ to start the discharge and the V_{th} shift against the "discharge time" was monitored, as indicated in Fig. 2. $V_{discharge}$ ranges from 0.7 V to −0.9 V in steps of 0.2 V and each $V_{discharge}$ lasted 1000 s.

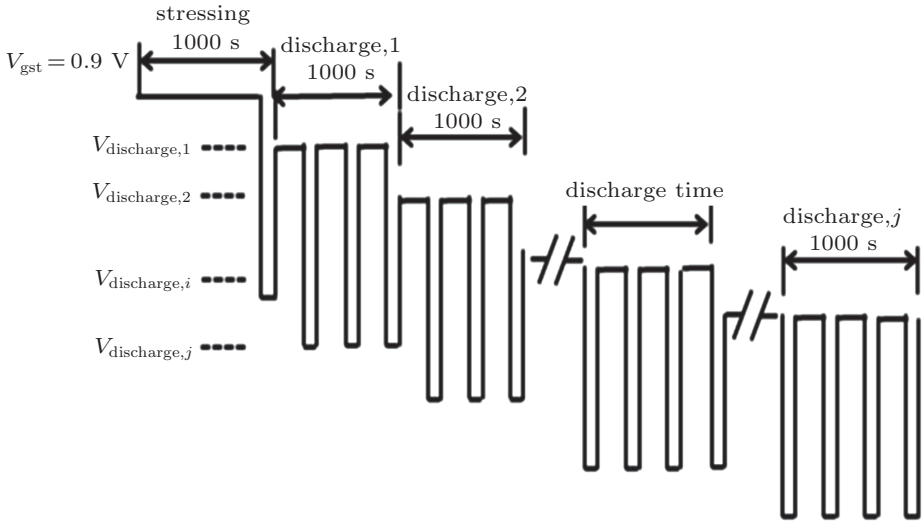


Fig. 2. Vg waveform. After stress, discharging occurs at $V_{discharge,1}$ for 1000 s. The gate bias is then changed to $V_{discharge,2}$ for the next discharging phase and the same procedure is applied.

3. Result and discussion

The BTI of the MOSFET device induces the shifts of the device's parameters, such as V_{th}, GM, leakage current (I_g), etc.[7] A physical understanding of PBTI degradation mechanisms can be obtained through the variations of these electrical parameters, especially the V_{th} shift.

In Fig. 3, PBTI degradations versus time are shown for different ultra-thin TiN thickness values (1.4 nm and 2.4 nm) of high-k/metal gate nMOSFETs with gate-last process. The degradations of V_{th} with varying stress V_g directly show that the 2.4-nm TiN layer is better than the 1.4-nm layer. In other words, the 1.4-nm TiN layer has the worst PBTI: the V_t shift difference is 13.41% at 0.9 V, 90 °C, 1000 s.

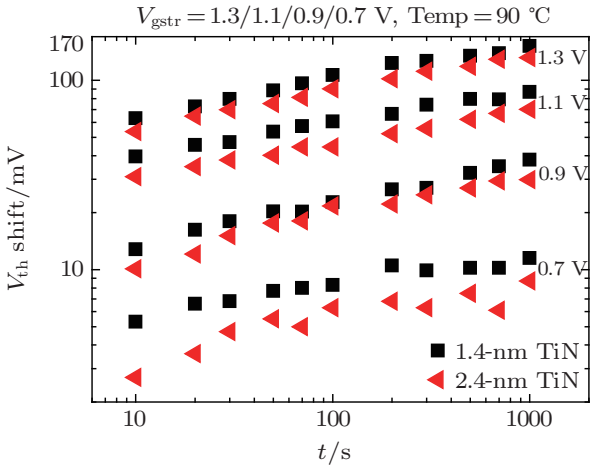


Fig. 3. (color online) Variations of V_{th} shift with time t for stress $V_g = 1.3$ V, 1.1 V, 0.9 V, 0.7 V.

The temperature dependences of PBTI are shown in Fig. 4(a). The temperatures are 60 °C, 90 °C, 125 °C, 160 °C, and the voltage stress is 0.9 V. In Fig. 4(b), the extracted thermal activation energy (E_a) values are 0.133 eV and 0.155 eV, for samples with 2.4-nm TiN and 1.4-nm TiN layers, respectively. The activation energy of the 2.4-nm TiN layer is similar to that of the 1.4 nm layer. As is well known, the activation energy of high-k stack is around 0.03 eV–0.04 eV, while that of conventional SiO_2 gate is about 0.2 eV–0.3 eV.[8,9] It is demonstrated that the degradation mechanism[10] introduced by high-k material is dominant for both the 2.4-nm and 1.4-nm TiN layers.

Usually, the PBTI degradation occurs in high-k bulk.[11] In order to obtain the quantity and distribution of N_{OX} in HK bulk, a new method is proposed, as described in Fig. 2, based on PBTI recovery characteristics.[12,13] Figure 5(a) shows that the larger trap density of the device with thinner capping TiN under both 90 °C and 160 °C. Figure 5(b) shows the energy profile extraction for traps by using ramp recovery stress, which is described in detail below,[14] similar to that in our previous work.[15]

(i) V_{th} shift after completing discharge under each $V_{discharge}$ is converted into the effective charge density, i.e., N_{OX} and plotted against $V_{discharge}$, where $N_{OX} = \Delta V_{th}\varepsilon_0\varepsilon_r/dq$, with $\Delta V_{th} = V_{th}$ (end of each discharge)-V_{th0} ($T_{stress} = 0$);

(ii) The next task is to convert $V_{discharge}$ into the energy level of E_C, i.e., $(E_T - E_C)$, by the oxide band structure, the same as that of our previous work,[15] where $E_T - E_C = q \cdot V_{OX}$ and $V_g = V_{OX} + V_S + V_{ms}$, with E_T being the trap energy level and E_C the conduction band of substrate silicon, and V_S the surface potential drop;

(iii) Plot N_{OX} against $(E_T - E_C)$ converted from the $V_{discharge}$, as described in Fig. 4(a); and,

(iv) Obtain the differentiation of N_{OX} against $(E_T - E_C)$ as described in Fig. 5(a) and D_{OX} against $(E_T - E_C)$ as described in Figs. 5(b) and 5(c).

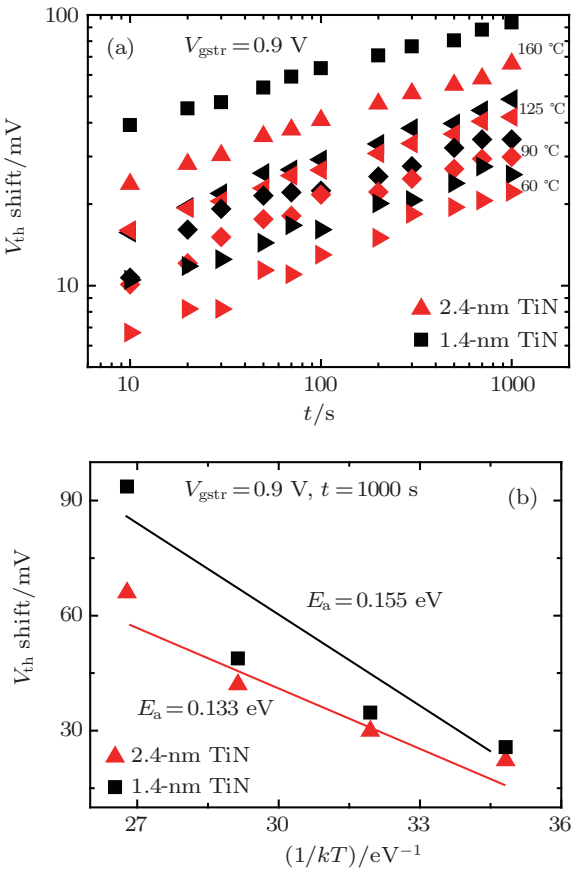


Fig. 4. (color online) (a) Variations of V_{th} shift with time t for (b) variations of V_{th} shift with reciprocal of kT $(1/kT)$ for 2.4-nm and 1.4-nm TiN layers, where the activation energy (E_a) values are extracted from the results in panel (a).

The results in Fig. 5 show that N_{OX}(1.4 nm) > N_{OX}(2.4 nm) and D_{OX}(1.4 nm) > D_{OX}(2.4 nm) for the cases of 90 °C and 160 °C. In particular, the maximum value appears at an energy 0.05 eV above the conduction band of silicon, which is shown in Fig. 6. This confirms that there are many more traps in the 1.4-nm TiN layer than in the 2.4-nm TiN layer. Figure 6 also shows the energy distribution of traps, indicating that there is a deeper trap in the HK bulk.

By combining the results, i.e., $E_a = 0.13$ eV for 2.4-nm TiN layer is closed to $E_a = 0.15$ eV for 1.4-nm TiN layer, in Fig. 4, as we just investigated, it is illustrated that trap generation happens in the HK dielectric layer, i.e., IL/HK interface and HK bulk.[16]

The influence of capping TiN thickness on PBTI could be explained by Nitrogen's out-diffusion from ALD TiN filling the oxygen vacancies in HK bulk, as described in Fig. 7.[17] In other words, the density of oxygen vacancies[18] is suppressed by thicker TiN capping layer due to the increased Nitrogen diffusion in the thicker (2.4 nm) film, which increases the stability of HK bulk and IL/HK interface.[19] So the thicker TiN capping layer shows better PBTI characteristics due to the better quality of the HK dielectric, as shown in Figs. 3 and 5.

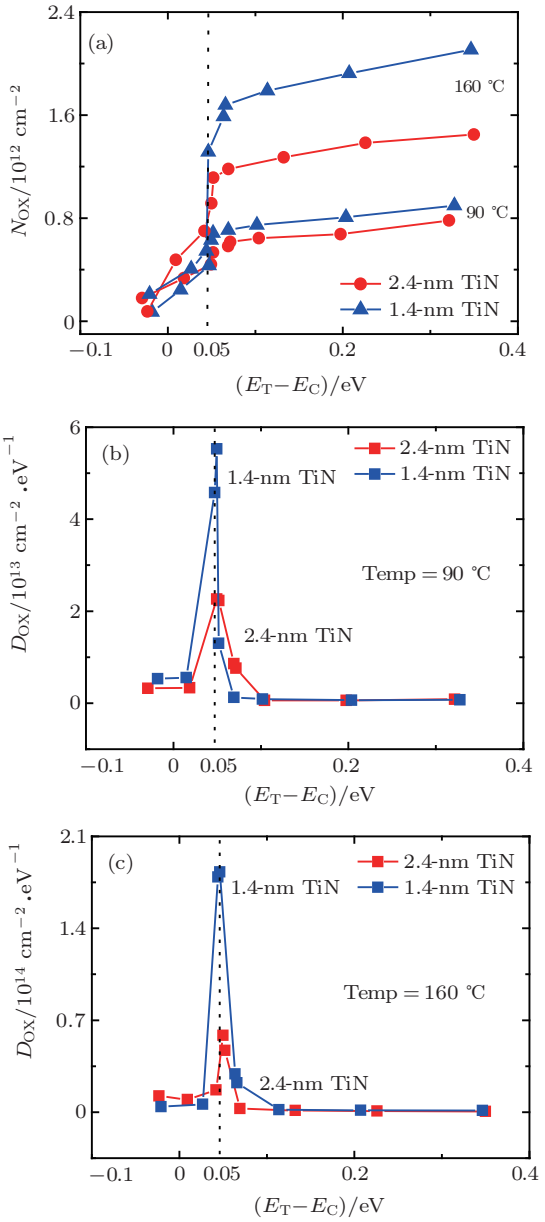


Fig. 5. (color online) (a) Profiles of effective charge density (N_{OX}) induced by PBTI recovery characteristics, (b) and (c) trap energy distributions at 90 °C and 160 °C, respectively.

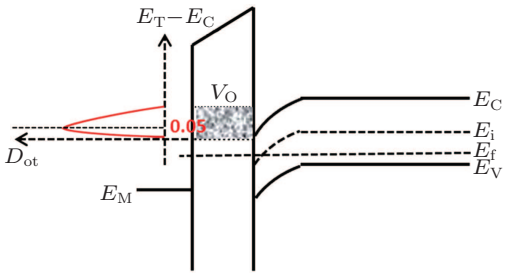


Fig. 6. (color online) Band diagram of silicon/high-k/metal gate stacks. The shadow area represents the trap energy range that is strongly influenced by stress and the dot distribution is given.

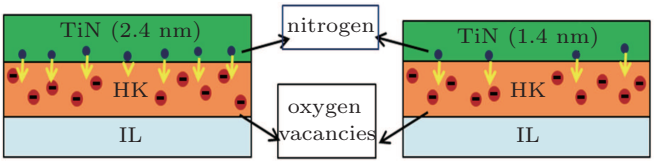


Fig. 7. (color online) Illustration of nitrogen diffusion from TiN film toward HK bulk. A thicker TiN capping layer can accelerate nitrogen diffusion.

4. Summary

The PBTI degradation of different thin TiN thickness with high-*k*/metal gate structure nMOSFETs is studied. Through a series of experiments, it is found that a thicker TiN capping layer shows better PBTI reliability due to the improvement of the IL/HK interface and HK bulk states by reducing the density of oxygen vacancies in HK gate dielectric through Nitrogen's out-diffusion from the TiN layer filling the oxygen vacancies in the HK bulk.

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