Interfacial and electrical characteristics of a HfO_2/n–InAlAs MOS-capacitor with different dielectric thicknesses*

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A HfO_2/n–InAlAs MOS-capacitor has the advantage of reducing the serious gate leakage current when it is adopted in InAs/AlSb HEMT instead of the conventional Schottky-gate. In this paper, three kinds of HfO_2/n–InAlAs MOS-capacitor samples with different HfO_2 thickness values of 6, 8, and 10 nm are fabricated and used to investigate the interfacial and electrical characteristics. As the thickness is increased, the equivalent dielectric constant ε_{ox} of HfO_2 layer is enhanced and the InAlAs-HfO_2 interface trap density D_{it} is reduced, leading to an effective reduction of the leakage current. It is found that the HfO_2 thickness of 10 nm is a suitable value to satisfy the demands of most applications of a HfO_2/n–InAlAs MOS-capacitor, with a sufficiently low leakage current compromised with the threshold voltage.

Keywords: HfO_2/n–InAlAs MOS-capacitor, high-k gate dielectric, interface trap density, leakage current

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1. Introduction

Due to their high electronic mobility and peak velocity, InAs/AlSb high electron mobility transistors (HEMTs) have received attention as promising devices for high-frequency, low-dissipation, and low-noise applications.[1,2] However, the very narrow band gap of InAs channel and the type-II staggered energy-band diagram alignment mean that the gate-leakage current is a critical problem for InAs/AlSb HEMTs, leading to lower noise performance and reliability.[3] Therefore, the development of a method to reduce the leakage current is a hot topic for InAs/AlSb HEMTs. For example, a lattice matched InAlAs buffer layer has been deposited on an AlSb barrier layer as the contact with the gate electrode to form a Schottky gate, which could restrict the leakage current of the device to μA magnitude;[3,4] however, this is far from adequate. According to Refs. [5] and [6], a high-k dielectric deposited between the semiconductor epitaxial and the metal electrode to form a metal–oxide–semiconductor capacitor (MOS-capacitor), behaving as a gate insulator, instead of the conventional Schottky gate, could effectively reduce the leakage current of device. Al_2O_3 is the most frequently used high-k dielectric and its use has been reported in other published papers;[6,11] however, the dielectric constant of Al_2O_3 is still too low to provide a high equivalent oxide thickness (w_{eot}), leading to a weak gate control ability and high threshold voltage, which makes the power dissipation of the device a considerable problem. In this case, HfO_2 has been considered as a competitive candidate for the high-k dielectric because of its high-k value and high energy band gap.[7,8] However there have been very few reports about the use of HfO_2 deposited on InAlAs as a MOS-capacitor. Therefore, it is necessary to investigate the physical and electrical performance of a HfO_2/InAlAs MOS-capacitor, and to determine the suitable HfO_2 thickness for the further application of a HfO_2/InAlAs MOS-capacitor in InAs/AlSb HEMTs.

In this paper, three kinds of HfO_2/n–InAlAs MOS-capacitor samples are fabricated, the thickness values of the oxide layer (t_{ox}) are 6, 8, and 10 nm. The chemical composition of HfO_2 layer is analyzed by x-ray photoelectron spectroscopy (XPS), and the HfO_2–InAlAs interface trap density is calculated according to the capacitance–voltage (C–V) test result. Furthermore, the leakage current performance of the samples with different values of t_{ox} are characterized in detail.

2. Experiments

The HfO_2/n–InAlAs MOS-capacitor was fabricated with the structure that is shown in Fig. 1. The 1.5-μm n-InAlAs layer, which was Si-doped with a concentration of $1\times10^{11}\text{cm}^{-3}$, was deposited epitaxially on a GaAs semi-insulating substrate. The good lattice match between the two reduced the substrate influence on the capacitor. A 5-nm InAs layer was deposited on the top of the InAlAs epitaxial layer for protection, and it was subsequently removed completely by an etching process with mixed citric acid and H_2O_2 in 1:1 ratio for 60 s in order to adequately expose the InAlAs in preparation for HfO_2 growth. The InAlAs surface was then treated with a chemical liquid containing 36%–38% HCl to remove the native oxides. It was next treated by 7%

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$(NH4)_2S$ to remove elemental As and produce a good-quality InAlAs surface.[7,8] HfO_2 film was subsequently grown on the clean InAlAs epitaxially by atomic layer deposition (ALD) at 245 °C with a pressure of 2300 Pa. A post deposition annealing (PDA) process was then used in order to form a diffusion barrier layer to prevent the interaction between HfO_2 and InAlAs.[9] Considering the crystallizing points of HfO_2 and InAlAs materials, the PDA temperature was chosen to be 380 °C. Finally, Ti/Pt/Au was deposited as the metal electrode with a thickness of 20/20/200 nm, in which Pt is adopted to prevent Au from entering the semiconductor through the formation of defects and contamination. The window of the metal electrode was formed by electron-beam lithography on the top of HfO_2. The layout is shown in Fig. 2. The biggest electrode is 100 times larger than the smallest one of 150×150 μm in order to make the *C*–*V* test accurate by using the size of electrode method.

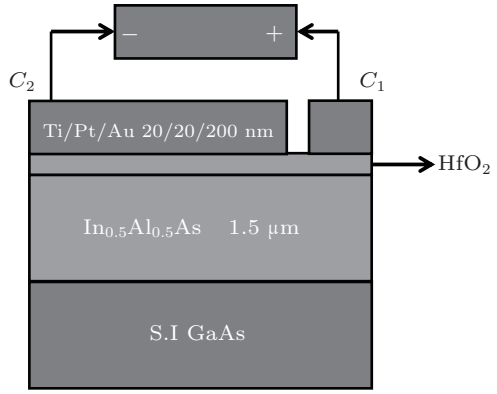


Fig. 1. Schematic diagram of a HfO_2/n–InAlAs MOS-capacitor.

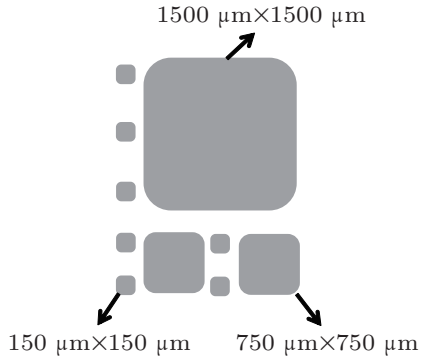


Fig. 2. Layout of a Ti/Pt/Au metal electrode for the unit capacitor.

3. Measurement and characterization

Three kinds of HfO_2/n–InAlAs MOS-capacitor samples with different oxide thickness (t_{ox}) values of 6, 8, and 10 nm were prepared by different growth circles using ALD. Figure 3 shows the XPS measurements on the HfO_2 surface after PDA processing. Given that 3d is present in Fig. 3(a), it can be seen that the bulk peak of the 6-nm sample moving towards the lower binding energy side is mainly attributed to As–InAl compounds with high concentration compared with those of 8-nm and 10-nm samples, suggesting that 6 nm is thin enough to allow the InAlAs–HfO_2 interfacial component to be detected. As t_{ox} is increased, the As_{3d} peak moves towards to the higher binding energy direction, primarily due to the formation of As–H compounds induced by the surface treatment. It is worth noticing that the concentration of As element does not vary obviously as t_{ox} is increased. This implies that the As in HfO_2 dielectric has a strong diffusion ability and that As could capture oxygen atoms from HfO_2 to form As–O states in the oxide layer, leading to redundant vacancy oxygen to form charge traps. As shown in Fig. 3(b), In $3d_{5/2}$ is found in greatly different concentrations for the samples with different t_{ox} values. The peak is obviously detected for the 6-nm sample, which can be explained by the In–AlAs states at 444.38 eV, In_2O states at 444.83 eV, and In_2O_3 at 445.2 eV.[10] In this case, the In–O states generate the vacancy oxygen and degrade the quality of the HfO_2 surface. However, the peak value is difficult to observe for 8 nm and 10 nm samples, indicating a weak diffusivity of In element in HfO_2 dielectric. Therefore, In compounds are not able to degrade the quality of oxide layers for samples with high t_{ox} values. Figure 3(c) presents the XPS result for Hf 4f. It is observed that the peak for the 6-nm sample possesses a high binding energy compared with those for the 8-nm and 10-nm samples because the 6-nm oxide layer is thin enough to detect HfAlO generated in the transition layer between HfO_2 and InAlAs, whereas HfAlO cannot be detected on HfO_2 surface when t_{ox} is increased to 10 nm, so an enhanced concentration of HfO_2 makes the Hf 4f peak shift towards a lower binding energy. The O 1s core level spectra in Fig. 3(d) also presents the same trend as Hf 4f spectra to show the appearance of HfAlO for the 6-nm sample. As t_{ox} is increased, the enhanced concentration of HfO_2 makes the bulk peak drift towards the lower binding energy side. Meanwhile, other non-ideal oxide (As–O, In–O, and Al–O states) are obviously reduced, causing a pure oxide layer surface that improves the quality of the MOS-capacitor.

An etching process is applied to HfO_2 dielectric to further analyze the HfO_2–InAlAs interface. In order to present the most typical distinctions for different HfO_2 thickness values, only 6-nm and 10-nm samples are discussed here. The XPS measurements are shown in Fig. 4. It is found that HfAlO with a higher dielectric constant than HfO_2 is detected on the interface of each of the 6-nm and 10-nm samples, which performs as a buffer layer to suppress the interaction between HfO_2 and InAlAs. Meanwhile a great many of As–O states, and amounts of light for In–O and Al–O states are detected on the interface, which could degrade the interfacial performance. In particular, a higher concentration of HfO_2 is detected for the 10-nm sample than that for the 6-nm sample, which is primarily attributed to the reduction of As–O states, which improves the quality of the interface and electrical performance of the MOS-capacitor.

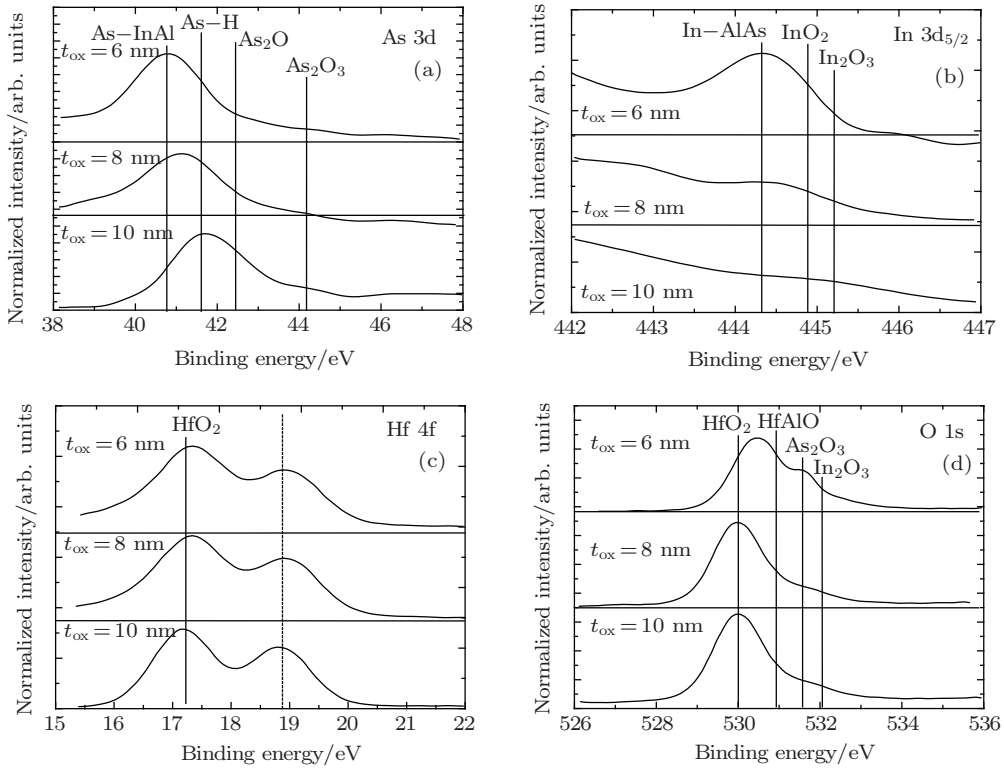


Fig. 3. Measured results by XPS after PDA process (a) As 3d, (b) In $3d_{5/2}$, (c) Hf 4f, (d) O 1s.

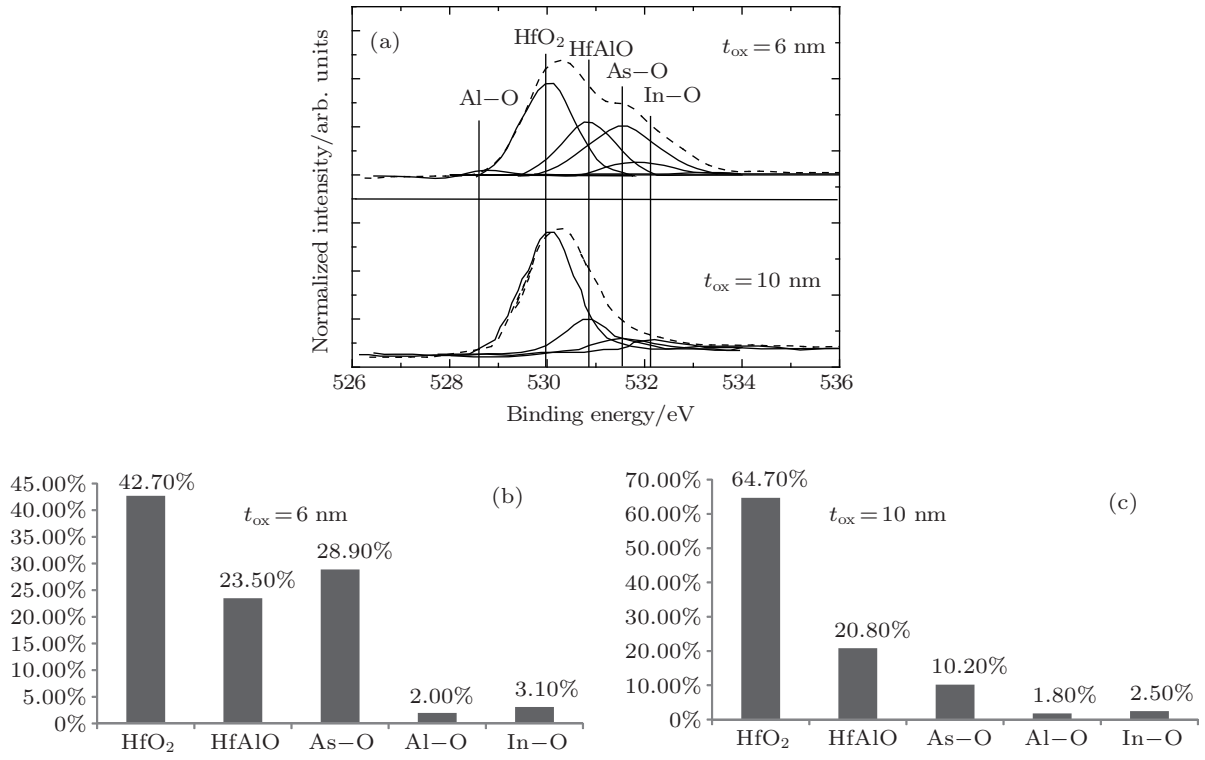


Fig. 4. Interfacial oxide performances with different t_{ox} values of 6 nm and 10 nm (a) interfacial XPS spectra measurements for O_{1s} and (b) various oxide ratios.

The *C*–*V* test of the MOS-capacitor with different t_{ox} values at 1 MHz by using high frequency equivalent capacitance method is shown in Fig. 5. The values of the accumulated capacitor C_M^a are sequenced as $C_M^a(6\text{ nm}) > C_M^a(8\text{ nm}) > C_M^a(10\text{ nm})$; thus, the oxide capacitance C_{ox} approximating to C_M^a is inversely proportional to t_{ox}. Therefore, as t_{ox} is increased, the equivalent oxide thickness w_{eot} is elevated according to Eq. (1) and the equivalent dielectric constant ε_{ox} is cal-

culated to be enhanced according to Eq. (2). This suggests that the quality of the dielectric layer is enhanced. The values are given in Table 1. The biggest ε_{ox} is calculated to be 6.19-nm for the 10-nm sample, but is still quite low compared with the pure dielectric constant of HfO_2. This is caused by other oxides with lower dielectric constants being formed in the HfO_2 layer, such as As–O and In–O. In addition, the calculated ε_{ox} is much lower than the reported value of HfO_2 deposited on silicon substrate, which may be explained by the formation of a low-k interfacial-layer between HfO_2 and InAlAs. On the other hand, the threshold voltage V_{th} of the MOS-capacitor could be also extracted from the C–V measurement according to the flat band capacitance (C_{FB}) and flat band voltage (V_{FB}) from Eqs. (3) and (4).[11] The results of V_{th} are shown in Table 1. It is found that the 6-nm sample presents the biggest V_{th} (2.78 V), which is primarily attributed to the great V_{FB} induced by the massive oxide charges. In addition, V_{th} is improved to 1.64 V while t_{ox} is increased to 8 nm due to the lower V_{FB} induced by the improved oxide layer. However, when t_{ox} is gradually increased from 7 nm to 10 nm, V_{th} is degraded from 1.64 V to 1.71 V. This happens because the influence of V_{FB} on V_{th} is lower when t_{ox} is increased and because the influence of oxide thickness becomes dominant according to Eq. (4). Actually, the V_{th} of 1.7 V for the 10-nm MOS-capacitor is still much higher when compared with the V_{th} (lower than 0.5 V) for Schottky-gate InAs/AlSb HEMTS.[3,4] However, this sacrifice induced by a thicker oxide layer could effectively enhance the leakage current, which will be discussed hereinafter. Furthermore, it is easily understood that if t_{ox} is increased continually up to more than 10 nm, then a much higher V_{th} could be introduced, which would severely degrade the power dissipation of the MOS-capacitor. Therefore, an over-valued oxide thickness should be avoided.

$$w_{eot} = \frac{\varepsilon_{SiO_2}\varepsilon_0 A}{C_{ox}}, \tag{1}$$

$$\varepsilon_{ox} = \frac{\varepsilon_{SiO_2}}{w_{eot}} t_{ox}, \tag{2}$$

$$C_{FB} = \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox} + (\varepsilon_{ox}/\varepsilon_{InAlAs})\sqrt{(kT/q)(\varepsilon_{InAlAs}\varepsilon_0/qN_d)}}, \tag{3}$$

$$V_{th} = V_{FB} - 2\frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right) - \frac{\sqrt{4q\varepsilon_{InAlAs}\varepsilon_0 N_d/\left[(kT/q)\ln\left(N_d/n_i\right)\right]}}{\varepsilon_{ox}\varepsilon_0/t_{ox}}, \tag{4}$$

where A is the area of capacitor, ε_{SiO_2} is the equivalent dielectric of SiO_2 (3.9), ε_0 is the permittivity of free space, k is the Boltzmann constant, T is the thermodynamic temperature, q is the electron charge, ε_{InAlAs} is the equivalent dielectric of InAlAs (12.42), N_d is the doping concentration of n-InAlAs, and n_i is the intrinsic carrier concentration of InAlAs at room temperature (i.e., 1.35×10^6 cm^{-3}).

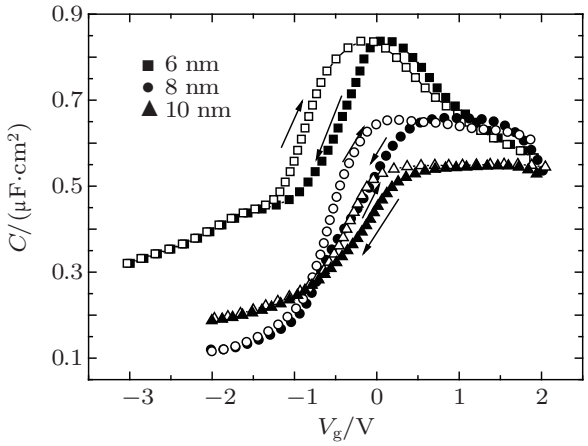


Fig. 5. C–V characteristics and the hysteresis performances of HfO_2/n–InAlAs MOS-capacitor with different t_{ox} values.

An obvious downward bending in the C–V measurement for the 6-nm sample with a bias more than 0 V is observed to infer a very serious leakage current, which is induced by the poor quality of HfO_2 film and the HfO_2–InAlAs interface. In contrast, the bending could basically not be detected when t_{ox} is increased to 10 nm, implying an improved leakage current performance.

Table 1. Electrical parameters extracted from the C–V measurements for HfO_2/n–InAlAs MOS-capacitor with different t_{ox} values.

t_{ox}/nm	C_{ox}/(μF/cm^2)	w_{eot}/nm	ε_{ox}	C_{FB}/(μF/cm^2)	V_{FB}/V	V_{th}/V
6	0.837	4.13	5.67	0.42	–1.75	–2.78
8	0.658	5.25	5.95	0.37	–0.5	–1.64
10	0.548	6.30	6.19	0.33	–0.47	–1.71

The interface traps as the centers of generation and the recombination for minority carriers effectively influence the sub-threshold swing, the threshold voltage, and the leakage current performance of the MOS-capacitor, which is greatly dependent on the match between dielectric and semiconductor.[10] Additionally, the interface trap density D_{it} values calculated by the Terman method from the C–V test result,[8,12] as shown in Fig. 6, suggest that the interfacial performance is also influenced by the thickness of the oxide layer. It is shown that the 6-nm sample has the biggest D_{it} of 10^{13}/eV·cm^2–10^{14}/eV·cm^2, which is primarily induced by the massive As–O states at the interface, but when t_{ox} is increased

to 10 nm, D_{it} is improved by lower than 10^{13}/eV·cm^2 for most calculated ranges due to the enhanced ratio of HfO_2 (as analysed above). However, the D_{it} of the 10-nm sample is still higher than that of the conventional HfO_2/Si MOS-capacitor, which could be primarily explained by the poorer match between HfO_2 and InAlAs. On the other hand, the PDA process could influence the interfacial characteristics, but in this paper 380 °C is not the optimal PDA temperature[15] to most effectively suppress the interaction between HfO_2 and InAlAs. Therefore, our next investigation will examine the improvement of the PDA process to further enhance the interfacial performance of the MOS-capacitor.

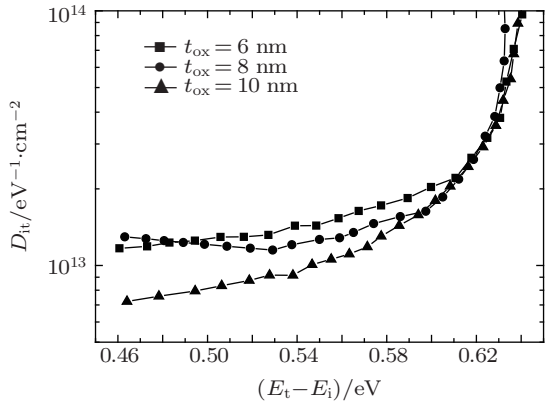


Fig. 6. Interface trap density D_{it} of HfO_2/n–InAlAs MOS-capacitor with different t_{ox}. $(E_t - E_i)$ presents the distance from the energy level of the interface trap state (E_t) to the intrinsic Fermi level (E_i).

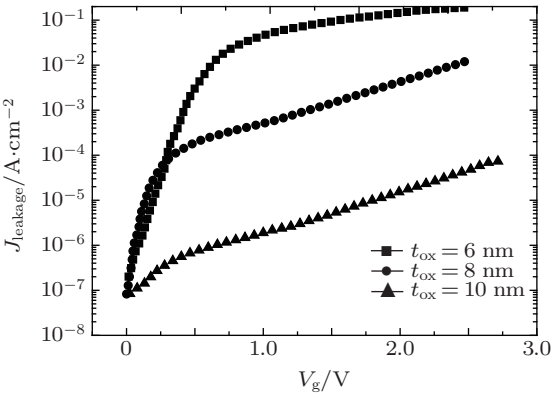


Fig. 7. $J_{leakage}$–V_g test result of HfO_2/n–InAlAs MOS-capacitor with different t_{ox} values.

As shown in the above conclusions, the qualities of HfO_2 surface and HfO_2–InAlAs interface are improved as t_{ox} increases. Therefore, the leakage current of the HfO_2/InAlAs MOS-capacitor should be effectively reduced by increasing the HfO_2 thickness, which is verified by the *I*–*V* test result in Fig. 7. The leakage current density $J_{leakage}$ for the 6-nm sample is biggest; $J_{leakage}$ is reduced by two orders of magnitude as t_{ox} is increased to 8 nm; and, when t_{ox} approaches 10 nm, $J_{leakage}$ achieves a very low values of 10^{-7} A/cm^2–10^{-5} A/cm^2 under bias condition of 0 V–2 V (i.e., the leakage current is 10^{-10} A–10^{-8} A). This indicates an obvious improvement compared with the metal-semiconductor Schottky structure, which is enough for most applications of the MOS-capacitor. But if t_{ox} is continually increased to more than 10 nm, then the threshold voltage V_{th} may be degraded to an unacceptably high value (as discussed above) and the power dissipation could deteriorate significantly. Therefore, increasing the thickness of HfO_2 layer up to 10 nm is adequate for most applications of a HfO_2/InAlAs MOS-capacitor.

4. Conclusions

In this paper, HfO_2/InAlAs MOS-capacitor samples with different oxide thickness t_{ox} values of 6, 8, and 10 nm are investigated. The XPS test result demonstrates that the quality of HfO_2 surface is enhanced when t_{ox} is increased, while the interface trap density D_{it} is reduced. As a result, the leakage current of the MOS-capacitor is effectively improved by increasing t_{ox}. We achieve a significant low leakage current density of 10^{-7} A/ cm^2–10^{-5} A/ cm^2 with gate voltage increasing from 0 V to 2 V when the HfO_2 thickness is chosen to be 10 nm, which is suitable for further application to InAs/AlSb HEMTs.

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