Exponential flux-controlled memristor model and its floating emulator*

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As commercial memristors are still unavailable in the market, mathematic models and emulators which can imitate the features of the memristor are meaningful for further research. In this paper, based on the analyses of characteristics of the q–φ curve, an exponential flux-controlled model, which has the quality that its memductance (memristance) will keep monotonically increasing or decreasing unless the voltage's polarity reverses (if not approach the boundaries), is constructed. A new approach to designing the floating emulator of the memristor is also proposed. This floating structure can flexibly meet various demands for the current through the memristor (especially the demand for a larger current). The simulations and experiments are presented to confirm the effectiveness of this model and its floating emulator.

Keywords: memristor, exponential model, floating emulator

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1. Introduction

In 1971, based on the symmetry and the completeness of the circuit theory, Chua proposed that there should be a basic two-terminal circuit element characterized by a nonlinear relationship between the charge q ($q(t) \triangleq \int_{-\infty}^{t} i(\tau)\mathrm{d}\tau$) and the flux φ ($\varphi(t) \triangleq \int_{-\infty}^{t} v(\tau)\mathrm{d}\tau$); this is the memristor.[1,2] If the nonlinear relationship is depicted as a single-valued function of the flux φ (the charge q), it is called a flux-controlled (charge-controlled) memristor which has many interesting and valuable properties.[1] For example, the passive memristor's memristance $M(q)$ ($M(q) = \mathrm{d}\varphi(q)/\mathrm{d}q$) and memductance $W(\varphi)$ ($W(\varphi) = \mathrm{d}q(\varphi)/\mathrm{d}\varphi$) are non-negative.[2] Moreover, the memristance (memductance) of the memristor depends on the complete history of its current (voltage), and remains constant at the instantaneous value of the moment when the power supply is removed. Furthermore, the i–v curve of the memristor under sinusoidal excitation is a zero-crossing, frequency-dependent pinched hysteresis loop, which is its foremost characteristic property.[2,3]

In spite of so many special features of the new basic element, there is no widespread attention until it was fabricated in HP labs in 2008.[4] After this remarkable work, more and more researchers make their effort to investigate the memristor, and a great number of valuable results have been obtianed in neural networks,[5–8] computer memory,[9–12] analog circuits,[13–21] stochastic impulsive systems,[22] and so on.

As indicated in Ref. [23], an appropriate model of the memristor is necessary for the convenience of theoretical analysis. The memristor is divided into two categories: the charge-controlled memristor and the flux-controlled memristor.[1] For the former, the HP research team proposed a charge-controlled memristor model and its experimental verifying was also carried out.[4] Based on the HP TiO_2 memristor, Joglekar and Wolf proposed a special window function which can ensure zero drift at the boundaries.[13] For the latter, Itoh and Chua presented a 'monotone-increasing' and 'piecewise-linear' q–φ function (PWL) in Ref. [24], and a cubic continuous nonlinear flux-controlled model was proposed in Ref. [25]. Additionally, it is known that commercial memristors are still unavailable in the market due to the cost and technical difficulties in fabricating nanodevices. Hence, a replacement which can imitate the features of the memristor is needed for further research. Several SPICE macromodels, which are very useful for simulating the memristor, were presented in Refs. [26]–[28]. Many excellent works on the hardware emulator which acts like a real memristor and lays a good foundation for experiments have also been reported.[29–33] All of these are practically useful works and have made a great contribution to the research on the memristor.

However, there are still some deficiencies. For example, neither of the flux-controlled models in Refs. [24] and [25] are completely in line with the variation law that the memristance (memductance) should always keep increasing or decreasing (if not approach the boundaries) until the voltage's polarity reverses.[4] This imperfection may cause some inconvenience when the initial phase of the input voltage is changed. Besides, the input (output) currents of the previous emulators are too small (usually less than 10 mA), so they have limitations

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in those situations which demand a larger current. According to the definition of the memristor in Ref. [2], many devices are also considered as memristors because they possess the particular features of the memristor, such as gas discharge arcs, mercury lamps, etc.[2,34–36] Therefore, a flux-controlled model which has the quality that its memductance (memristance) will keep increasing or decreasing unless the voltage's polarity reverses (if not approach the boundaries) and a design of the memristor emulator which can meet various demands for the current through the memristor (especially the demand for a larger current) are of great significance to the research on the memristor. In this paper, a new flux-controlled model based on an exponential function is proposed and its corresponding floating emulator (allows a larger current) is also presented.

The remainder of this paper is organized as follows. The new exponential flux-controlled q–φ function is proposed and discussed in detail in Section 2. In Section 3, the design principle of the floating memristor circuit emulator is described, and some experimental results are presented. The conclusion is given in Section 4.

2. Exponential flux-controlled memristor model

The characteristics of the memristor are determined by the relationship between the charge and the flux, which means that the q–φ curve should be identified at first.[1] From Refs. [1]–[4], the passive memristor is an energy dissipation element, and it cannot discharge or store energy. Thus, its q–φ curve must go through the origin. What is more, because the relationship between q and φ must be nonlinear (a linear relationship will make it a linear resistor) and actual elements always have boundaries, both $M(q)$ and $W(\varphi)$ are positive and non-constant. As described above, the q–φ curve must be zero-crossing, monotonically increasing and nonlinear, as shown in Fig. 1(a).

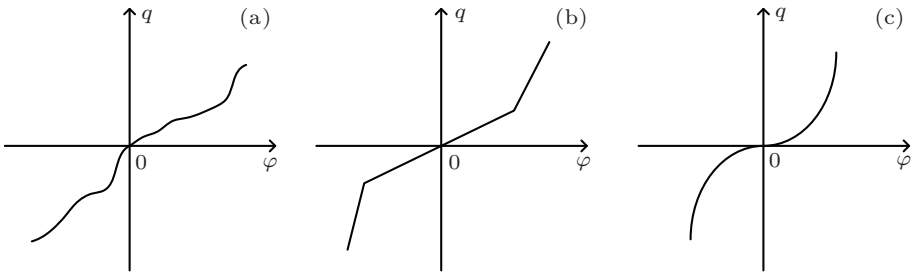


Fig. 1. Schematic diagrams of the q–φ curve of the memristor. (a) Possible q–φ curve of the memristor. (b) The q–φ curve of the PWL model. (c) The q–φ curve of the cubic model.

Up to now, the published papers on the flux-controlled memristor are mainly based on two models: the PWL model[24] and the cubic nonlinearity.[25] In other words, these two models have made a great contribution to the research on the memristor. As indicated in Ref. [4], if the memristance does not approach the boundaries, it will keep increasing or decreasing unless the voltage's polarity reverses. However, the variation laws of the memristances in the two models are not immutable with different excitation voltages. For example, the q–φ function of the cubic flux-controlled model is given by

$$q(\varphi) = \alpha\varphi + \beta\varphi^3. \tag{1}$$

Then, the memductance $W(\varphi)$ can be obtained as

$$W(\varphi) = \alpha + 3\beta\varphi^2. \tag{2}$$

Let $\alpha = 1$, $\beta = 1000$, and $\varphi(t)_{|t=t_0} = 0$. As shown in Fig. 2, by applying the voltage v_1 ($v_1 = V_{\rm m}\sin(2\pi ft)$) to the memristor, the memductance will be monotonically increasing (decreasing) when the instantaneous value of v_1 is positive (negative). However, the $W(\varphi)$–t curve will not be monotonic whether the terminal voltage is in the positive interval or the negative interval when the voltage equals v_2 ($v_2 = V_{\rm m}\sin(2\pi ft + \pi/2)$). In other words, the variation laws of the flux-controlled models' memductances in Refs. [24] and [25] will not always be the same with different excitation voltages, so they have some limitations in applications. For instance, even though the polarity of the terminal voltage has been known, it cannot be easily determined whether the memductances are increasing or not.

The reason for this deficiency can be observed from their q–φ curves. The memductance $W(\varphi)$ ($W(\varphi) = {\rm d}q(\varphi)/{\rm d}\varphi$) is equal to the slope of the q–φ curve. As shown in Figs. 1(b) and 1(c), the slopes of the q–φ curves decrease (increase) gradually as φ increases when φ is less (greater) than 0. Besides, φ is the integral of the voltage ($\varphi(t) \triangleq \int_{-\infty}^{t} v(\tau){\rm d}\tau$). Therefore, the variation laws of those memductances do not always remain the same with different excitation voltages.

To fix the above drawback of the former two models, we propose a novel model of the flux-controlled memristor, which is given by

$$q_1(\varphi) = k(a^{b\varphi} - 1), \tag{3}$$

where $a > 1$, and $kb > 0$. Then, the memductance function of this memristor can be given by

$$W_1(\varphi) = a^{b\varphi}kb\ln a. \tag{4}$$

When $b < 0$, the model of Eq. (3) is a decremental flux-controlled memristor, that is, its memductance is monotonically decreasing (increasing) when the supply voltage is positive (negative), and its q–φ curve is shown in Fig. 3(a). On the contrary, when $b > 0$, equation (3) presents an incremental flux-controlled memristor and the corresponding q–φ curve is shown in Fig. 3(b). In other words, the proposed exponential model has a stable variation law of the memductance (memristance) under various excitation voltages.

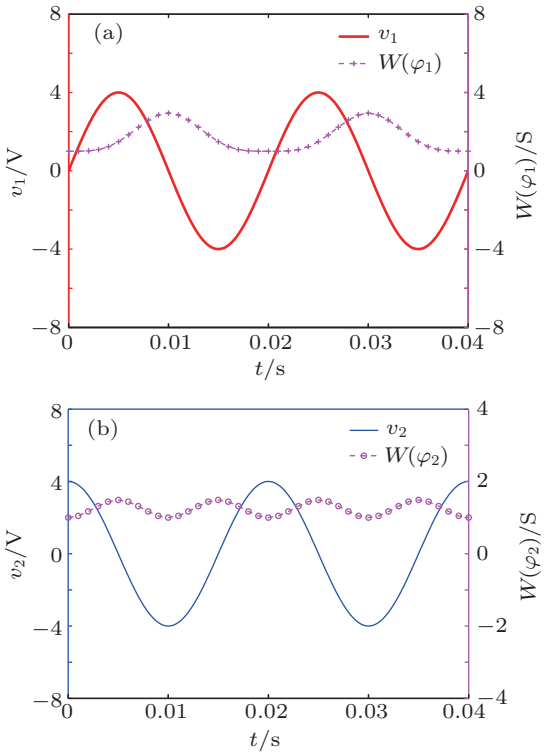


Fig. 2. (color online) Time domain waveforms of the cubic model's memductance under different excitation voltages: (a) excitation voltage v_1, (b) excitation voltage v_2. Here $V_m = 4$ V and $f = 50$ Hz.

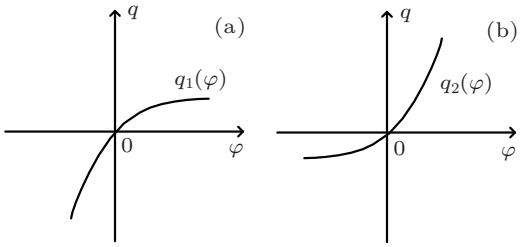


Fig. 3. The q–φ curves of the proposed flux-controlled model: (a) decremental memristor, (b) incremental memristor.

Here, the decremental memristor as an example is discussed in detail. The incremental memristor can be analyzed in the same way. Set the parameters as follows: $a = \mathrm{e}$, $b = 50\ln(0.5)$, and $k = -1/(2500\ln 2)$. Then, from Fig. 4, one can see that the memductance is monotonically decreasing (increasing) when the supply voltage is positive (negative) whether the voltage v_1 ($v_1 = V_m \sin(2\pi f t)$) or v_2 ($v_2 = V_m \sin(2\pi f t + \pi/2)$) is supplied to the decremental memristor.

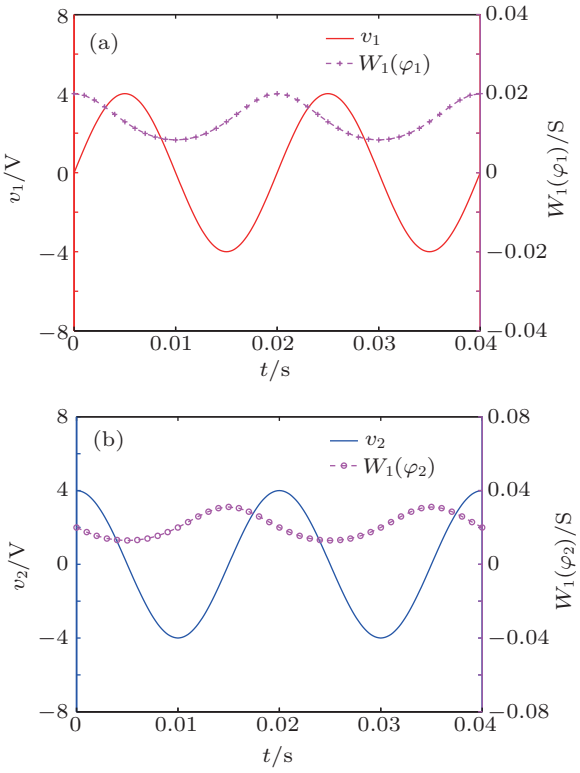


Fig. 4. (color online) Time domain waveforms of the memductance of the decremental memristor under different excitation voltages. $V_m = 4$ V and $f = 50$ Hz. (a) Excitation voltage v_1. (b) Excitation voltage v_2.

Figure 5 shows that the i–v curve of our memristor under sinusoidal excitation is a zero-crossing and frequency-dependent pinched hysteresis loop, which means that the memristor will turn into a linear resistor as the frequency increases. How does the frequency of the supply voltage affect the performance of the memristor? Do the other parameters in Eq. (3) have any effect on the memristor's i–v curve? We take the decremental memristor as an example and supply the voltage v_2 to it. By assuming that the amplitude of the exciting voltage at the initial time ($t = 0$) is 0, i.e., $v = v_2(t)|_{t=0} = 0$, the following formula can be obtained:

$$\varphi(t) = \int_0^t v\left(t'\right) \mathrm{d}t' = \frac{V_m}{\omega} \sin(\omega t), \tag{5}$$

where $\omega = 2\pi f$.

From Eqs. (4) and (5), the relationship between the current through and the voltage across the decremental memristor can be derived as

$$\begin{aligned} i &= W_1(\varphi) v = v a^{b\varphi} k b \ln a \\ &= \begin{cases} v a^{b\sqrt{v_m^2 - v^2}/\omega} k b \ln a, & t \in (0, T/2), \\ v a^{-b\sqrt{v_m^2 - v^2}/\omega} k b \ln a, & t \in (T/2, T). \end{cases} \end{aligned} \tag{6}$$

As shown in Eq. (6), the current i is a double-valued function of the voltage v. What is more, due to $i(v) = -i(-v)$, the i–v curve of the memristor must be odd symmetric with respect to the origin. Accordingly, for simplicity, the i–v curve within (0,

$T/4$) and ($3T/4$, T) is discussed (i.e., the positive interval of v_2). From Fig. 5(b) and the variation law of the decremental memristor's memductance, the i–v curve in $(0, T/4)$ should be a concave curve, while the part in $(3T/4, T)$ should be a convex curve. Note that the convexity or concavity of a curve can be determined by its second derivative. The second derivative of Eq. (6) can be calculated as follows:

$$\begin{cases} i_1'' = \dfrac{kb^2(\ln a)^2 a^{b\sqrt{v_m^2-v^2}/\omega} v}{\omega^2(v_m^2-v^2)^{3/2}} \\ \quad \times (bv^2\sqrt{v_m^2-v^2}\ln a + \omega(2v^2-3V_m^2)), \quad t \in \left(0, \dfrac{T}{2}\right), \\ i_2'' = \dfrac{kb^2(\ln a)^2 a^{-b\sqrt{v_m^2-v^2}/\omega} v}{\omega^2(v_m^2-v^2)^{3/2}} \\ \quad \times (bv^2\sqrt{v_m^2-v^2}\ln a - \omega(2v^2-3V_m^2)), \quad t \in \left(\dfrac{T}{2}, T\right). \end{cases} \tag{7}$$

For the decremental memristor, there should be $i_1'' > 0$ and $i_2'' < 0$ in the positive interval of the supply voltage. Then, it can be obtained that $\omega > -bV_m \ln a$, which means that the memristor will behave like a linear resistor if the supply voltage changes slowly.

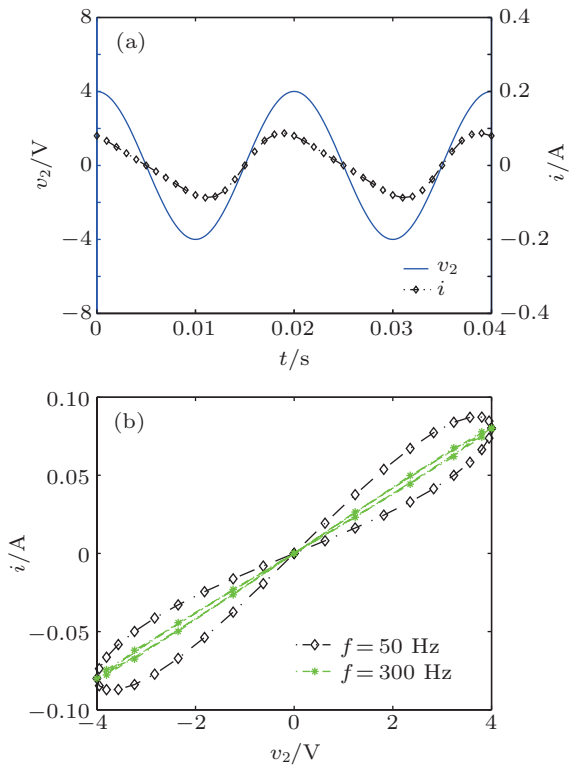


Fig. 5. (color online) The simulation results of the decremental memristor under the exciting voltage v_2. (a) Time domain waveforms of the current when v_2 ($V_m = 4$ V, $f = 50$ Hz) is supplied to the decremental memristor. (b) The i–v curves of decremental memristor with different frequencies.

Figure 6 illustrates the analytical approach about the parameters' effect on the memristor. As depicted in Fig. 6(a), for any two points on the i–v curve of the decremental memristor which have the same abscissa (the voltage), their position relationship can be described by the ratio of their ordinates (the current), i.e.,

$$\lambda = \frac{va^{b\sqrt{v_m^2-v^2}/\omega} kb\ln a}{va^{-b\sqrt{v_m^2-v^2}/\omega} kb\ln a} = a^{2b\sqrt{v_m^2-v^2}/\omega}. \tag{8}$$

From Eq. (8), due to $b < 0$, one can see that λ will gradually close to 1 as b or ω increases. In other words, the decremental memristor will turn into a linear resistor if b or the frequency is too large, as shown in Figs. 5(b) and 6(b).

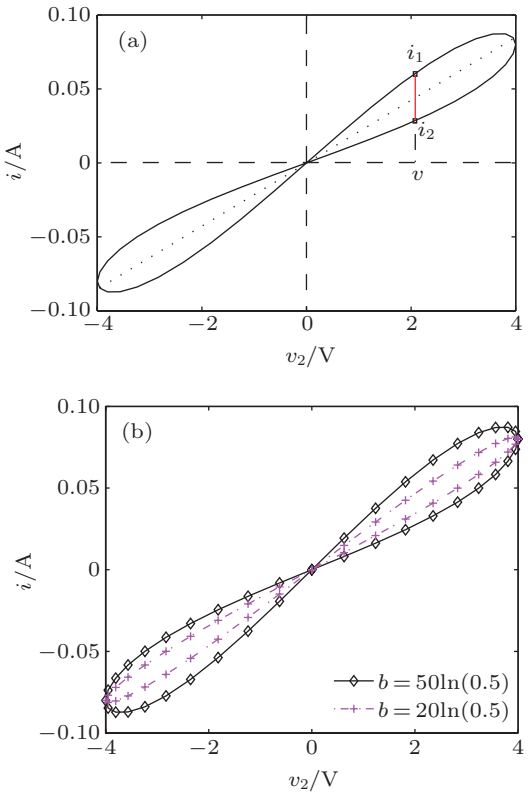


Fig. 6. (color online) Schematic diagrams of the analytical approach about parameters' effect on the memristor. (a) Position relationship of the selected two points. (b) The i–v curves of decremental memristor with different values of b when v_2 is supplied to the decremental memristor. Here $f = 50$ Hz, and $a =$ e.

Above all, the model (3) possesses the features of the memristor and ensures that the variation law of its memristance never changes under different exciting voltages.

3. Design and experiments of the floating memristor emulator circuit

According to Eq. (6) and by considering that φ is the integral of the terminal voltage v, the floating emulator for the decremental memristor can be designed by a rational combination of the multiplication circuit, the integrated circuit, the adder circuit, the subtraction circuit, the exponential circuit, and the floating structures. The full schematic of the floating decremental memristor emulator is depicted in Fig. 7.

The multiplication circuit is implemented by an analog multiplier AD633 whose output voltage v_7 is one-tenth of the product of the '1 input voltage' and '3 input voltage'.

The output voltage of the operational amplifier A_N is denoted by v_{AN}, where N is a natural number. The subtraction circuit, which consists of A_1, A_2, and A_3 is used to obtain the voltage across the memristor v_{in}. The capacitor C_1, A_4, and A_5 produce the flux φ by integrating v_{in}.

The exponential circuit is implemented by a monolithic antilogarithmic amplifier ICL8049 and its output voltage can be approximately given by

$$v_{10} = R_{out}\frac{v_P}{R_7}\,e^{-v_{A5}f(R_6)}. \tag{9}$$

The function $f(R_6)$ is the scale factor which is a single-valued function of R_6. By connecting the input to a precise 1 V supply and adjusting the potentiometer R_6 for $v_{10} = 1$ V, one can obtain $f(R_6) = -\ln(0.5)$.

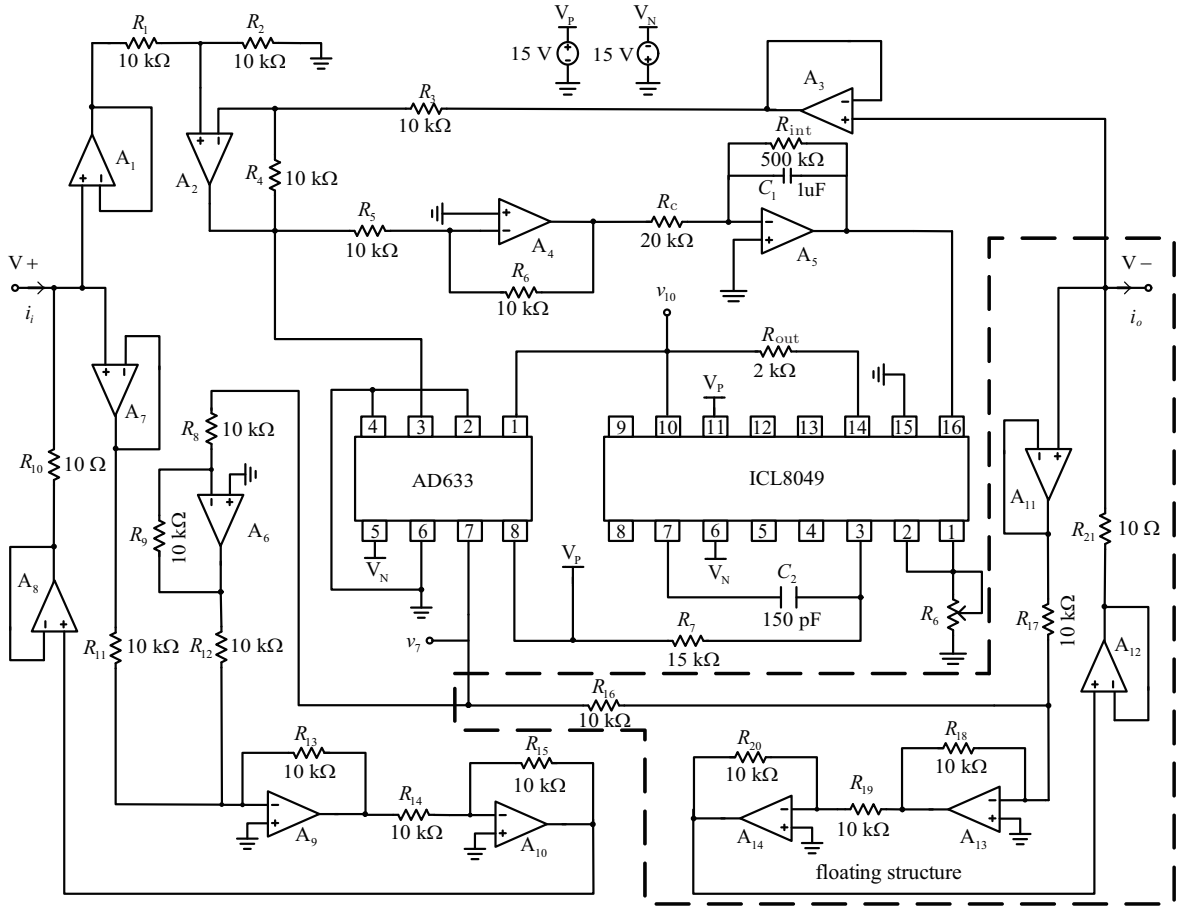


Fig. 7. Full schematic of the floating decremental memristor emulator.

As shown in Fig. 7, the floating structure of the input terminal of the emulator consists of A_6, A_7, A_8, A_9, and A_{10}, while that of the output terminal is composed of A_{11}, A_{12}, A_{13}, and A_{14}. The resistor R_{10} is equal to R_{21}. Note that the input currents of the operational amplifiers are so small that they can be ignored. Then, the following equations can be obtained:

$$v_{A13} = -(v_{A11} + v_7) = -(v_- + v_7), \tag{10}$$

$$v_{A12} = v_{A14} = -v_{A13} = v_- + v_7, \tag{11}$$

$$i_o = (v_{A12} - v_-)/R_{21} = v_7/R_{21}. \tag{12}$$

In the same way, the input current of the emulator can be given by

$$i_i = v_7/R_{10} = i_o. \tag{13}$$

According to the above analysis, the following equations (assuming that the initial voltage across the capacitor C_1 is 0 V) can be derived:

$$v_{A2} = v_+ - v_- = v_{in}, \tag{14}$$

$$v_{A5} = \frac{1}{R_c C_1}\int_{-\infty}^{t} v_{in}\,dt = \frac{\varphi}{R_c C_1}, \tag{15}$$

$$v_7 = v_{A2} \times v_{10}/10. \tag{16}$$

From Eqs. (9) and (14)–(16), one can obtain

$$i_i = i_o = \frac{R_{out} v_P}{10 R_7 R_{10}}\,e^{-\varphi f(R_6)/R_c C_1} \times (v_+ - v_-). \tag{17}$$

By comparing Eq. (17) with Eq. (6), the parameters of the pro-

posed decremental memristor can be calculated as follows:

$$\begin{cases} a = \mathrm{e}, \\ b = -f(R_6)/(R_\mathrm{c}C_1) = 50\ln(0.5), \\ k = -R_\mathrm{out}v_\mathrm{P}R_\mathrm{c}C_1/(10R_7R_{10}f(R_6)) = -1/(2500\ln 2). \end{cases} \tag{18}$$

From Eqs. (17) and (18), one can see that it is effective to use the designed circuit in Fig. 7 to implement the proposed decremental memristor. At the same time, the input current of the memristor emulator is equal to the output current, which means that the emulator is floating-ground. Moreover, this design of floating structure can be flexible enough to satisfy different demands for the current through the memristor (especially the demand for a larger current) simply by selecting different types of amplifiers to implement A_8 (A_{12}) and adjusting the resistor R_{10} (R_{21}). For instance, if A_8 and A_{12} are implemented by the high-voltage and high-current operation amplifiers, a larger input (output) current can be conveniently obtained. Furthermore, this design approach can also be used to improve other emulators with ground restriction. If the antilog amplifier ICL8049 in Fig. 7 is replaced by a multiplication circuit and an adder circuit, figure 7 will turn into a floating schematic of the emulator proposed in the Ref. [25].

In order to further verify the effectiveness of the floating memristor emulator, some experimental results are presented. In our experiment, the voltage probe Gwinstek GTP-151R is used to detect the input (output) terminal voltage to ground (v_+ (v_-)) and the output voltage of the ICL8049 (v_{10}), and the differential probe Tektronix P5200A is used to detect the terminal voltage across the decremental memristor emulator v_in. The current probe Tektronix A622 is used to detect the input (output) terminal current i_i (i_o). The digital storage oscilloscope Gwinstek GDS-3254 is used to measure and capture the measured waveforms from the probes.

In addition, all the operation amplifiers shown in Fig. 7 except A_8 and A_{12} are implemented by LF356. The A_8 and A_{12} are implemented by the high-voltage and high-current operation amplifiers OPA551 to facilitate the measurements of the terminal current. The R_{10} and R_{21} are implemented by power resistors.

As shown in Fig. 8, channels 3 and 4 of the oscilloscope Gwinstek GDS-3254 are used to capture the input terminal voltage to ground (v_+) and the output terminal voltage to ground (v_-), respectively. It can be observed that both of them are floating. The channel 1 is used to capture the voltage across the emulator (v_in). The red line has displayed the result of 'CH3–CH4 (i.e., $v_+ - v_-$)' by using the math subtract function in the oscilloscope Gwinstek GDS-3254, and it is in good agreement with v_in. In other words, the emulator is working at the floating-ground situation and the voltage across the emulator is $v_\mathrm{in} = v_+ - v_- = V_\mathrm{m}\sin(2\pi ft + \pi/2)$ in the experiment, where $V_\mathrm{m} = 4$ V and $f = 50$ Hz.

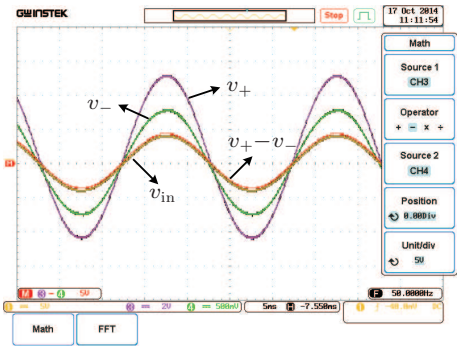


Fig. 8. (color online) The measurements of the input terminal voltage to ground, the output terminal voltage to ground, and the voltage across the emulator. X-axis: 5 ms/div; Y-axis: 5 V/div for v_in, 2 V/div for v_+, 500 mV/div for v_-, 5 V/div for v_M, 5 V/div for $(v_+ - v_-)$.

By comparing Eq. (17) with Eq. (9), it can be observed that $v_{10} = 10R_{10}W(\varphi) = 100W(\varphi)$. Thus, the time-domain waveforms of v_{10} can be used as a substitute for $W(\varphi)$ to observe the variation law of the memductance. The experimental results about the variation of the memductance along the time are shown in Fig. 9, which agree very well with the analytical results in Fig. 4(b), i.e., v_{10} is monotonically decreasing (increasing) when the terminal voltage v_in is positive (negative), and these prove that the emulator can represent a decremental memristor.

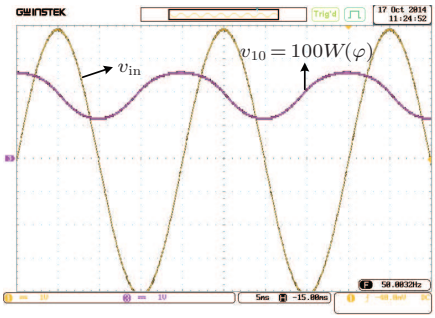


Fig. 9. (color online) Variations of the memductance with time. X-axis: 5 ms/div; Y-axis: 1 V/div.

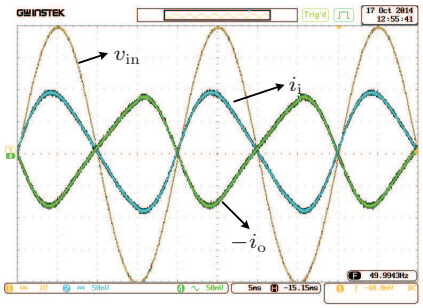


Fig. 10. (color online) The time domain waveforms of the currents flowing into the input terminal and the output terminal of the emulator. X-axis: 5 ms/div; Y-axis: 1 V/div for v_in, 50 mA/div for i_i, 50 mA/div for i_o.

In order to observe the terminal current, channels 2 and 4 are used to capture the currents flowing in the input terminal and the output terminal of the emulator, respectively. As shown in Fig. 10, the current into the input terminal is consistent with the current from the output terminal, which proves

the validity of the floating memristor emulator. The experimental results in Fig. 10 also agree very well with Fig. 5(a). Note that the input (output) currents' peak has been approximated to 100 mA.

The i–v curves of the emulator in Fig. 11 show that the curve will tend to be a straight line as the excitation frequency increases.

From Eq. (18), one can see that the value of b can be adjusted by the product of R_cC_1. Figure 12 shows that the i–v curve of the emulator is very close to a straight line when b is large enough.

To sum up, the experimental results here are in agreement with the theoretical analysis. Therefore, the design scheme for a floating memristor emulator proposed here is effective.

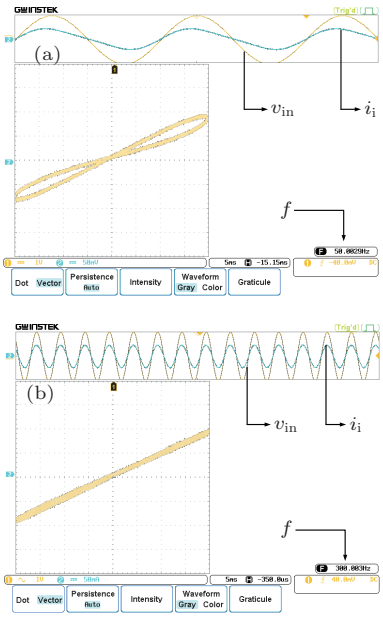


Fig. 11. (color online) The i–v curves of the emulator: (a) $f = 50$ Hz, (b) $f = 300$ Hz. The horizontal axis represents v_{in}, while the vertical axis represents i_i.

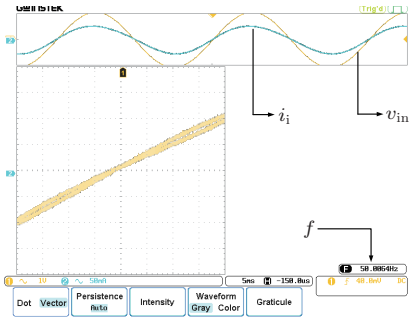


Fig. 12. (color online) The i–v curves of the emulator when b is larger. The horizontal axis represents v_{in}, while the vertical axis represents i_i. Here $f = 50$ Hz, $R_c = 50$ kΩ, and $C_1 = 1$ μF.

4. Conclusion

This paper mainly focuses on two important matters in the research on the memristor: a model with a stable variation law of the memductance (memristance) under various excitation voltages and a floating hardware circuit that can emulate the features of the memristor and allow a larger input (output) current. The former is resolved by using the exponential function to improve the flux-controlled model. The latter is implemented by a rational combination of some off-the-shelf solid state devices. The experimental results are in good agreement with the theoretical analysis.

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