Composite behaviors of dual meminductor circuits*

Zheng Ci-Yan(郑辞晏)[a], Yu Dong-Sheng(于东升)[a]†, Liang Yan(梁 燕)[a], and Chen Meng-Ke(陈孟科)[b]

[a] School of Information and Electrical Engineering, China University of Mining and Technology, Xuzhou 221116, China
[b] School of Mechanical Engineering, Huaihai Institute of Technology, Lianyungang 222005, China

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This paper focuses on analyzing the composite dynamic behaviors of two meminductors in serial and parallel connections with different polarities. Based on the constitutive relations, two time-integral-of-flux (TIF) controlled meminductors are adopted to theoretically demonstrate the variation of memductance in terms of TIF, charge, flux, and current. By utilizing a floating memristor-less meminductor emulator, the theoretical analysis reported in this paper is confirmed via a PSPICE simulation study and hardware experiment. Good agreement among theoretical analysis, simulation, and hardware validation confirms that dual meminductor circuits in composite connections behave as a new meminductor with higher complexity.

Keywords: composite behavior, serial connection, parallel connection, meminductor

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1. Introduction

In the year of 1971 and 1976, Chua,[1] Chua and Kang[2] predicted the existence of the fourth two-terminal fundamental circuit element out of existing ones (resistor, inductor, and conductor). This new element is called a memristor (MR), whose mathematical model is based on the charge–flux relationship. The research work of the MR did not draw enough attention until May 2008, when the HP lab managed to find a nanoscale solid-state device possessing the properties of an MR.[3] In 2009, the definitions of meminductive and memcapacitive systems were extensively brought forward and then the special cases of memcapacitors (MCs) and meminductors (MLs) were symmetrically described.[4] Pinched hysteretic loops, regarded as a typical fingerprint of MR, MC, and ML, are also depicted in detail in Ref. [5].

Unlike the MR, there are no practical nano devices capable of characterizing ML and MC, thus many emulators have been proposed to mimic ML and MC for further research. However, many of the existing ML models possess disadvantages more or less, such as, being hard to fabricate, or application complexity, or grounded restriction. For instance, an anolog ML emulator has been constructed on the basis of an MR emulator consisting of a light-dependent resistor (LDR),[6] and this ML emulator can be easily implemented in practical circuit but has grounded restriction. In Ref. [7] an ML emulator without employing any memristive system was designed, however, only SPICE simulation was given for validation. Meanwhile, many effective mutators were proposed to transform MR into an ML or a meminductive system: in Refs. [8] and [9], universal mutators to transform a grounded MR into a floating ML were reported, although no practical experiment was given; in Ref. [10], a mutator to transfer an MR into a meminductive system with floating terminals was proposed and its relevant practical implementation was presented. The MR-based circuit may render the newly-built ML much complex. Recently, in Ref. [11], there has been proposed a practical floating flux-controlled ML emulator without requiring any MR.

Many research efforts have focused on probing the dynamic behaviors of circuits containing one single mem-element, such as manifolds of non-isolated equilibria of mem-circuits,[12] the responses of ML under various current excitation signals like DC, sinusoidal, and periodic current signals,[13] the behavior of MC under step and sinusoidal voltage excitations[14] and so forth.

On the other hand, the dynamic behaviors of circuits containing more than one MR element have already been studied. It is shown in Refs. [15] and [16] that compared with the connection of a single MR, composite connections of two MRs, or an MR in parallel with an inductor or a capacitor can generate diversified dynamic behaviors. Based on Ref. [15], in Ref. [17] the dynamic behaviors of composite MRs were studied with taking the coupling effect between two MRs into consideration. However, the dynamic behaviors of multiple MLs connected together have not fully been studied yet. Unlike MR, ML is a dynamic element with the ability to store energy. Circuits containing one ML with resistors or MRs are characterized as the first-order dynamic circuits. However, composite behaviors of dynamic circuits containing dual or more MLs are rarely discovered and undeniably deserve more concerns.

In addition, to probe the dynamic behaviors of composite MLs can facilitate the development process of ML-

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†Corresponding author. E-mail: dongsiee@163.com
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based application circuits. Until now, research interests related to potential applications of MLs include designing adaptive filters with controllable inductance,[18] building a chaotic signal generator,[19] implementing digital low-power computation[20] and fast computation.[21]

In the present work, inspired by the work about composite MR circuits, dynamic behaviors of two MLs in serial and parallel connections with different polarities are discussed innovatively. The rest of this paper is organized as follows. In Section 2, a brief description of a single ML is introduced. In Section 3, MLs in serial connections with two different polarities are discussed. Furthermore, an additional inductor is serially added to this serial ML circuit in order to further testify its dynamic characteristic. Similarly, in Section 4, results of MLs in parallel connections with two different polarities are given, along with an extra inductor in serial connection. In Sections 5 and 6, a practical time-integral-of-flux controlled ML emulator is used to validate the theoretical analysis by using PSPICE simulation and hardware experiment, respectively. In Section 7, concluding remarks are presented.

2. Brief description of ML

As previously defined by Chua, the basic constitutive variables of MR are charge q and flux φ, which are the integral of current and voltage, respectively. The integration enables MR to have the ability to memorize the past circuit history.[1] There exist different ways to define the constitutive relations of ML, one is stated in Ref. [22], which continues to take charge q and flux φ as two variables, the other is stated in Ref. [4], showing that by defining ρ as the time integral of flux (TIF), meminductive systems can be divided into charge-controlled and ρ-controlled ones. The basic relations between voltage and flux, flux and ρ can be written as follows:

$$\int_{t_0}^{t} v\,\mathrm{d}t = \varphi, \quad \int_{t_0}^{t} \varphi\,\mathrm{d}t = \rho. \tag{1}$$

By using L_{M} and L_{M}^{-1} to denote meminductance and the inverse meminductance respectively, the definitive equations of two different types of ML are listed in Table 1.

Table 1. Definitive equations of two different kinds of MLs.

ML categories	Terminal equation	Parametric equations
Charge-controlled ML	$\varphi(t) = L_{\mathrm{M}}(t)i(t)$	$\rho = \hat{\rho}(q), L_{\mathrm{M}}(q) = \mathrm{d}\hat{\rho}(q)/\mathrm{d}q$
ρ-controlled ML	$i(t) = L_{\mathrm{M}}^{-1}(\rho)\varphi(t)$	$q = \hat{q}(\rho), L_{\mathrm{M}}^{-1}(\rho) = \mathrm{d}\hat{q}(\rho)/\mathrm{d}\rho$

From Table 1, we can see that MLs can be classified as charge-controlled and ρ-controlled MLs. In this paper, we only take the ρ-controlled ML into consideration.

As defined in Table 1, the current, inverse meminductance, flux, charge, and the ρ are related by

$$i(t) = L_M^{-1}(\rho)\varphi(t), \tag{2}$$

$$L_{\mathrm{M}}^{-1}(\rho) = \frac{\mathrm{d}\hat{q}(\rho)}{\mathrm{d}\rho}. \tag{3}$$

Obviously, from Eq. (2), L_{M} can be detected by measuring the slope of the φ–i curve. According to Eqs. (2) and (3), a ρ-controlled ideal meminductive system with two MLs can be defined by

$$i_1(t) = L_{\mathrm{M}}^{-1}(\rho_1)\varphi_1(t), \tag{4}$$

$$i_2(t) = L_{\mathrm{M}}^{-1}(\rho_2)\varphi_2(t), \tag{5}$$

$$\frac{\mathrm{d}\rho_1}{\mathrm{d}t} = \varphi_1(t), \quad \frac{\mathrm{d}\rho_2}{\mathrm{d}t} = \varphi_2(t). \tag{6}$$

In Refs. [6]–[11], several SPICE emulator circuits have been proposed to mimic the dynamic behaviors of ML. For the sake of analysis simplicity, the ρ-controlled ML in Ref. [11] is taken into account, of which the inverse meminductance is in proportion to TIF with coefficient α, namely

$$L_{\mathrm{M}}^{-1}(\rho) = \alpha\rho + \beta, \tag{7}$$

where β is the initial value of L_{M}^{-1}. Considering Eqs. (4)–(7), the individual inverse meminductances of two individual MLs can be rewritten as

$$L_{\mathrm{M1}}^{-1}(\rho) = \alpha_1\rho_1 + \beta_1, \tag{8}$$

$$L_{\mathrm{M2}}^{-1}(\rho) = \alpha_2\rho_2 + \beta_2. \tag{9}$$

In the following sections, two MLs described by Eqs. (8) and (9) are used for analyzing the composite behaviors of dual ML based circuits.

3. MLs in serial connections

Figure 1 shows the symbol of a single ML. There are several ways to connect dual MLs in a circuit. Firstly, the scenario of two MLs connected in series with different polarities is discussed in this section.

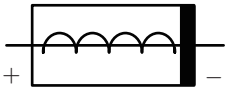


Fig. 1. The symbol of a single ML.

3.1. Serial ML circuit with identical polarities

Figure 2 shows the schematic diagram of two MLs connected in series with identical polarities. When the input excitation voltage v_{12} is applied to this serial circuit between terminals A_1 and A_2, according to Kirchhoff's voltage law (KVL),

the voltage and current relation of each ML can be expressed as

$$v_{12} = v_1 + v_2, \tag{10}$$

$$i = L_{\mathrm{M1}}^{-1}(\rho)\varphi_1(t) = L_{\mathrm{M2}}^{-1}(\rho)\varphi_2(t). \tag{11}$$

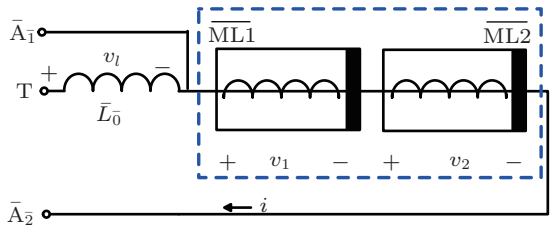


Fig. 2. (color online) MLs connected in series with identical polarities.

By integrating both sides of Eq. (10), relations between the two fluxes can be presented by

$$\varphi_{12} = \varphi_1 + \varphi_2, \tag{12}$$

where φ_1 and φ_2 are the time integrals of v_1 and v_2, respectively. In addition, by integrating both sides of Eq. (12), the following relation can be obtained:

$$\rho_{12} = \rho_1 + \rho_2. \tag{13}$$

By combining Eqs. (8), (9), and (11), the expression of current can be calculated by

$$i = (\alpha_1\rho_1 + \beta_1)\varphi_1(t) = (\alpha_2\rho_2 + \beta_2)\varphi_2(t). \tag{14}$$

Based on Eq. (14) and assuming the initial value of ρ to be zero, we can obtain

$$\frac{1}{2}\alpha_1\rho_1^2 + \beta_1\rho_1 = \frac{1}{2}\alpha_2\rho_2^2 + \beta_2\rho_2. \tag{15}$$

From Eq. (13), ρ_2 can be replaced by $(\rho_{12}–\rho_1)$, thus we can obtain the following equation:

$$\frac{1}{2}\alpha_1\rho_1^2 + \beta_1\rho_1 = \frac{1}{2}\alpha_2(\rho_{12} - \rho_1)^2 + \beta_2(\rho_{12} - \rho_1). \tag{16}$$

Equation (16) is a second-order resolvable equation with unknown variable ρ_1. The analytical expressions of ρ_1 and ρ_2 can be rewritten by

$$\rho_1 = \frac{\sqrt{(\beta_1+\beta_2+\alpha_2\rho_{12})^2 + (\alpha_1-\alpha_2)\left(\rho_{12}^2 + 2\beta_2\rho_{12}\right)} - (\beta_1+\beta_2+\alpha_2\rho_{12})}{\alpha_1-\alpha_2}, \tag{17}$$

$$\rho_2 = \frac{\alpha_1\rho_{12} + \beta_1 + \beta_2 + \sqrt{(\beta_1+\beta_2+\alpha_2\rho_{12})^2 + (\alpha_1-\alpha_2)\left(\rho_{12}^2 + 2\beta_2\rho_{12}\right)}}{\alpha_1-\alpha_2}. \tag{18}$$

If we take the special case of $\alpha_1 = \alpha_2 = \alpha$ for demonstration, equation (16) can be simplified into

$$\rho_1(\beta_1 + \beta_2 + \alpha\rho_{12}) = \frac{1}{2}\alpha\rho_{12}^2 + \beta_2\rho_{12}. \tag{19}$$

As a result, the expressions of ρ_1 and ρ_2 can be simplified into

$$\rho_1 = \frac{\alpha\rho_{12}^2 + 2\beta_2\rho_{12}}{2(\beta_1+\beta_2+\alpha\rho_{12})}, \tag{20}$$

$$\rho_2 = \frac{\alpha\rho_{12}^2 + 2\beta_1\rho_{12}}{2(\beta_1+\beta_2+\alpha\rho_{12})}. \tag{21}$$

Therefore, the inverse meminductance of individual ML can be obtained by substituting Eqs. (20) and (21) into Eqs. (8) and (9) respectively, leading to

$$L_{\mathrm{M1}}^{-1}(\rho) = \alpha\frac{\alpha\rho_{12}^2 + 2\beta_2\rho_{12}}{2(\beta_1+\beta_2+\alpha\rho_{12})} + \beta_1, \tag{22}$$

$$L_{\mathrm{M2}}^{-1}(\rho) = \alpha\frac{\alpha\rho_{12}^2 + 2\beta_1\rho_{12}}{2(\beta_1+\beta_2+\alpha\rho_{12})} + \beta_2. \tag{23}$$

For further simplification, we assume $\beta_1 = \beta_2 = \beta$, which leads to

$$\rho_1 = \rho_2 = \frac{1}{2}\rho_{12}, \quad \varphi_1 + \varphi_2 = \frac{1}{2}\varphi_{12}, \quad v_1 + v_2 = \frac{1}{2}v_{12}. \tag{24}$$

According to Eq. (24), we can obtain that

$$L_{\mathrm{M1}}^{-1} = L_{\mathrm{M2}}^{-1} = \frac{\alpha^2\rho_{12}^2 + 2\alpha\beta\rho_{12}}{4\beta + 2\alpha\rho_{12}} + \beta = \alpha\frac{\rho_{12}}{2} + \beta. \tag{25}$$

For two serially connected inductors L_1 and L_2, their composite inverse inductance is supposed to be $1/(L_1+L_2)$. Similarly, in an MLs's circuit, the composite inverse meminductance can be calculated from

$$L_{\mathrm{M12}}^{-1} = \frac{L_{\mathrm{M1}}^{-1}L_{\mathrm{M2}}^{-1}}{L_{\mathrm{M1}}^{-1} + L_{\mathrm{M2}}^{-1}}. \tag{26}$$

Thus, the composite inverse meminductance can be induced based on Eq. (25) as follows:

$$L_{\mathrm{M12}}^{-1} = \frac{L_{\mathrm{M1}}^{-1}}{2} = \frac{L_{\mathrm{M2}}^{-1}}{2} = \left(\frac{\alpha\rho_{12}}{4} + \frac{\beta}{2}\right). \tag{27}$$

Obviously, when connected in a series with identical polarities, two MLs can surely be operated as a new ML, which has linear ρ-controlled inverse meminductance.

3.2. Serial MR circuit with opposite polarities

In this subsection, two MLs connected in a series with opposite polarities are taken into account as shown in Fig. 3.

When the input excitation voltage v_{12} is applied to this serial circuit between terminals A_3 and A_4, the voltages, fluxes and the values of ρ can be related by

$$v_{12} = v_1 + v_2, \quad \varphi_{12} = \varphi_1 + \varphi_2, \quad \rho_{12} = \rho_1 + \rho_2. \tag{28}$$

In this scenario, the expression of current leads to

$$i = (\alpha_1\rho_1 + \beta_1)\varphi_1(t) = (-\alpha_2\rho_2 + \beta_2)\varphi_2(t). \tag{29}$$

Similarly, by integrating both sides of Eq. (29) and substituting ρ_2 by $(\rho_{12}–\rho_1)$, the following equation can be obtained:

$$\frac{1}{2}\alpha_1\rho_1^2 + \beta_1\rho_1 = -\frac{1}{2}\alpha_2(\rho_{12} - \rho_1)^2 + \beta_2(\rho_{12} - \rho_1). \tag{30}$$

This equation can be analytically solved as

$$\rho_1 = \frac{-(\beta_1 + \beta_2 - \alpha_2\rho_{12}) + \sqrt{(\beta_1 + \beta_2 - \alpha_2\rho_{12})^2 - (\alpha_1 + \alpha_2)\left(\alpha_2\rho_{12}^2 - 2\beta_2\rho_{12}\right)}}{\alpha_1 + \alpha_2}, \tag{31}$$

$$\rho_2 = \frac{\alpha_1\rho_{12} + \beta_1 + \beta_2 - \sqrt{(\beta_1 + \beta_2 - \alpha_2\rho_{12})^2 - (\alpha_1 + \alpha_2)\left(\alpha_2\rho_{12}^2 - 2\beta_2\rho_{12}\right)}}{\alpha_1 + \alpha_2}. \tag{32}$$

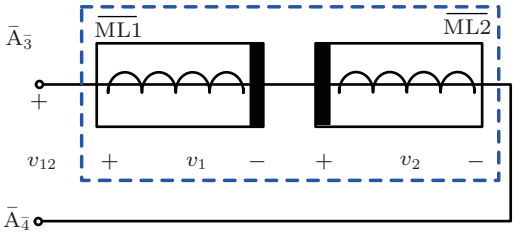


Fig. 3. (color online) MLs connected in a series with opposite polarities.

Likewise, by setting $\alpha_1 = \alpha_2 = \alpha$ and $\beta_1 = \beta_2 = \beta$, ρ_1 and ρ_2 can be simplified into

$$\rho_1 = \frac{-2\beta + \alpha\rho_{12} + \sqrt{4\beta^2 - \alpha^2\rho_{12}^2}}{2\alpha}, \tag{33}$$

$$\rho_2 = \frac{2\beta + \alpha\rho_{12} - \sqrt{4\beta^2 - \alpha^2\rho_{12}^2}}{2\alpha}. \tag{34}$$

Hence, the inverse meminductance of an individual ML can be obtained by substituting Eqs. (33) and (34) into Eqs. (8) and (9) respectively, leading to

$$L_{\mathrm{M1}}^{-1} = \frac{\alpha\rho_{12} + \sqrt{4\beta^2 - \alpha^2\rho_{12}^2}}{2}, \tag{35}$$

$$L_{\mathrm{M2}}^{-1} = \frac{-\alpha\rho_{12} + \sqrt{4\beta^2 - \alpha^2\rho_{12}^2}}{2}. \tag{36}$$

To further investigate the dynamic behavior of dual MLs connected in a series, an extra inductor L_0 is adopted in serial connection with these two MLs as depicted in Fig. 2. The input voltage v_{12} is now applied between terminals T and A2. The voltages, fluxes, and values of ρ can be related correspondingly by

$$v_{12} = v_l + v_1 + v_2, \quad \varphi_{12} = \varphi_l + \varphi_1 + \varphi_2,$$
$$\rho_{12} = \rho_l + \rho_1 + \rho_2. \tag{37}$$

The current flowing through each circuit element is

$$i = \varphi_{\mathrm{L}}L_0^{-1} = \varphi_1(t)(\alpha_1\rho_1 + \beta_1) = \varphi_2(t)(\alpha_2\rho_2 + \beta_2). \tag{38}$$

By substituting Eq. (38) into Eq. (37), we have

$$\varphi_{12} = \varphi_L + \varphi_1 + \varphi_2 = iL_0 + \frac{i}{\alpha_1\rho_1 + \beta_1} + \frac{i}{\alpha_2\rho_2 + \beta_2}. \tag{39}$$

Then the value of the current can be represented as

$$\begin{aligned} i &= \frac{\varphi_{12}}{L_0 + \dfrac{1}{\alpha_1\rho_1 + \beta_1} + \dfrac{1}{\alpha_2\rho_2 + \beta_2}} \\ &= L_{\mathrm{M1}}^{-1}(\rho)\varphi_1(t) = L_{\mathrm{M2}}^{-1}(\rho)\varphi_2(t). \end{aligned} \tag{40}$$

Thus the expression of flux can be written as

$$\begin{aligned} \varphi_1(t) &= \frac{i}{L_{\mathrm{M1}}^{-1}} \\ &= \frac{\varphi_{12}}{\left(L_0 + \dfrac{1}{\alpha_1\rho_1 + \beta_1} + \dfrac{1}{\alpha_2\rho_2 + \beta_2}\right)(\alpha_1\rho_1 + \beta_1)}, \end{aligned} \tag{41}$$

$$\varphi_1(t) = \frac{\varphi_{12}(\alpha_2\rho_2 + \beta_2)}{L_0(\alpha_1\rho_1 + \beta_1)(\alpha_2\rho_2 + \beta_2) + \alpha_1\rho_1 + \beta_1 + \alpha_2\rho_2 + \beta_2}, \tag{42}$$

$$\varphi_2(t) = \frac{\varphi_{12}(\alpha_1\rho_1 + \beta_1)}{L_0(\alpha_1\rho_1 + \beta_1)(\alpha_2\rho_2 + \beta_2) + \alpha_1\rho_1 + \beta_1 + \alpha_2\rho_2 + \beta_2}. \tag{43}$$

In view of Eq. (6), the expression of ρ can be calculated through the integration of the flux. However, equations (42) and (43) can be hardly resolved analytically. By taking into account the special case of $\alpha_1 = \alpha_2 = \alpha$ and $\beta_1 = \beta_2 = \beta$, and considering Eq. (24), the values of ρ for two MLs are the same

$$\rho_1 = \rho_2, \tag{44}$$

$$\begin{aligned} \varphi_1(t) = \varphi_2(t) &= \frac{\mathrm{d}\rho}{\mathrm{d}t} = \frac{\varphi_{12}(\alpha\rho + \beta)}{L_0(\alpha\rho + \beta)^2 + 2(\alpha\rho + \beta)} \\ &= \frac{\varphi_{12}}{L_0(\alpha\rho + \beta) + 2}. \end{aligned} \tag{45}$$

Consequently, the expression of ρ is

$$\rho = \frac{1}{2L_0}\ln[L_0(\alpha\rho + \beta) + 2]. \tag{46}$$

The expression of the composite inverse meminductance can be obtained by substituting Eq. (46) into Eqs. (8) and (9), then calculated through Eq. (26) as

$$L_{\mathrm{M12}}^{-1}(\rho)=\frac{\alpha}{4L_0}\ln[L_0(\alpha\rho+\beta)+2]+\frac{\beta}{2}. \tag{47}$$

4. MLs in parallel connections

In this section, MLs are configured in parallel connections in consideration of two different polarity cases.

4.1. Parallel ML circuit with identical polarities

As is depicted in Fig. 4, ML1 and ML2 are connected in parallel with identical polarities. For parallel connections, when the input voltage v_{12} is applied between terminals B_1 and B_2, the voltages, fluxes, and values of ρ can be related correspondingly by

$$v_1=v_2=v_{12},\quad \varphi_1=\varphi_2=\varphi_{12},\quad \rho_1=\rho_2=\rho_{12}. \tag{48}$$

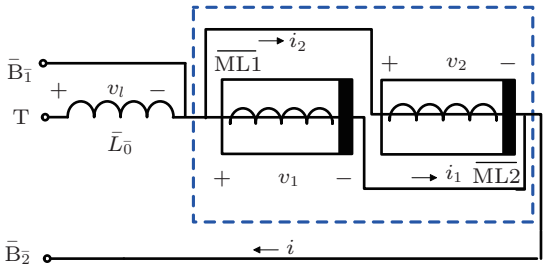


Fig. 4. (color online) MLs connected in parallel with identical polarities.

According to Kirchhoff's current law (KCL), the total current i is equal to the sum of i_1 and i_2, namely

$$i=i_1+i_2. \tag{49}$$

By substituting Eqs. (4) and (5) into Eq. (49), we have

$$\begin{aligned} i &= (\alpha_1\rho_1+\beta_1)\varphi_1+(\alpha_2\rho_2+\beta_2)\varphi_2 \\ &= (\alpha_1+\alpha_2)\rho_{12}\varphi_{12}+(\beta_1+\beta_2)\varphi_{12}. \end{aligned} \tag{50}$$

Then we integrate both sides of Eq. (50) by considering the special initial value condition of charge equal to zero, and obtain

$$q=\frac{1}{2}(\alpha_1+\alpha_2)\rho_{12}^2+(\beta_1+\beta_2)\rho_{12}. \tag{51}$$

According to Eq. (3), the inverse composite meminductance can be obtained by taking derivatives of Eq. (51), and the calculated result is

$$L_{\mathrm{M12}}^{-1}(\rho)=\frac{\mathrm{d}q(\rho_{12})}{\mathrm{d}\rho_{12}}=(\alpha_1+\alpha_2)\rho_{12}+(\beta_1+\beta_2). \tag{52}$$

From Eq. (52), we can draw the conclusion that MLs in parallel connections can also be recognized as a new ρ-controlled ML with inverse meminductance equal to the sum of two individual inverse meminductances. Equation (52) is in good agreement with the expected theoretical results of two parallel connected MLs as $L_{\mathrm{M12}}^{-1}=L_{\mathrm{M1}}^{-1}+L_{\mathrm{M2}}^{-1}$.

4.2. Parallel ML circuit with opposite polarities

When two MLs are connected in parallel with opposite polarities as shown in Fig. 5, and the input voltage v_{12} is applied to terminals B_3 and B_4, the relations among voltages, fluxes and values of ρ are the same as those presented in Eq. (48). Likewise, the relation between currents is identical to that in Eq. (49). Owing to the opposite polarities of MLs, the expression of total current can be obtained by substituting Eqs. (4) and (5) into Eq. (49), the results are

$$\begin{aligned} i &= (\alpha_1\rho_1+\beta_1)\varphi_1+(-\alpha_2\rho_2+\beta_2)\varphi_2 \\ &= (\alpha_1-\alpha_2)\rho_{12}\varphi_{12}+(\beta_1+\beta_2)\varphi_{12}. \end{aligned} \tag{53}$$

By integrating both sides of Eq. (53) we have

$$q=\frac{1}{2}(\alpha_1-\alpha_2)\rho_{12}^2+(\beta_1+\beta_2)\rho_{12}. \tag{54}$$

Using Eqs. (54) and (3), the total meminductance of MLs in parallel connection with opposite polarities can be calculated as

$$L_{\mathrm{M12}}^{-1}(\rho)=\frac{\mathrm{d}q(\rho_{12})}{\mathrm{d}\rho_{12}}=(\alpha_1-\alpha_2)\rho_{12}+(\beta_1+\beta_2). \tag{55}$$

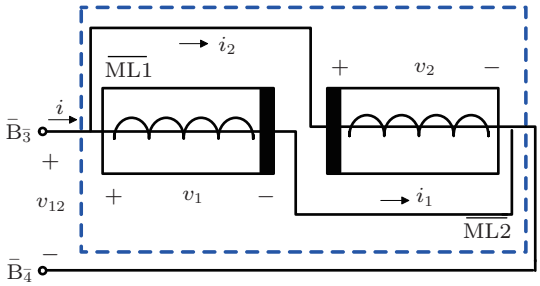


Fig. 5. (color online) MLs connected in parallel with opposite polarities.

For the further investigation of the dynamic of a parallel circuit, an additional inductor is considered in the connection. As shown in Fig. 4, the voltage v_{12} denotes the voltage imposed on terminals T and B2. The currents, voltages, and fluxes can be related correspondingly by

$$i=i_1+i_2,\quad v_{12}=v_l+v_1,\quad \varphi_{12}=\varphi_l+\varphi_1. \tag{56}$$

The composite inverse meminductance of two MLs connected in parallel is shown in Eq. (52). Taking into account that $i=\varphi/L$ and by considering Eq. (56), the relation of fluxes can be written as

$$L_0\varphi_1[(\alpha_1+\alpha_2)+\beta_1+\beta_2]+\varphi_1=\varphi_{12}. \tag{57}$$

By integrating both sides of Eq. (57), the following equation holds:

$$\frac{1}{2}L_0(\alpha_1+\alpha_2)\rho_1^2+R_{\mathrm{S}}(\beta_1+\beta_2)\rho_1+\rho_1=\rho_{12}. \tag{58}$$

Thus, the expression of ρ can be solved as

$$\rho_1 = \rho_2 = \frac{-[1+L_0(\beta_1+\beta_2)] + \sqrt{[1+L_0(\beta_1+\beta_2)]^2 + 2L_0(\alpha_1+\alpha_2)\rho_{12}}}{L_0(\alpha_1+\alpha_2)}. \tag{59}$$

The expression of the composite inverse meminductance can be obtained by substituting Eq. (59) into Eq. (52), namely

$$L_{\mathrm{M12}}^{-1}(\rho_{12}) = \frac{-1+\sqrt{[1+L_0(\beta_1+\beta_2)]^2 + 2L_0(\alpha_1+\alpha_2)\rho_{12}}}{L_0}. \tag{60}$$

5. Simulation analysis

In order to validate the theoretical analysis, by referring to a previously proposed ML emulator,[11] the PSPICE model of a single ML, which is then used to establish the dual MLs circuit, is shown in Fig. 6, where A and B are two ports for this element to connect in a circuit. Owing to the difficulty in capturing the values of charge in the practical circuit implementation using PSPICE and hardware, here, flux and current are chosen as two variables instead of ρ and q, which are also in good agreement with the constitutive relation of ML.

In this emulator circuit, $v_{\mathrm{ci}} = v_{\varphi}$, and v_{ci} is proportional to the time integral of current i_{ci} flowing out from terminal 5 of U1. Owing to the input–output characteristics of the circuit component AD844, the current flowing into terminal 2 is invariably conveyed to the output terminal 5. Besides, the voltages of terminals 2, 3, and 5 are the same. Thus, the voltage applied between terminals A and B is identical to the voltage across nodes C and D, namely, $v_{\mathrm{AB}} = v_{\mathrm{Ri}} = v_{\mathrm{ci}} = v_{\varphi}$. The equation of v_{ci} is

$$v_{\mathrm{ci}} = \frac{1}{R_{\mathrm{i}}C_{\mathrm{i}}}\int_{t_0}^{t} v_{\mathrm{AB}}\,\mathrm{d}\tau = \frac{1}{R_{\mathrm{i}}C_{\mathrm{i}}}\varphi. \tag{61}$$

Obviously, v_{ci} is proportional to flux φ, thus the value of v_{ci} can be used to represent that of φ. The flux can then be calculated as $\varphi = v_{\mathrm{ci}}R_{\mathrm{i}}C_{\mathrm{i}} = v_{\mathrm{ci}} \times 10^{-2}$.

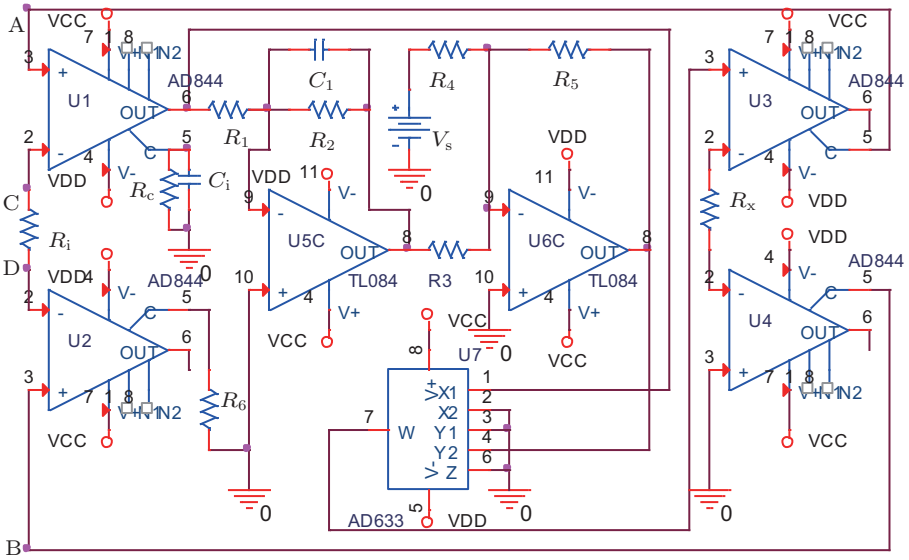


Fig. 6. (color online) Pspice model of a single ML.

Moreover, the output voltages of $U_{5\mathrm{C}}$ and $U_{6\mathrm{C}}$ can be expressed as

$$v_{\rho} = -\frac{1}{R_1C_1}\int_{t_0}^{t} v_{\varphi}\,\mathrm{d}\tau = -\frac{1}{R_1R_{\mathrm{i}}C_1C_{\mathrm{i}}}\rho, \tag{62}$$

$$v_{\mathrm{y2}} = -R_5\left(\frac{1}{R_3}v_{\rho} + \frac{1}{R_4}v_{\mathrm{s}}\right). \tag{63}$$

The value of inverse meminductance can be identified as

$$L_{\mathrm{M}}^{-1} = \frac{R_5}{10R_{\mathrm{i}}C_{\mathrm{i}}R_{\mathrm{x}}}\left(\frac{1}{R_3}\frac{1}{R_1R_{\mathrm{i}}C_1C_{\mathrm{i}}}\rho - \frac{1}{R_4}v_{\mathrm{s}}\right) = L_{\mathrm{M0}}^{-1} + \alpha\rho, \tag{64}$$

where

$$\alpha = \frac{R_5}{10R_3R_{\mathrm{x}}R_1R_{\mathrm{i}}^2C_1C_{\mathrm{i}}^2},$$

$$L_{\mathrm{M0}}^{-1} = \beta = -\frac{R_5}{10R_4R_{\mathrm{i}}C_{\mathrm{i}}R_{\mathrm{x}}}v_{\mathrm{s}}.$$

Note that the value of L_{M}^{-1} is in proportion to the voltage value v_{y2}. Hence, v_{y2} is captured to represent L_{M}^{-1} based on the relation of $L_{\mathrm{M}}^{-1} = v_{\mathrm{y2}}/10R_{\mathrm{i}}C_{\mathrm{i}}R_{\mathrm{x}} = 10^{-2}v_{\mathrm{y2}}$.

5.1. Serial connections

As is well known, mem-elements can store historic information, so the initial values of inverse meminductace for

two MLs are possibly different. In the simulation process, we set the initial inverse meminductance values of two MLs to be $\beta_1 = 0.09\ \mathrm{H}^{-1}$ and $\beta_2 = 0.05625\ \mathrm{H}^{-1}$. Meanwhile, the values of α_1 and α_2 are configured as $\alpha_1 = \alpha_2 = 235.29412$. As for the supply voltage v_{12}, we adopt a sinusoidal input signal $v_{12}(t) = 5.75\sin(73.8\pi t)$ to excite the dual ML circuit.

5.1.1. Serial ML circuit with identical polarities

As is well known, the flux, inductance, and current flowing through an inductor are related by $L = \varphi/i$. Figure 7 shows the relationships between current (i) and the equivalent flux corresponding to two individual MLs and the serial ML circuit (v_{ci1}, v_{ci2}, v_{ci12}). The slope of the curve can be used to represent the instant value of the composite meminductance value. It can be clearly seen that the two serial MLs and their composite ML possess meminductive characteristics with typical nonlinear pinched hysteresis loops behaving as an inclined "8", which differs from the behavior of a linear inductor. For the reason that the relation among L_{M12}, L_{M1}, and L_{M2} in serial connection can be described as $L_{M12} = L_{M1} + L_{M2}$, here, the value of the composite L_{M12} is larger than those of L_{M1} and L_{M2}. Thus the slope of the φ_{12}/i curve, which denotes the value of L_{M12}, is steeper than those denoting the values of L_{M1} and L_{M2} for any given current.

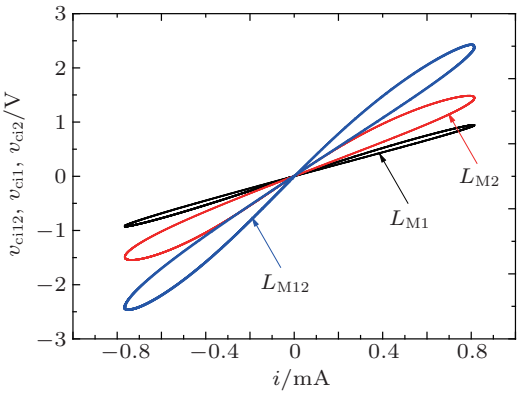


Fig. 7. (color online) Simulation results of pinched hysteresis loops for MLs connected in series with identical polarities.

Figure 8 shows the relationships between the equivalent flux and inverse meminductance corresponding to two individual MLs and the serial ML circuit (v_{ci1}, v_{ci2}, v_{ci12} and v_{y2-1}, v_{y2-2}, v_{y2-12}). It can be seen from Fig. 8(a) that there are two values of the equivalent inverse meminductance corresponding to each given flux. Evidently, the changing flux range of L_{M2} is wider than that of L_{M1}. The reason is that according to Eq.(7), the inverse meminductance value is related to the initial value L_{M0}^{-1}. As the initial value of β_1 is previously set to be larger than β_2, the initial absolute voltage value across ML1 is smaller than that across ML2. On the basis of Eq. (1), the range of flux for ML1 is smaller than that for ML2, and the instant value of L_{M1}^{-1} is always larger than that of L_{M2}^{-1}. The value of inverse meminductance is in proportion to the value of ρ, which is the integral of flux. As a result, the minimum and maximum inverse meminductance values of single ML do not occur with the same value of flux. This result is also applicable to L_{M2} and the composite L_{M12}.

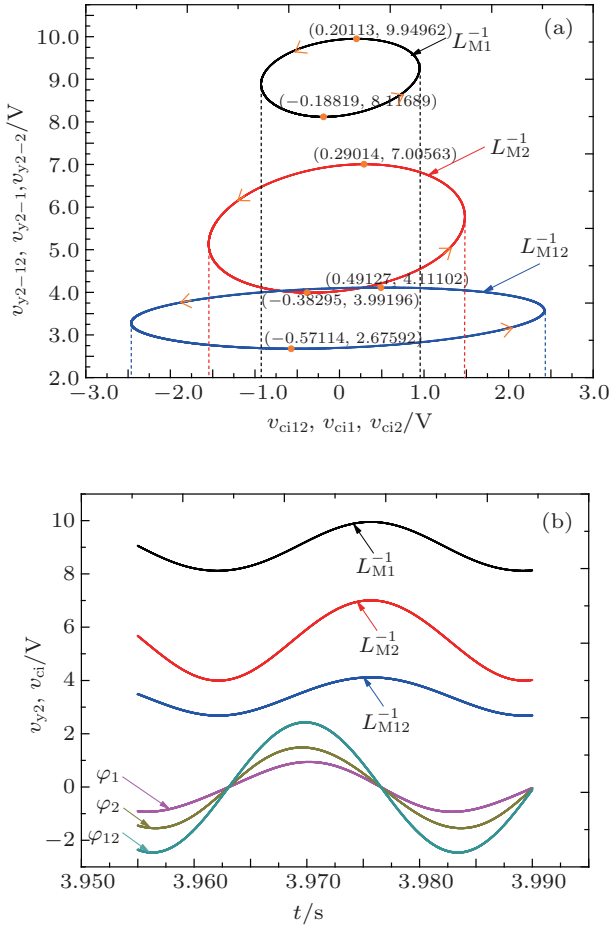


Fig. 8. (color online) Serial ML circuit with identical polarities. (a) Relation between inverse meminductance versus flux; (b) time-domain waveforms of equivalent inverse meminductance and flux.

Figure 8(b) displays the time-dependent curves of values of equivalent inverse ML and fluxes of this dual ML circuit. Nevertheless, due to the nonlinearity of ML, the flux curves of MLs are no longer sinusoidal waves. These curves imply that the inverse meminductance value of the composite ML is smaller than those of individual MLs, but these three curves approach to their maximum and minimum values simultaneously. This is because two MLs are connected in series with identical polarities, the currents going through each ML are identical. In consequence, as the meminductance of M1 increases, the meminductance of M2 increases, and as the meminductance of M1 decreases, the meminductance of M2 decreases as well.

Figure 8 suggests that corresponding to the alternating input voltage v_{12}, equivalent L_{M1}^{-1}, L_{M2}^{-1}, and L_{M12}^{-1} vary periodically along the anticlockwise direction as indicated with arrows in Fig. 8(a).

Figure 9 illustrates the variations of the minimum and the maximum equivalent inverse meminductance ($v_{y2,max}$ and $v_{y2,min}$) and the corresponding fluxes φ for each ML and the composite ML with supply voltage amplitude in a range from 1.75 V to 5.75 V in steps of 0.2 V. In Fig. 9(a), when the supply voltage amplitude increases, the maximum values of L_{M1}^{-1}, L_{M2}^{-1}, and L_{M12}^{-1} increase and their minimum values decrease. At the same time, from Fig. 9(b), we can see that when the equivalent inverse meminductance value of each ML reaches its minimum value, the corresponding flux of each ML increases with the increase of the input voltage amplitude. Contrarily, when the equivalent inverse meminductance value of each ML reaches its maximum value, the corresponding flux of each ML increases, accompanied with the increase of ρ of each single ML, according to Eq. (1). In view of Eqs. (8) and (9), the maximum inverse meminductance value of each ML increases and the minimum inverse meminductance value decreases. Owing to the relations between composite and individual flux and ρ presented in Eqs. (12) and (13), with the increase of supply voltage amplitude, the composite flux and ρ of composite ML increase when L_{M12}^{-1} reaches its maximum value, and decrease when L_{M12}^{-1} reaches its minimum value.

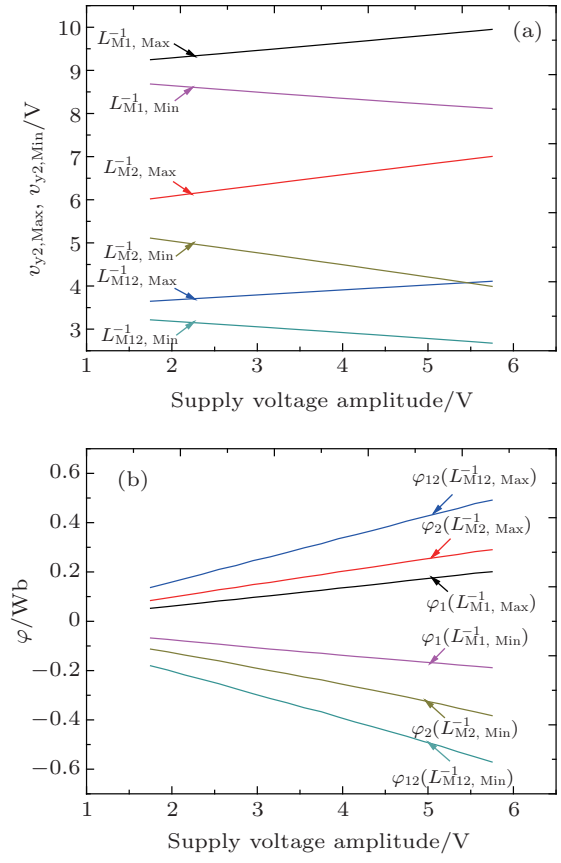


Fig. 9. (color online) (a) Minimum and maximum values of equivalent inverse meminductance $v_{y2,Max}$ and $v_{y2,Min}$ and (b) corresponding fluxes φ for each ML and the composite ML versus supply voltage amplitude in a range from 1.75 V to 5.75 V.

5.1.2. Serial ML circuit with opposite polarities

For the connection scenario with opposite polarities, figure 10 presents the curves of current versus fluxes in terms of two individual MLs and the composite ML. Like the case of identical polarities, these two serial MLs also behave together as a new ML with a typical pinched hysteresis loop. According to Eq. (29), the coefficient of ρ for ML2 is a negative value in the opposite connected series, so the curves are slightly different from those in the connection scenario with identical polarities.

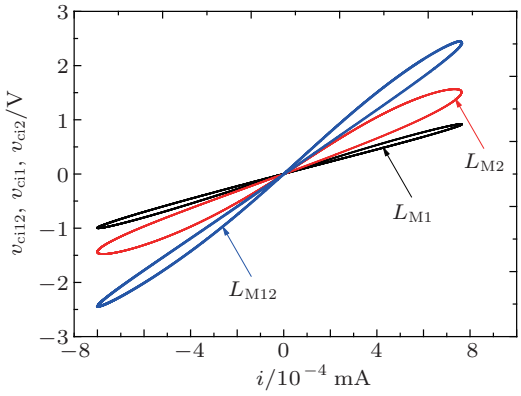


Fig. 10. (color online) Simulation results of pinched hysteresis loops for MLs connected in series with opposite polarities.

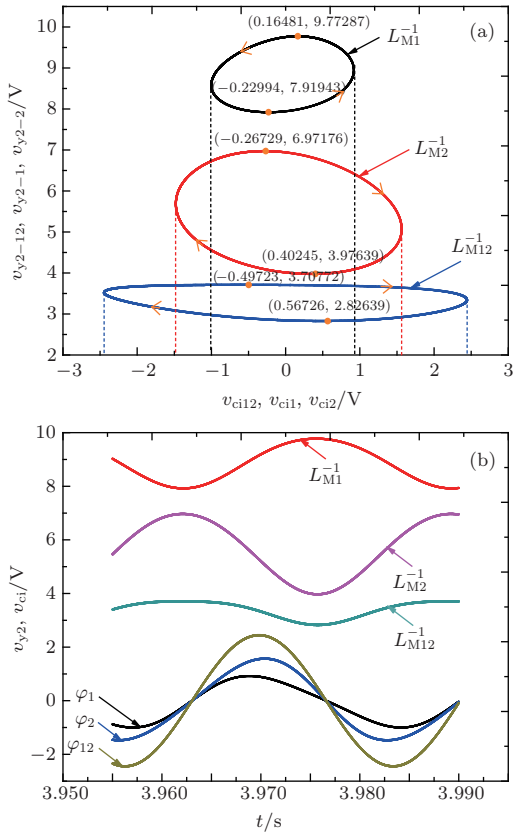


Fig. 11. (color online) Serial ML circuit with opposite polarities. (a) Equivalent inverse meminductance versus flux relation, (b) time-dependent waveforms of equivalent inverse meminductance and flux.

Figure 11 shows the equivalent inverse meminductance, the flux values of each ML, and the composite ML of serially connected MLs with opposite polarities. It can be concluded from Fig. 11(b) that when the curve of L_{M1}^{-1} arrives at its maximum value, the curves of L_{M2}^{-1} and L_{M12}^{-1} simultaneously reach their minimum values, since identical currents flow through both MLs. In consequence, as the meminductance of M1 increases, the meminductance of M2 increases, and as the meminductance of M1 decreases, the meminductance of M2 increases. According to Eq. (7), the inverse meminductance value is related to the initial value L_{M0}^{-1}. The initial value of β_1 is set to be larger than β_2, thus the initial absolute voltage value across ML1 is smaller than that across ML2. On the basis of Eqs. (1) and (29), the range of flux for ML1 is smaller than that for ML2, thus the variance of L_{M12}^{-1} keeps the same pace with L_{M2}^{-1}.

It can be concluded from Fig. 11 that corresponding to the alternating voltage V_{12}, equivalent L_{M1}^{-1}, L_{M2}^{-1}, and L_{M12}^{-1} all vary periodically, while equivalent L_{M1}^{-1} evolves along the anticlockwise direction and equivalent L_{M2}^{-1} and L_{M12}^{-1} alters along the clockwise direction, as indicated with the arrows in Fig. 11.

Figure 12 illustrates the variations of the minimum and maximum equivalent inverse meminductance and corresponding fluxes for each ML and the composite ML with supply voltage amplitude in the range from 1.75 V to 5.75 V in steps of 0.2 V. From these curves, we can see that with the increase of the supply voltage amplitude, the maximum values of L_{M1}^{-1}, L_{M2}^{-1}, and L_{M12}^{-1} increase, and the minimum values of L_{M1}^{-1}, L_{M2}^{-1}, and L_{M12}^{-1} decrease. When ML1 reaches its maximal inverse meminductance, ML2 and the composite ML reach their minimal inverse meminductance values, and with the increase of input voltage amplitude, the corresponding flux of each ML increases gradually. Contrarily, when ML1 reaches its minimal inverse meminductance, ML2 and the composite ML reach their maximal inverse meminductance values, and with the increase of input voltage amplitude, the corresponding flux of each ML decreases gradually.

5.1.3. Dual serially connected MLs with identical polarities and a serial inductor

In this case, an inductor of inductance equal to 0.035 H is serially attached to this serial MLs' circuit with identical polarities. In Fig. 14, by only collecting the values of inverse meminductance of two MLs and their corresponding fluxes, we discover that the relation between them leads to a conspicuous conclusion that these two MLs in serial connection also behave like a single ML. That result also validates the good floating performance of this ML based circuit, which renders this composite circuit a wider range of use without grounded restriction.

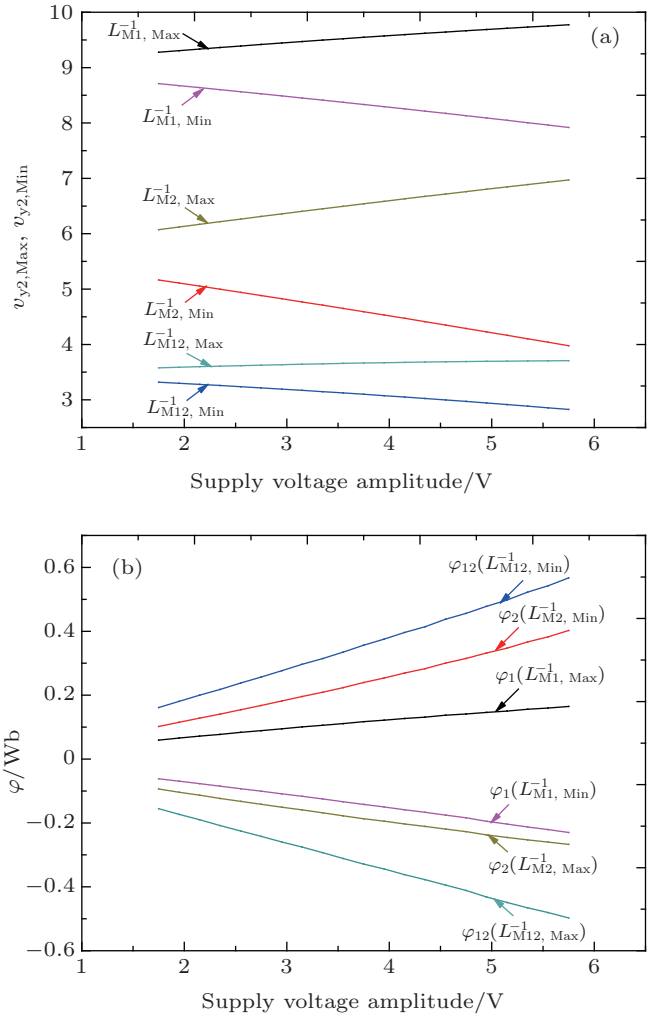


Fig. 12. (color online) Variations of (a) minimum and maximum values of equivalent inverse meminductance and (b) corresponding fluxes for each ML and the composite ML with supply voltage amplitude in the range from 1.75 V to 5.75 V.

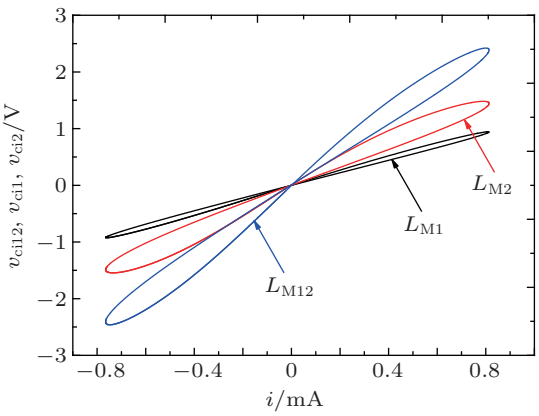


Fig. 13. (color online) Simulation results of pinched hysteresis loops for MLs connected in parallel with identical polarities and with another inductor.

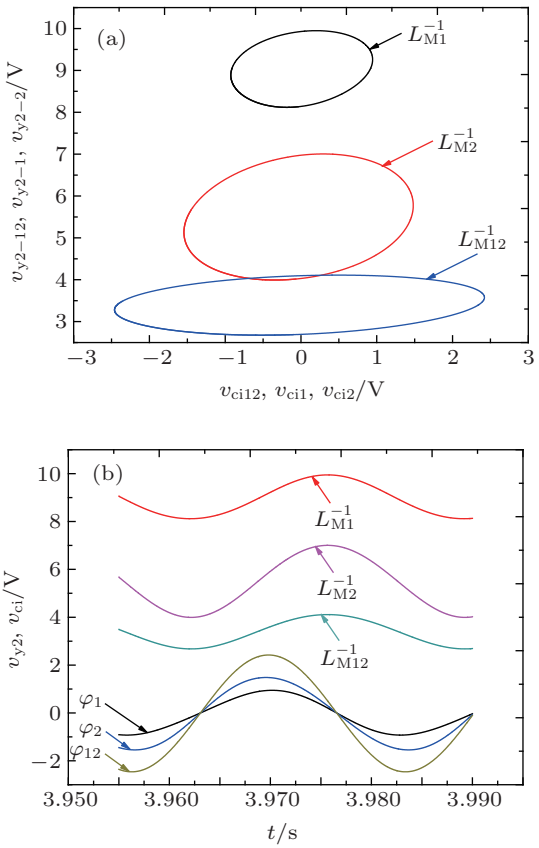


Fig. 14. (color online) Serial ML circuit with identical polarities connected with an additional inductor. (a) Equivalent inverse meminductance versus flux relation, (b) time-dependent waveforms of equivalent inverse meminductance and flux.

5.2. Parallel connections

First, we adopt two scenarios of parameter α to describe the dual MLs in parallel connection, namely, $\alpha_1 = \alpha_2$ (equal to 235.29412) and $\alpha_1 \neq \alpha_2$ ($\alpha_1 = 120$ and $\alpha_2 = 235.29412$). The other parameters are $\beta_1 = 0.09\ \mathrm{H}^{-1}$, $\beta_2 = 0.05625\ \mathrm{H}^{-1}$, and $v_{12}(t) = 5.75\sin(73.8\pi t)$.

5.2.1. Parallel ML circuit with identical polarities

Figure 15 shows the relationships between current and fluxes of two individual MLs and the composite parallel ML circuit, so the slopes of these curves can be used to represent the instant values of equivalent inverse meminductance due to the relation among flux, inductance, and current as $L = \varphi/i$. These curves imply that two parallel MLs and their composite ML also possess meminductive characteristics with typical nonlinear pinched hysteresis loops behaving as an inclined "8". According to Eq. (52), the composite meminductance value is smaller than any of the single meminductance values. Thus, the slope of L_{M12} for a given current is slighter than those of L_{M1} and L_{M2}.

The cases of $\alpha_1 = \alpha_2$ and $\alpha_1 \neq \alpha_2$ for ML circuit connected in parallel with identical polarities are both analyzed. Firstly, coefficient α for two MLs is configured as $\alpha_1 = \alpha_2 = 235.29412$, and the initial values of the inverse meminductance L_{M1}^{-1} and L_{M2}^{-1} are set to be $\beta_1 = 0.09\ \mathrm{H}^{-1}$ and $\beta_2 = 0.05625\ \mathrm{H}^{-1}$, respectively. Figure 16 shows the relations between currents flowing through MLs and the corresponding values of equivalent inverse meminductance under these circumstances. We can discover from Fig. 16(a) that the shapes of curves for ML1 and ML1 are in high similarity.

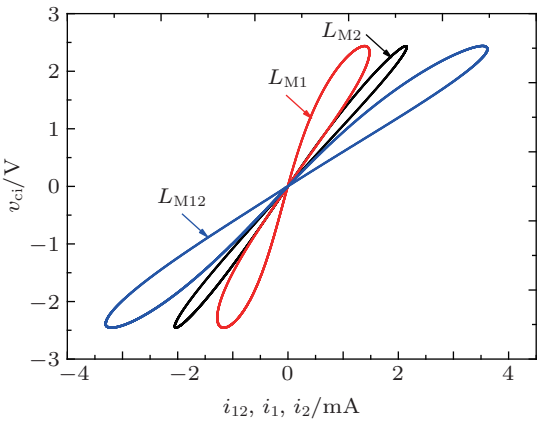


Fig. 15. (color online) Simulation results of pinched hysteresis loops for MLs connected in parallel with identical polarities.

The value of inverse meminductance is in proportion to the value of ρ as described by Eq. (1). For inductors and MLs, the phase difference between voltage and current is $\pi/2$, and the current lags $\pi/2$ behind the terminal voltage. As a result, the minimum and maximum inverse meminductance values of single ML1, ML2, and ML12 do not occur with the same value of current. If we set different values of coefficient α for two MLs, to be $\alpha_1 = 120$ and $\alpha_2 = 235.29412$, there are only slight differences between the maximum and minimum of two ML1 curves. In the following analysis, only the latter scenario of $\alpha_1 \neq \alpha_2$ is taken for demonstration.

We can see from Fig. 16(b) that there are two values of the inverse meminductance corresponding to any current, except for the minimum and maximum values. However, due to the nonlinearity of the ML, the maximum and minimum absolute values of current flowing through ML1 and ML2 are different. Evidently, the variation range of current of ML1 is wider than that of ML2. The reason is that in a parallel ML circuit with identical polarities, each single ML has the same terminal voltage. As a result, according to Eq. (1), flux and ρ for each single ML are the same. As $\beta_1 > \beta_2$, the value of L_{M0-1}^{-1} is set to be larger than that of L_{M0-2}^{-1}, where L_{M0-1}^{-1} and L_{M0-2}^{-1} denote the initial inverse values of inverse meminductance of ML1 and ML2, respectively. Though from Eqs. (8) and (9) we can see that the value of inverse meminductance is related to α and $\alpha_1 < \alpha_2$, the inverse meminductance value of ML1 here is still larger than that of ML1, because α_2 is not large enough. Thus the value of L_{M1} is always smaller than that of L_{M2}. According to $\varphi = Li$, the absolute value of current flowing through ML1 is larger than that through ML2, which can also be shown in Fig. 16(c).

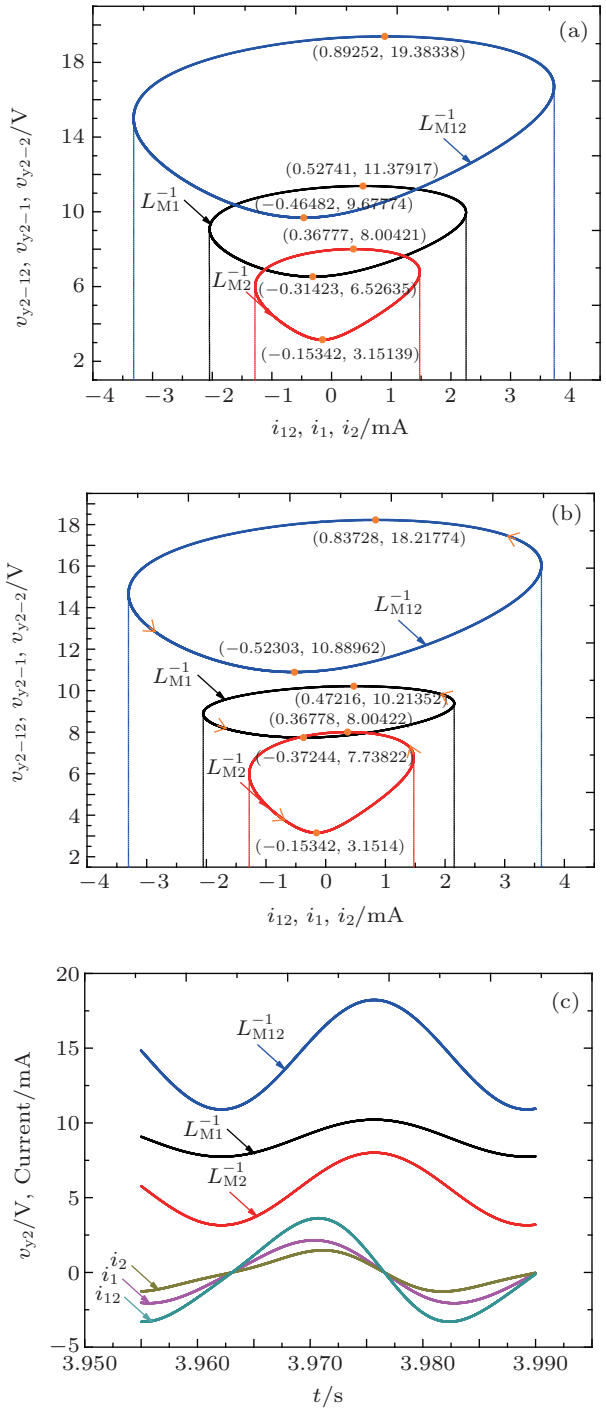


Fig. 16. (color online) Parallel ML circuit with identical polarities: equivalent inverse meminductance versus current relation (a) $\alpha_1 = \alpha_2$; (b) $\alpha_1 \neq \alpha_2$; (c) time-domain waveforms of equivalent inverse meminductance and current.

From Fig. 16(c), we can discover that the equivalent inverse meminductance values of ML1, ML2, and ML12 vary simultaneously in the same time steps, namely, they reach their maximum and minimum values at the same time. Meantime, the value of the instant inverse meminductance of L_{M1}^{-1} is always larger than that of L_{M2}^{-1}. Additionally, the currents i_1, i_2, and i_{12} simultaneously cross zero. It is worth noting that when a sinusoidal input signal is adopted for exciting this parallel ML circuit, the wave of current flowing through each ML is no longer sinusoidal due to the nonlinearity of ML.

By combining Fig. 16(b) with Fig. 16(c), we can conclude that corresponding to the alternating input voltage V_{12} , equivalent L_{M1}^{-1}, L_{M2}^{-1}, and L_{M12}^{-1} vary periodically well, which are all in the anticlockwise direction as indicated with arrows in Fig. 16(b).

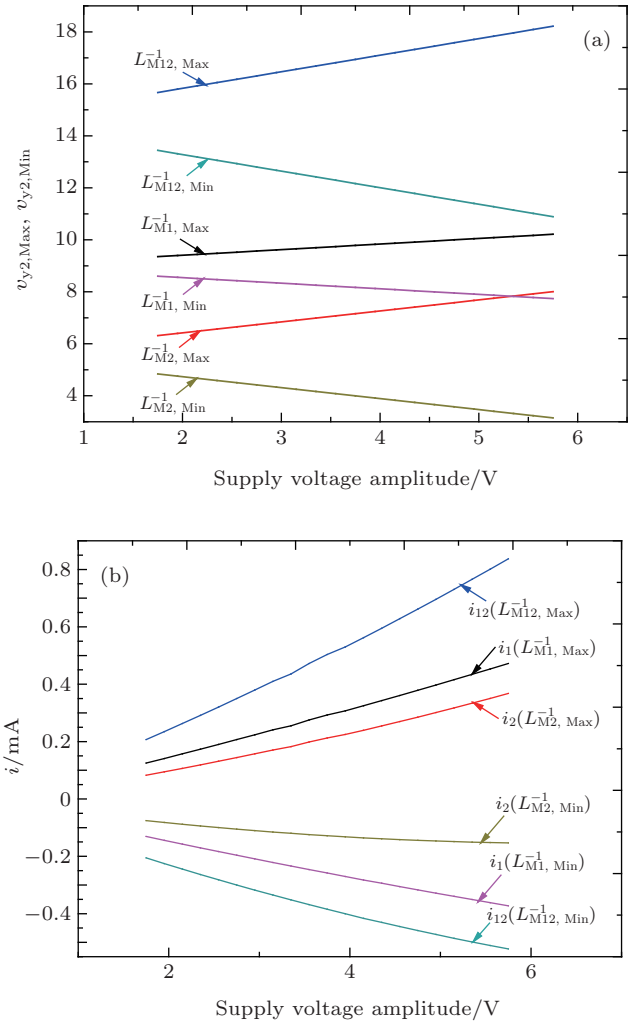


Fig. 17. (color online) Variations of (a) the minimum and maximum values of equivalent inverse meminductance and (b) corresponding currents for each ML and the composite ML with supply voltage amplitude.

Figures 17(a) and 17(b) illustrate the variations of the minimum and maximum equivalent inverse meminductance and corresponding currents for each ML and the composite ML with the supply voltage amplitude in a range from 1.75 V to 5.75 V, in steps of 0.2 V. We can find from Fig. 17(a) that with the increase of the supply voltage amplitude, the maximum values of L_{M1}^{-1}, L_{M2}^{-1}, and L_{M12}^{-1} increased and their minimum values decreased. At the same time, Fig. 17(b) illustrates that when the equivalent inverse meminductance values reach their maximum values, the corresponding current flowing through each ML and the total current i_{12} increase with the increase of input voltage amplitude. On the contrary, when the equivalent inverse meminductance values reach their minimum values, the corresponding current flowing through each

ML and the total current i_{12} decrease. This result can be explained by Eq. (1) as follows: as the terminal voltage across each ML and i_{12} increase, the values of flux and ρ increase. Accordingly, the values of inverse meminductance increase. Since $\varphi = Li$, the increase of current flowing through each ML will lead to the increase of composite current.

5.2.2. Parallel ML circuit with opposite polarities

Figure 18 shows the relationships between current and flux of two individual MLs and the composite ML with opposite polarities. Like the case of MLs connected in parallel with identical polarities, these two MLs in parallel connection also together behave as a new ML with a typical pinched hysteresis loop. Compared with that in Fig. 15, the variation range of inverse meminductance of the composite ML is smaller than that in the identical scenario.

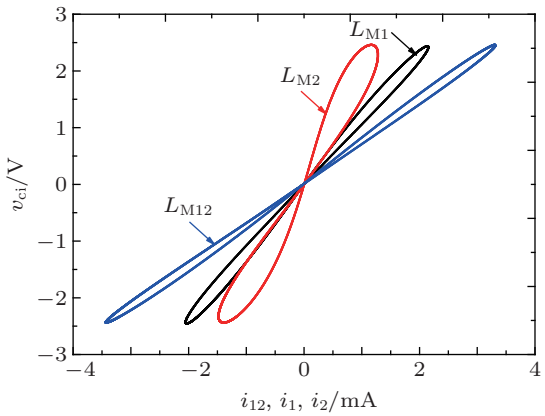


Fig. 18. (color online) Simulation results of pinched hysteresis loops for MLs connected in series with opposite polarities.

Two cases of $\alpha_1 = \alpha_2$ and $\alpha_1 \neq \alpha_2$ are also adopted for analyzing this parallel ML circuit with opposite polarities. Firstly, we set $\alpha_1 = \alpha_2 = 235.29412$, and the initial values of the inverse meminductance L_{M1}^{-1} and L_{M2}^{-1} to be $\beta_1 = 0.09$ H^{-1} and $\beta_2 = 0.05625$ H^{-1}, respectively. Figure 19 shows the relations between currents flowing through MLs, and corresponding values of their equivalent inverse meminductance under these circumstances. We find that the equivalent composite meminductance value becomes constant and does not vary with current. This is because the sum of two variables ρ_1 and ρ_2 with their coefficient α_1 and $(-\alpha_2)$ always stay at zero. Thus the value of composite inverse meminductance is always $\beta_1 + \beta_2$. If we set coefficient α differently, say, $\alpha_1 = 120$ and $\alpha_2 = 235.29412$, the inverse meminductance value will vary with composite current i_{12}. In the following analysis, only the latter scenario of $\alpha_1 \neq \alpha_2$ is taken for demonstration.

Note that compared with that in Fig. 16(b), the variation range of inverse meminductance of the composite ML is smaller than that in the identical polarity scenario. From Fig. 19(c), we find that equivalent inverse meminductance values of ML1, ML2, and ML12 simultaneously vary, reaching their maximal or minimal values at the same time. However, unlike the identical polarity scenario, the value of the instant inverse meminductance L_{M1}^{-1} is not always larger than L_{M2}^{-1}. A single variation period of inverse meminductance in the time interval (3.96047, 3.98757) s is taken as an example.

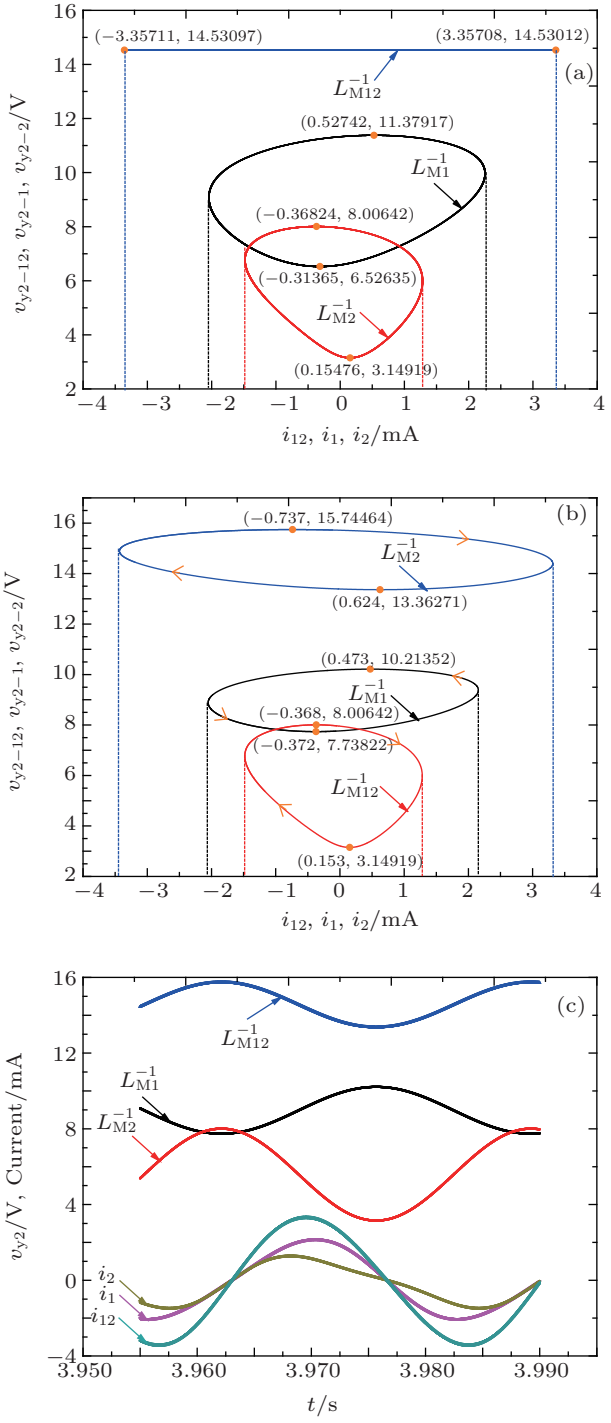


Fig. 19. (color online) Parallel ML circuit with opposite polarities: equivalent inverse meminductance versus current relation (a) when $\alpha_1 = \alpha_2$; (b) when $\alpha_1 \neq \alpha_2$; (c) time-dependent waveforms of equivalent inverse meminductance and current.

L_{M2}^{-1} is larger than L_{M1}^{-1} in the time interval (3.96047, 3.96382) s and smaller than L_{M1}^{-1} in the time interval (3.96382, 3.98757) s. This is because ML1 and ML2 are connected in parallel with opposite polarities, so the inverse meminductance values of two MLs change in the inverse direction with current. When the value of L_{M1}^{-1} increases, the value of L_{M2}^{-1} decreases. Thus, there is a possibility for the value of L_{M1}^{-1} to be smaller than that of L_{M2}^{-1}. In Eq. (55), if $\alpha_1 < \alpha_2$, the coefficient of ρ, namely, $(\alpha_1 - \alpha_2)$ for the composite inverse meminductance will have the same sign as $(-\alpha_2)$ so the changed direction of composite meminductance is the same as that of ML2.

The combination of Figs. 19(b) and 19(c) suggests that corresponding to the alternating current i_{12}, equivalent L_{M1}^{-1}, L_{M2}^{-1}, and L_{M12}^{-1} all vary in periodicity, while equivalent L_{M1}^{-1} changes in the anticlockwise direction and equivalent L_{M2}^{-1} and L_{M12}^{-1} evolve in the clockwise direction, as indicated with arrows in Fig. 19(b).

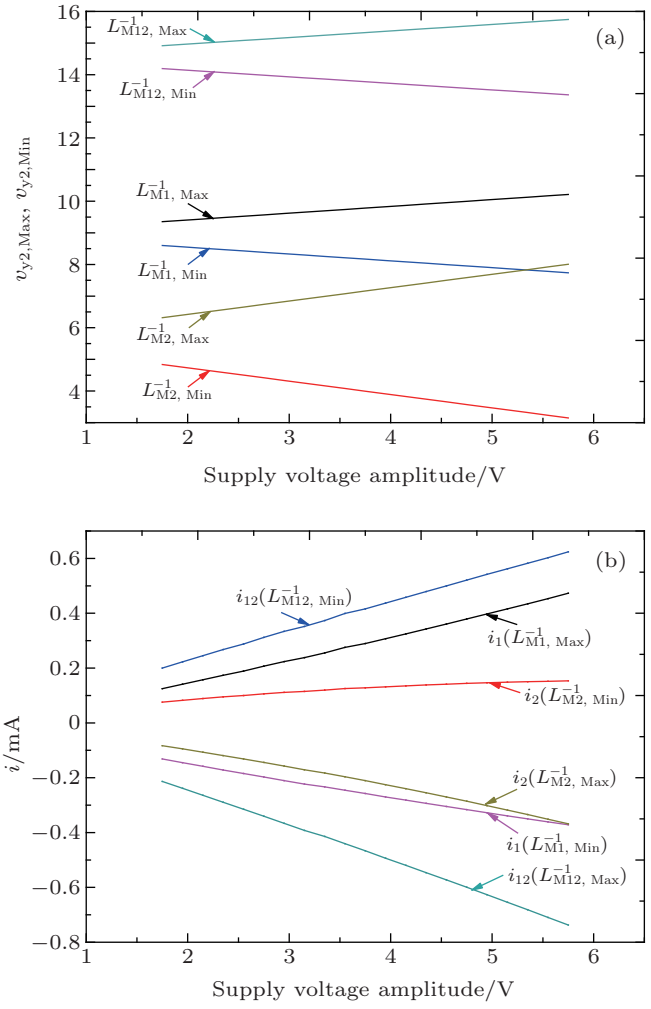


Fig. 20. (color online) Variations of (a) the minimum and maximum values of equivalent inverse meminductance and (b) corresponding currents for each ML and the composite ML with supply voltage amplitude in the range from 1.75 V to 5.75 V.

Figures 20(a) and 20(b) illustrate the variations of the minimum and maximum equivalent inverse meminductance and corresponding currents for MLs with supply voltage amplitude in the range from 1.75 V to 5.75 V, in steps of 0.2 V. From Fig. 20(a) we can find that with the increase of supply voltage amplitude, the maximum values of L_{M1}^{-1}, L_{M2}^{-1}, and L_{M12}^{-1} increase, while their minimum values decrease. As previously mentioned, from Fig. 20(b) we can see that the changing trend of inverse meminductance of ML1 is opposite to those of ML2 and ML12, thus when the equivalent inverse meminductance value of ML1 reaches its maximum value and the equivalent inverse meminductance values of ML2 and ML12 reach their minimum values, the corresponding currents flowing through ML1 and ML2 and the total current increase with the increase of input voltage amplitude. On the contrary, when the equivalent inverse meminductance value of ML1 reaches its minimum value and the equivalent inverse meminductance values of ML2 and ML12 reach their maximum values, the corresponding currents flowing through ML1 and ML2 and the total current decrease with the increase of input voltage amplitude.

5.2.3. Dual MLs in parallel connection with identical polarities and a serial inductor

In this case, an inductor with an inductance of 0.125 H is serially attached to the ML in parallel connection with identical polarities. In Figs. 21 and 22, we also collect the values of inverse meminductance of two MLs and their corresponding currents, and then find that these two MLs in parallel connection, as connected with an inductor, also behave like one single floating ML.

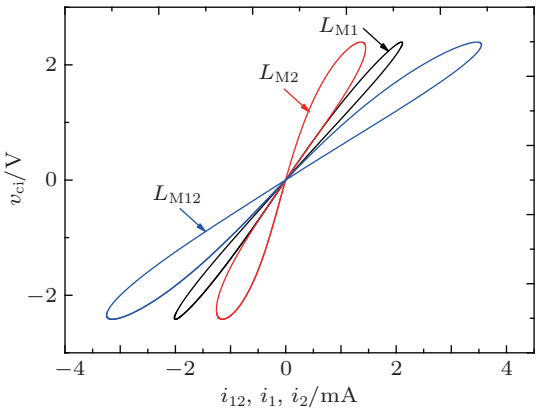


Fig. 21. (color online) Simulation results of pinched hysteresis loops for MLs connected in parallel with opposite polarities and with another inductor.

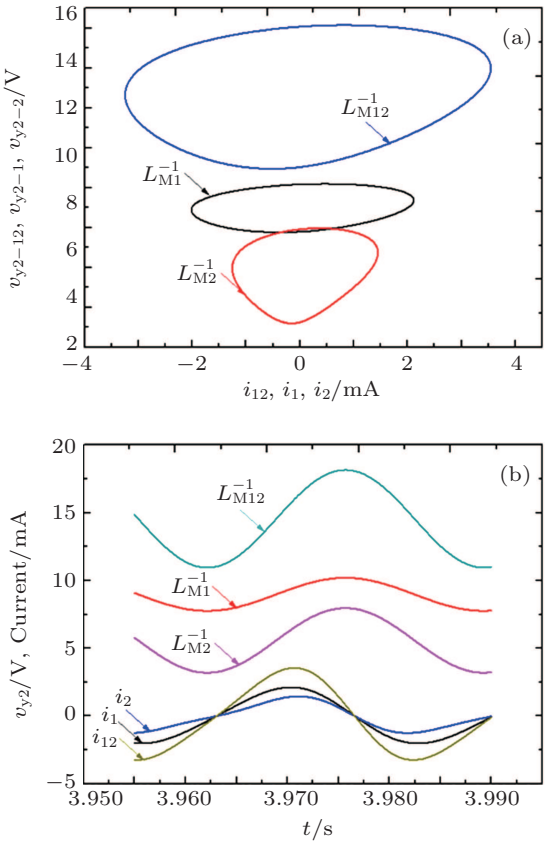


Fig. 22. (color online) Parallel ML circuit with identical polarities connected with an additional inductor. (a) Equivalent inverse meminductance versus current relation, (b) time-dependent waveforms of equivalent inverse meminductance and current.

6. Experimental verification

A hardware circuit which can emulate dual MLs is built to validate the correctness of theoretical analysis and simulation results. The experimental data are sampled by an oscilloscope TDS2024C and then processed in the OriginPro 9.0 software to draw experimental curves.

6.1. Design of dual MLs circuits

It can be seen from Fig. 6 that four transimpedance operational amplifiers (AD844), two amplifiers (TL084), and one multiplier (AD633) are used to constitute one single ML. As shown in Fig. 23, the circuit enclosed by the upper dotted frame can work as an individual ML emulator (denoted as ML1). Similarly, the circuit enclosed in the lower dotted frame can also work as an individual ML (denoted as ML2). The values of inverse meminductance for each ML can be adjusted via parameters as illustrated in Eq. (64). Experimental results under different circuit configurations can be reached by connecting two MLs together in terms of two polarities. For example, as terminals A and D, B and C are connected together, these two MLs are in parallel connection with opposite polarities.

By considering Eqs. (61), (63), and (64), flux φ and inverse meminductance L_{M}^{-1} can be represented by v_{ci} and v_{y2}, respectively. Furthermore, due to the action of AD844, the current flowing through each ML can be represented by the inverse value of voltage across R_{x}, namely, $-v_{\mathrm{rx}}$.

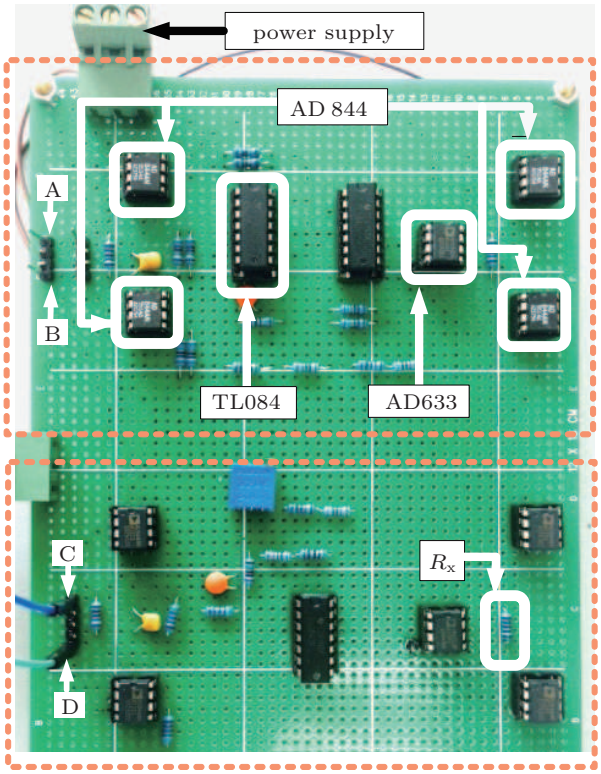


Fig. 23. (color online) Hardware circuit connection of dual ML emulators.

6.2. Experimental analysis

The scenarios of MLs in serial connection with identical polarities and parallel connection with opposite polarities are taken for demonstration.

To begin with, the experimental parameters for MLs in serial connection with identical polarities are given as follows: $R_{\mathrm{i1}} = R_{\mathrm{i2}} = 10$ kΩ, $R_{\mathrm{c1}} = R_{\mathrm{c2}} = 51$ kΩ, $C_{\mathrm{i1}} = C_{\mathrm{i2}} = 1$ u, $C_{11} = C_{12} = 0.1$ u, $R_{11} = R_{12} = 51$ kΩ, $R_{21} = R_{22} = 200$ kΩ, $R_{31} = R_{32} = 25$ kΩ, $R_{41} = 50$ kΩ, $R_{42} = 80$ kΩ, $R_{51} = R_{52} = 30$ kΩ, $R_{61} = R_{62} = 51$ kΩ, $R_{x1} = R_{x2} = 1$ kΩ, $v_{\mathrm{s1}} = v_{\mathrm{s2}} = -15$ V. Based on these parameters, the initial values of inverse meminductance of two MLs are calculated to be $\beta_1 = 0.09$ H^{-1} and $\beta_2 = 0.05625$ H^{-1}. Meanwhile, the values of α_1 and α_2 are configured as $\alpha_1 = \alpha_2 = 235.29412$. As for the supply voltage v_{12}, it can be described by a 36.9 Hz sinusoidal function with 5.75 V amplitude. Experimental data of equivalent flux and inverse meminductance for serial ML circuit with identical polarities are collected and shown in Fig. 24. Obviously, the experimental loops are in close proximity to the simulated results in Fig. 8.

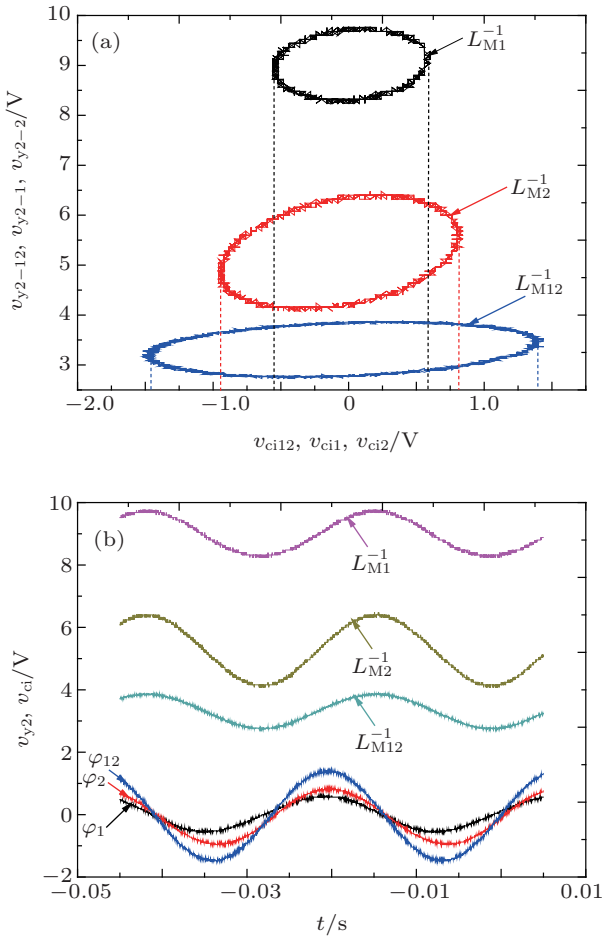


Fig. 24. (color online) Measured curves of serial ML circuit with identical polarities: (a) relation between inverse meminductance versus flux; (b) time-dependent waveforms of equivalent inverse meminductance and flux.

The parameters for experimentally testing MLs in parallel connection with opposite polarities are then configured as follows: $R_{i1} = R_{i2} = 10$ kΩ, $R_{c1} = R_{c2} = 51$ kΩ, $C_{i1} = C_{i2} = 1$ u, $C_{11} = C_{12} = 0.1$ u, $R_{11} = 100$ kΩ, $R_{12} = 51$ kΩ, $R_{21} = R_{22} = 200$ kΩ, $R_{31} = R_{32} = 25$ kΩ, $R_{41} = 50$ kΩ, $R_{42} = 80$ kΩ, $R_{51} = R_{52} = 30$ kΩ, $R_{61} = R_{62} = 51$ kΩ, $R_{x1} = R_{x2} = 1$ kΩ, $v_{s1} = v_{s2} = -15$ V. Thus, the parameters in Eqs. (8) and (9) are configured as $\beta_1 = 0.09$ H^{-1}, $\beta_2 = 0.05625$ H^{-1}, $\alpha_1 = 120$, and $\alpha_2 = 235.29412$. The supply voltage v_{12} is described by $v_{12}(t) = 5.75\sin(73.8\pi t)$. Experimental data of equivalent current and inverse meminductance for parallel ML circuit with opposite polarities are gathered and plotted in Fig. 25, which is highly consistent with the preceding waveform in Fig. 19.

However, there remain some minimal errors between simulated results and experimental measured results. For example, the time-domain curve of L_{M1}^{-1} intersects that of L_{M2}^{-1} in Fig. 19(c), but not in Fig. 25(b). In addition, flux values in Fig. 24(b) will not always cross zero simultaneously, which is slightly different from those in Fig. 8(b). These errors can mainly be attributed to the inaccuracy of circuit elements. Besides, two high-value resistors R_c and R_2 in parallel with the integral capacitors C_i and C_1 are introduced in order to minimize the DC offsets. This common practice can also lead to these practically emulating errors. However, this experimental mismatch is comparatively small and can also be reduced by optimizing the emulator parameters. The experimental results reveal that the proposed emulator is applicable for investigating the dynamic behaviors of MLs.

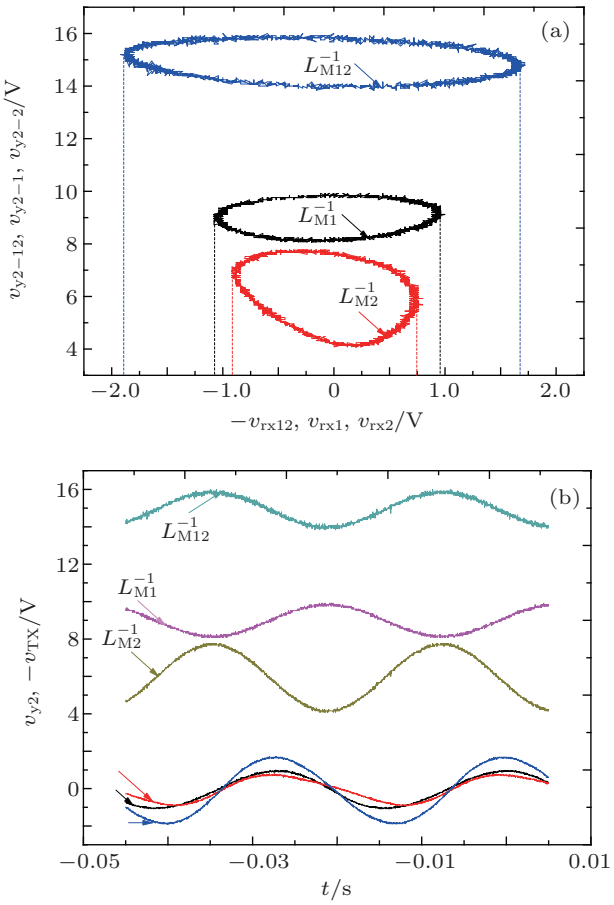


Fig. 25. (color online) Measured curves of a parallel ML circuit with opposite polarities: (a) equivalent inverse meminductance versus current relation, and (b) time-dependent waveforms of equivalent inverse meminductance and current.

7. Conclusions

In this paper, the composite behaviors of serial and parallel ML circuits with different polarities are theoretically analyzed, then simulated based on PSPICE, and finally characterized by the hardware circuit. The simulation and hardware results are in good accordance with the theoretical analysis. Despite the connection properties, the composite ML also acts like another time-integral-of-flux controlled ML with new meminductance, and different connections in terms of topologies and polarities can finally lead to various kinds of inverse meminductance values. Additionally, the floating performance of the composite ML circuit is also validated, which renders the circuit of composite dual MLs a wider scope of application without grounded restriction. The above characteristics provide unique approaches for MLs to be utilized in circuit

designs. The main contribution of this work is that it provides some practicable conclusions about composite MLs connections and the analyzing method can be extended to multiple MLs connection and be instructive to subsequent research work on the potential applications of ML.

References

[1] Chua L O 1971 *IEEE Trans. Circ. Theory* **18** 507
[2] Chua L O and Kang S M 1976 *Proc. IEEE* **64** 209
[3] Strukov D B, Snider G S, Stewart D R and Williams R S 2008 *Nature* **453** 80
[4] Di Ventra M, Pershin Y V and Chua L O 2009 *Proc. IEEE* **97** 1717
[5] Biolek D, Biolek Z and Biolkova V 2011 *Electron. Lett.* **47** 1385
[6] Liang Y, Yu D S and Chen H 2013 *Acta. Phys. Sin.* **62** 158501 (in Chinese)
[7] Sah M P, Budhathoki R K and Yang C J 2014 *J. Semicond. Technol. Sci.* **14** 750
[8] Li Z J, Zeng Y C and Tan Z P 2014 *Acta. Phys. Sin.* **63** 098501 (in Chinese)
[9] Pershin Y V and Di Ventra M 2011 *Electron. Lett.* **47** 243
[10] Yu D S, Liang Y and Iu H H C 2014 *Chin. Phys. B* **23** 070702
[11] Liang Y, Chen H and Yu D S 2014 *IEEE Trans. Circuits and Syst. II, Exp. Briefs* **61** 299
[12] Riaza R 2013 *IEEE Trans. Circuits Syst. I, Reg. Papers* **60** 1570
[13] Fouda M E and Radwan A G 2014 *Circ. Syst. Signal. Pr.* **33** 1573
[14] Fouda M E and Radwan A G 2014 *Microelectron. J.* **45** 1372
[15] Budhathoki R K, Sah M P, Adhikari S P, Kim H and Chua L O 2013 *IEEE Trans. Circ. Syst. I, Reg. Papers* **60** 2688
[16] Bao B C, Feng F, Dong W and Pan S H 2013 *Chin. Phys. B* **22** 068401
[17] Yu D S, Iu H H C, Liang Y, Fernando T and Chua L O 2015 *IEEE Trans. Circuits and Syst. I, Reg. Papers* **62** 1607
[18] Driscoll T, Quinn J, Klein S, Kim H T, Kim B J, Pershin Y V, Di Ventra M and Basov D N 2010 *Appl. Phys. Lett.* **97** 093502
[19] Hu Z H, Li Y X, Jia L and Yu J B 2010 *Proc. IEEE ICCCAS*, July 28–30, 2010, Chengdu, China, p. 820
[20] Pershin Y V and Di Ventra M 2012 *Proc. IEEE* **100** 2071
[21] Di Ventra M and Pershin Y V 2012 *International Workshop on Cellular Nanoscale Networks and their Applications*, August 29–31, 2012, Turin, Italy
[22] Bao B C, Hu F W, Liu Z and Xu J P 2015 *Chin. Phys. B* **23** 070503