A threshold voltage model of short-channel fully-depleted recessed-source/drain (Re-S/D) SOI MOSFETs with high-*k* dielectric*

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In this paper, a surface potential based threshold voltage model of fully-depleted (FD) recessed-source/drain (Re-S/D) silicon-on-insulator (SOI) metal-oxide semiconductor field-effect transistor (MOSFET) is presented while considering the effects of high-*k* gate-dielectric material induced fringing-field. The two-dimensional (2D) Poisson's equation is solved in a channel region in order to obtain the surface potential under the assumption of the parabolic potential profile in the transverse direction of the channel with appropriate boundary conditions. The accuracy of the model is verified by comparing the model's results with the 2D simulation results from ATLAS over a wide range of channel lengths and other parameters, including the dielectric constant of gate-dielectric material.

Keywords: recessed-source/drain (Re-S/D), high-*k* gate-material, fringing field and SCEs

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1. Introduction

Over the past few years, considerable attention has been paid to recessed-source/drain (Re-S/D) silicon-on-insulator (SOI) metal-oxide semiconductor field-effect transistor (MOSFET) by both academic researchers and the semiconductor industry due to its better drive current capability than that of the conventional SOI MOSFET.[1–9] In the recessed-source/drain SOI MOSFET, source and drain are extended deeper into the buried oxide (BOX) in order to mitigate the effects of large source and drain resistances, which originate from the ultrathin body structure.[10,11] A number of analytical models have already been presented for short-channel Re-S/D SOI MOSFETs to address various subthreshold parameters, such as threshold voltage,[3–5] subthreshold current, and subthreshold swing.[6,7]

As SOI MOSFET has a highly scalable structure. An ultrathin gate oxide ($t_{ox} < 2$ nm), which is of the SiO_2 in general, is needed to curb the short-channel effects if the device channel length goes below 32 nm.[12] However, an ultrathin gate oxide of thickness less than 2 nm causes a higher leakage current density, which arises mainly from the quantum-mechanical direct tunneling through the gate oxide.[13] Therefore, suitable high-*k* gate-dielectrics with good physical property and low electrical thickness have been looked for in order to control both short-channel effects and gate leakage current simultaneously. HfO_2 (relative permittivity $\varepsilon_k = 22$), ZrO_2 ($\varepsilon_k = 25$), and Ta_2O_5 ($\varepsilon_k = 26$) are found to possess excellent performance with high permittivity and energy gap.[14,15] High on-current and reduced subthreshold swing have already been reported for SOI double-gate MOSFETs by carefully choosing the gate-dielectric material.[16] However, the use of a thicker high-*k* dielectric material in place of SiO_2 causes considerable fringing-field lines, which in turn modulate the source-channel barrier height, resulting in the change of subthreshold characteristics.[17–24] The effect of fringing-field lines on the subthreshold characteristics of SOI MOSFET is modeled in terms of a fringing capacitance C_{bot}.[20] The fringing capacitance is attributed to the electric field interaction between the bottom of gate electrode and source/drain region through the side-wall spacer, as shown in Fig. 1. A large number of theoretical models of C_{bot} have been presented in the technical literature[20–24] for different complementary metal-oxide semiconductor (CMOS) devices. Mohapatra *et al.*[23] developed a parasitic capacitance model in deep submicrometer conventional high-*k* dielectric metal-oxide semiconductor (MOS) transistor in the presence of source/drain electrodes by considering three types of parasitic capacitances: C_{side}, the sidewall fringing capacitance between gate and source/drain regions (through high-*k*); C_{pp}, the parallel plate capacitance between gate and source/drain electrodes; C_{top} the top fringing capacitance between top surface of the gate and source/drain electrodes through the first layer of passivation dielectrics. Later, Kumar *et al.*[20] developed a parasitic capacitance model for high-*k* gate-dielectric silicon-on-insulator (SOI) MOSFET by considering the effect of the parasitic internal fringe capacitance associated with the bottom edge of the

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gate electrode and the source and drain regions. They also developed a threshold voltage model for SOI MOSFET including the fringing capacitance model.[20] A compact model of fringing field induced parasitic capacitance for MOSFET has been developed by Liu *et al.*[24] They have used conformal mapping method to derive the capacitance $C_{\rm bot}$.[24]

However, the effect of high-k dielectric on the subthreshold characteristics of Re-S/D SOI MOSFETs has not been analyzed to date, either experimentally or analytically. In this paper, we present a threshold voltage model, which is an important subthreshold characteristic, of Re-S/D SOI MOSFET with high-k dielectric by considering the influence of fringing field in terms of capacitance $C_{\rm bot}$. The two dimensional (2D) Poisson's equation is solved in a channel region in order to determine the electrostatic potential. Furthermore, the surface potential, which is obtained from 2D electrostatic potential, is modified by adding a potential $V(x)$ in order to capture the effect of high-k dielectric induced fringing field. Moreover, to invoke the effect of lightly doped substrate, which is used generally in practice, a substrate induced surface potential (SISP) parameter is also introduced in the boundary conditions.[25] Subsequently, the minimum of surface potential is utilized to present the threshold voltage model. Both amorphous and epitaxial silicon are found to be used for extended source/drain in Re-S/D SOI MOSFET.[26–29] Thean *et al.*[26] etched out portions of both channel and BOX by selectively using HF solution and they subsequently deposited epitaxial silicon as source and drain regions, including the extended regions in the BOX. On the other hand, Bin[27] in his patent reported that amorphous semiconductor layer is used to form recessed source/drain. The model results are verified by comparing them with the simulated results which are obtained from the 2D simulator from SILVACO.[30]

2. Device simulation

The schematic structure of the Re-S/D UTB SOI MOSFET device with high-k gate-material used in our analysis and simulation is shown in Fig. 1. Here, L, w, $t_{\rm Si}$, $t_{\rm gt}$, $t_{\rm sp}$, $t_{\rm ox}$, and $t_{\rm box}$ are the gate length, channel width, channel thickness, thickness of gate, length of spacer, gate-dielectric thickness, and the thickness of BOX, respectively; $t_{\rm rsd}$ and $d_{\rm box}$ are the source/drain penetration in the BOX and the length of source/drain overlap over the BOX, respectively. A doping concentration $N_{\rm a}$ is assumed to be uniform in the silicon channel region. The high-k gate-dielectric considered for modeling and simulations is HfO_2 with a permittivity (ε_k) of 22, unless otherwise stated. The entire channel region is considered to be ultrathin to avoid the consequence of floating body effects. The x and y axes are considered to be along the channel length and channel thickness respectively as shown in the schematic structure. The drift-diffusion (DD) model of carrier transportation is taken into account in device simulation. The CVT mobility model is also used as it is a versatile mobility model in which mobility depends on many parameters such as doping density, temperature, parallel electric field and vertical electric field. ATLAS default model parameter β and $vsat.n$ are modified by setting $\beta = 1$ and $vsat.n = [(1.5L+21.6)/(L+2.7)] \times 10^7$ cm/s (where L is in nm).[31] This modification is performed in order to calibrate the model results with simulation results as the default DD model of ATLAS simulator starts to predict the inaccurate results in sub 100-nm channel length regime and, therefore, some modifications to the parameters are required. The Fermi–Dirac carrier statistical model is employed to minimize carrier concentration in the heavily doped region. A quantum transport equation is also solved by using non equilibrium Green function (NGEF) approach to include the quantum effects.[30] The symbol and values of all the parameters used during modeling and simulation are detailed in Table 1.

Table 1. Device dimensions and parameters used for simulations.

Parameters	Symbol	Values
Gate work-function	$\phi_{\rm M}$	4.6 eV, 4.8 eV
Channel doping	$N_{\rm a}$	10^{16} cm^{-3}
Source/drain doping	$N_{\rm d}$	10^{20} cm^{-3}
Substrate doping	$N_{\rm sub}$	10^{15} cm^{-3}
Silicon thickness	$t_{\rm Si}$	8 nm
Gate oxide thickness	$t'_{\rm ox}$	1.5 nm–3 nm
Buried oxide thickness	$t_{\rm box}$	100 nm–200 nm
The depth of S/D in the buried oxide	$t_{\rm rsd}$	30 nm, 100 nm
Gate oxide thickness	$t_{\rm gt}$	25 nm
Gate dielectric constant	ε_k	3.8, 12, 22, 27
Length of the spacer	$t_{\rm sp}$	25 nm
Recessed length	$d_{\rm box}$	3 nm
Channel length	L	20 nm–300 nm
Gate voltage	$V_{\rm GS}$	0.1 V
Drain voltage	$V_{\rm DS}$	0.1 V
Substrate voltage	$V_{\rm SUB}$	−3.0 V to 1 V

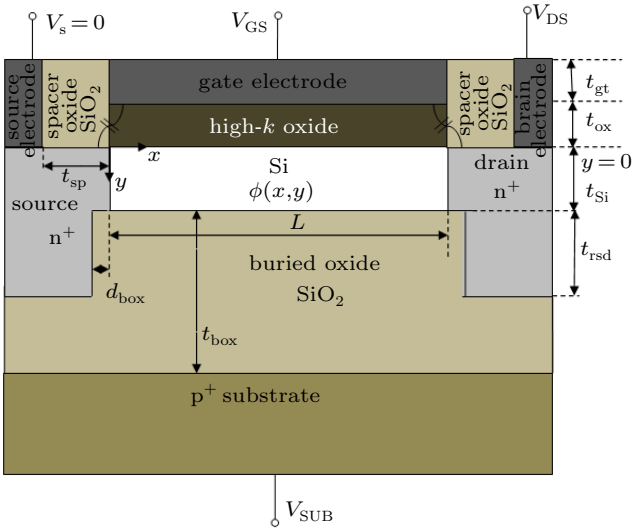


Fig. 1. (color online) Schematic structure of the Re-S/D FD SOI MOSFET, showing the internal parasitic fringe capacitance.

3. Modeling of threshold voltage

3.1. Modeling of surface potential and threshold voltage

Before the onset of strong inversion, the 2D Poisson's equation in the channel region of an Re-S/D fully-depleted (FD) SOI MOSFET, as shown in Fig. 1, can be written as follows:[32]

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=\frac{qN_a}{\varepsilon_{Si}}, \tag{1}$$

where $\phi(x,y)$ is the channel potential and ε_{Si} is permittivity of silicon.

The potential profile in the vertical direction in the channel can be approximated by the following parabolic function as follows:[32]

$$\phi(x,y)=\phi_f(x)+C_1(x)y+C_2(x)y^2. \tag{2}$$

Here, the coefficients $C_1(x)$ and $C_2(x)$ are the functions of x only, and $\phi_f(x)=\phi(x,0)$ is the surface potential at SiO_2/Si interface. These coefficients are to be determined by using the following boundary conditions: the surface potential at the source end is

$$\phi(0,y)=V_{bi}, \tag{3}$$

whereas at the drain end is

$$\phi(L,y)=V_{bi}+V_{DS}. \tag{4}$$

The continuity of the electric flux at the SiO_2/Si interface is formulated as

$$\left[\frac{\partial\phi(x,y)}{\partial y}\right]_{y=0}=\frac{C_{ox}}{\varepsilon_{Si}}\frac{\phi_f(x)-(V_{GS}-V_{FB1})}{L}. \tag{5}$$

The electric flux at the Si/BOX interface is also continuous, as shown below.

$$\left[\frac{\partial\phi(x,y)}{\partial y}\right]_{y=t_{Si}}=\frac{C_{rsd}}{\varepsilon_{Si}}\frac{0-V_{FB2}-\phi_b(x)}{L}+\frac{C_{rsd}}{\varepsilon_{Si}}\frac{V_D-V_{FB2}-\phi_b(x)}{L}+\frac{C_{box}}{\varepsilon_{Si}}\frac{V_{SUB}+\Delta V-V_{FB3}-\phi_b(x)}{L}, \tag{6}$$

where V_{bi} is the built-in voltage at the source/drain and Si given by

$$V_{bi}=\frac{kT}{q}\ln\left(\frac{N_aN_d}{n_i^2}\right),$$

N_d is the doping concentration, n_i is the intrinsic carrier concentration in the silicon, V_{FB1}, V_{FB2}, and V_{FB3} represent the flat-band voltages respectively,[4] V_D and V_{GS} are the drain- and gate-to-source bias-voltages, respectively; and, ΔV is the substrate-induced surface potential (SISP) at substrate/BOX interface. The parameter ΔV has been already derived in our previous work.[4] The potential at channel-BOX interface is

$$\phi_b(x)=\phi_b(x,y=t_{Si}),$$

which is named a back surface potential. The symbol V_{SUB} refers to the substrate bias voltage.

In Eq. (5), C_{ox} is the front channel oxide capacitance per unit length and it is given by[3]

$$C_{ox}=\frac{\varepsilon_{ox}L}{t_{ox}}, \tag{7}$$

with C_{Si} being the silicon channel capacitance per unit length and it is given by

$$C_{Si}=\frac{\varepsilon_{Si}L}{t_{Si}}, \tag{8}$$

C_{box} being the BOX capacitance per unit length and it is given by

$$C_{box}=\frac{\varepsilon_{ox}L}{t_{box}}, \tag{9}$$

C_{rsd} being the recessed source/drain buried-oxide capacitance per unit length and it is given by[4]

$$C_{rsd}=\begin{cases}\dfrac{\varepsilon_{box}}{\theta}\ln\left(1+\dfrac{L}{2d_{box}}\right), & \text{for } \dfrac{L}{2}<t_{rsd},\\ \dfrac{\varepsilon_{box}}{\theta}\ln\left(1+\dfrac{t_{rsd}}{2d_{box}}\right), & \text{for } \dfrac{L}{2}>t_{rsd}=0,\end{cases} \tag{10}$$

with d_{box} being the length of source/drain overlap over BOX,

$$\theta=\left(\frac{\pi}{2}+\frac{\pi}{2}\sec h\frac{t_{rsd}}{d_{box}}\right)$$

being the effective angle between the two slanted electrodes i.e., back-channel and source/drain extension.[4] It is worth noting here that θ is not always necessarily equal to the physical angle between Re-S/D and back-channel. It can be noticed that θ is $\pi/2$ for the Re-S/D SOI MOSFET as $d_{box}=0$, whereas becomes π for the conventional SOI MOSFETs because of $t_{rsd}=0$. Therefore, with the introduction of parameter d_{box}, the present model becomes more flexible.

Upon solving the Poisson's equation by using Eq. (1) with the help of boundary conditions given by Eqs. (5) and (6) at both front and back surface of silicon body, we obtain the following expression of 2D channel potential $\phi(x,y)$:

$$\begin{aligned}\phi(x,y)\;=\;&\phi_f(x)+\frac{C_{ox}}{t_{Si}\cdot C_{Si}}[\phi_f(x)-(V_G-V_{FB1})]y\\&+\frac{C_{box}}{2t_{Si}^2\cdot C_{Si}}y^2\left\{\frac{C_{rsd}}{2t_{Si}^2\cdot C_{Si}}[V_{DS}-2V_{FB2}-\phi_b(x)]\right.\\&+[V_{SUB}+\Delta V-V_{FB3}-\phi_b(x)]\\&\left.+\frac{C_{ox}}{2t_{Si}^2\cdot C_{Si}}[\phi_f(x)-(V_G-V_{FB1})]\right\}.\end{aligned} \tag{11}$$

Further, the following two differential equations for $\phi_{f,b}$ are obtained by using $\phi(x,y)$ of Eq. (11) in Eq. (1) at $y=0$ and $y=t_{Si}$ respectively,

$$\frac{d^2\phi_{f,b}(x)}{dx^2}-\alpha_{f,b}\phi_{f,b}(x)=\beta_{f,b}, \tag{12}$$

where,

$$\alpha_f=2\frac{1+\left(\dfrac{C_{ox}(C_{Si}+2C_{rsd}+C_{box})}{C_{Si}(2C_{rsd}+C_{ox})}\right)}{t_{Si}^2\left(1+2\dfrac{C_{Si}}{2C_{rsd}+C_{ox}}\right)}, \tag{13}$$

$$\beta_{\rm f}=\frac{qN_{\rm a}}{\varepsilon_{\rm Si}}-2\frac{\left[(V_{\rm GS}-V_{\rm FB1})\left(\frac{C_{\rm ox}\left(C_{\rm Si}+2C_{\rm rsd}+C_{\rm box}\right)}{C_{\rm Si}\left(2C_{\rm rsd}+C_{\rm ox}\right)}\right)+(V_{\rm DS}-2V_{\rm FB2})\left(\frac{2C_{\rm rsd}}{2C_{\rm rsd}+C_{\rm box}}\right)+(V_{\rm SUB}+\Delta V-V_{\rm FB3})\left(\frac{2C_{\rm box}}{2C_{\rm rsd}+C_{\rm box}}\right)\right]}{t_{\rm Si}^2\left(1+2\frac{C_{\rm Si}}{2C_{\rm rsd}+C_{\rm ox}}\right)},\quad(14)$$

$$\alpha_{\rm b}=2\frac{1+\left(\frac{\left(C_{\rm ox}+C_{\rm Si}\right)\left(2C_{\rm rsd}+C_{\rm box}\right)}{C_{\rm ox}C_{\rm Si}}\right)}{t_{\rm Si}^2\left(1+2\frac{C_{\rm Si}}{C_{\rm ox}}\right)},\quad(15)$$

$$\beta_{\rm b}=\frac{qN_{\rm a}}{\varepsilon_{\rm Si}}-2\frac{(V_{\rm GS}-V_{\rm FB1})+(V_{\rm DS}-2V_{\rm FB2})\left(\frac{C_{\rm rsd}}{C_{\rm ox}}+\frac{C_{\rm rsd}}{C_{\rm Si}}\right)+(V_{\rm SUB}+\Delta V-V_{\rm FB3})}{t_{\rm Si}^2\left(1+2\frac{C_{\rm Si}}{C_{\rm ox}}\right)}.\quad(16)$$

Using the boundary conditions of Eqs. (3) and (4) in solving Eq. (12) gives the following equations for the front and back surface potential

$$\phi_{\rm f,b}=A_{\rm f,b}\,{\rm e}^{\sqrt{\alpha_{\rm f,b}}x}+B_{\rm f,b}\,{\rm e}^{\sqrt{\alpha_{\rm f,b}}x}-\frac{\beta_{\rm f,b}}{\alpha_{\rm f,b}},\quad(17)$$

where

$$A_{\rm f,b}=\frac{\beta_{\rm f,b}\left({\rm e}^{\sqrt{\alpha_{\rm f,b}}L}-1\right)+\alpha_{\rm f,b}\left[V_{\rm bi}\left({\rm e}^{\sqrt{\alpha_{\rm f,b}}L}-1\right)+V_{\rm DS}\,{\rm e}^{\sqrt{\alpha_{\rm f,b}}L}\right]}{\alpha_{\rm f,b}\left({\rm e}^{2\sqrt{\alpha_{\rm f,b}}L}-1\right)},\quad(18)$$

$$B_{\rm f,b}=\frac{{\rm e}^{\sqrt{\alpha_{\rm f,b}}L}\left\{\beta_{\rm f,b}\left({\rm e}^{\sqrt{\alpha_{\rm f,b}}L}-1\right)-\alpha_{\rm f,b}\left[V_{\rm bi}\left(1-{\rm e}^{\sqrt{\alpha_{\rm f,b}}L}\right)+V_{\rm DS}\right]\right\}}{\alpha_{\rm f,b}\left({\rm e}^{2\sqrt{\alpha_{\rm f,b}}L}-1\right)}.\quad(19)$$

The positions $(x_{\rm min})_{\rm f,b}$ of the front and back channel minimum surface potentials (virtual cathode potential, $\phi_{\rm f,b\,min}$) can be obtained by solving

$$\left.\frac{{\rm d}\phi_{\rm f,b}(x)}{{\rm d}x}\right|_{(x_{\rm min})_{\rm f,b}}=0$$

and are determined as

$$(x_{\rm min})_{\rm f,b}=\frac{1}{2}\frac{\ln\left(B_{\rm f,b}/A_{\rm f,b}\right)}{\sqrt{\alpha_{\rm f,b}}}.\quad(20)$$

The minimum values of front and back surface potential $\phi_{\rm f,b\,min}$ can be obtained by substituting $(x_{\rm min})_{\rm f,b}$ of Eq. (20) into Eq. (11) as

$$\phi_{\rm f,b\,min}=2\sqrt{A_{\rm f,b}B_{\rm f,b}}-\frac{\beta_{\rm f,b}}{\alpha_{\rm f,b}}.\quad(21)$$

Furthermore, in order to obtain the surface potential including the effect of the fringe capacitance $C_{\rm bot}$, the potentials $V_{\rm f,b}\left(x,\sigma_1\right)|_{\rm source}$ and $V_{\rm f,b}\left(L_{\rm g}-x,\sigma_2\right)|_{\rm drain}$ due to the charges on the source and drain regions, respectively, are added to surface potential $\phi_{\rm f,b}$ and the expression for surface potential Eq. (11) is modified as

$$\phi_{\rm f,b}=A_{\rm f,b}\,{\rm e}^{\sqrt{\alpha_{\rm f,b}}x}+B_{\rm f,b}\,{\rm e}^{\sqrt{\alpha_{\rm f,b}}x}-\frac{\beta_{\rm f,b}}{\alpha_{\rm f,b}}+\left(V_{\rm f,b}(x,\sigma_1)|_{\rm source}+V_{\rm f,b}\left(L_{\rm g}-x,\sigma_2\right)|_{\rm drain}\right).\quad(22)$$

The origin and derivation of potential $V\left(x,\sigma_{1,2}\right)$ are discussed in Subsection 3.2.

Now, the minimum values of front and back surface potential could be obtained by using Eq. (22). However, the direct derivative of Eq. (22) may lead to a very complicated equation of $(x_{\rm min})_{\rm f,b}$ and which in turn gives an implicit equation for threshold voltage. Therefore, assuming that first two terms vary more rapidly than the last two, and the last two terms only modify the minimum values of $\phi_{\rm min\,f,b}$, the following equations for the modified minimum front and back surface potentials could be obtained:

$$\phi'_{\rm min\,f,b}=2\sqrt{A_{\rm f,b}B_{\rm f,b}}-\frac{\beta_{\rm f,b}}{\alpha_{\rm f,b}}+\left(V_{\rm f,b}\left(x,\sigma_1\right)|_{\rm source}+V_{\rm f,b}\left(L_{\rm g}-x,\sigma_2\right)|_{\rm drain}\right)|_{x=x_{\rm min}}.\quad(23)$$

The threshold voltages associated with front and back surfaces of the channel could be obtained by using

$$\phi'_{\rm min\,f,b}\big|_{V_{\rm G}=V_{\rm th\,f,b,}}=2\phi_{\rm f},\quad(24)$$

where $\phi_{\rm f}$ is the Fermi potential.

Now, after inserting Eq. (23) into Eq. (24), we obtain the following equations for front and back channel-surface threshold voltages $V_{\rm th\,f,b}$:

$$V_{\rm th\,f,b}=\frac{-b_{\rm f,b}+\sqrt{b_{\rm f,b}^2-4a_{\rm f,b}c_{\rm f,b}}}{2a_{\rm f,b}},\quad(25)$$

where

$$a_{\rm f,b}=u_{\rm f1,b1}u_{\rm f2,b2}-\left(\frac{m_{\rm f,b}}{2\alpha_{\rm f,b}}\right)^2,\quad(26)$$

$$c_{\rm f,b}=v_{\rm f1,b1}v_{\rm f2b2}-\phi_{\rm f}^2-\left(\frac{n_{\rm f,b}}{2\alpha_{\rm f,b}}\right)^2-\frac{n_{\rm f,b}}{\alpha_{\rm f,b}}\phi_{\rm f},\quad(27)$$

$$b_{\rm f,b}=u_{\rm f1,b1}v_{\rm f2b2}+u_{\rm f2b2}v_{\rm f1,b1}-\frac{m_{\rm f,b}n_{\rm f,b}}{2\alpha_{\rm f,b}^2}-\frac{m_{\rm f,b}}{\alpha_{\rm f,b}}\phi_{\rm f},\quad(28)$$

$$v_{\rm f1,b1}=\frac{n_{\rm f,b}\left({\rm e}^{\sqrt{\alpha_{\rm f,b}}L}-1\right)+\alpha_{\rm f,b}\left[V_{\rm bi}\left({\rm e}^{\sqrt{\alpha_{\rm f,b}}L}-1\right)+V_{\rm DS}\,{\rm e}^{\sqrt{\alpha_{\rm f,b}}L}\right]}{\alpha_{\rm f,b}\left({\rm e}^{2\sqrt{\alpha_{\rm f,b}}L}-1\right)},\quad(29)$$

$$v_{\rm f2,b2}=\frac{{\rm e}^{\sqrt{\alpha_{\rm f,b}}L}\left\{n_{\rm f,b}\left({\rm e}^{\sqrt{\alpha_{\rm f,b}}L}-1\right)-\alpha_{\rm f,b}\left[V_{\rm bi}\left(1-{\rm e}^{\sqrt{\alpha_{\rm f,b}}L}\right)+V_{\rm DS}\right]\right\}}{\alpha_{\rm f,b}\left({\rm e}^{2\sqrt{\alpha_{\rm f,b}}L}-1\right)},\quad(30)$$

$$u_{\mathrm{f1,b1}} = \frac{m_{\mathrm{f,b}}\left(\mathrm{e}^{\sqrt{\alpha_{\mathrm{f,b}}}L}-1\right)}{\alpha_{\mathrm{f,b}}\left(\mathrm{e}^{2\sqrt{\alpha_{\mathrm{f,b}}}L}-1\right)}, \tag{31}$$

$$u_{\mathrm{f2,b2}} = \frac{m_{\mathrm{f,b}}\,\mathrm{e}^{\sqrt{\alpha_{\mathrm{f,b}}}L}\left(\mathrm{e}^{\sqrt{\alpha_{\mathrm{f,b}}}L}-1\right)}{\alpha_{\mathrm{f,b}}\left(\mathrm{e}^{2\sqrt{\alpha_{\mathrm{f,b}}}L}-1\right)}, \tag{32}$$

$$m_{\mathrm{f,b}} = -2\frac{\left(\dfrac{C_{\mathrm{ox}}\left(C_{\mathrm{Si}}+2C_{\mathrm{rsd}}+C_{\mathrm{box}}\right)}{C_{\mathrm{Si}}\left(2C_{\mathrm{rsd}}+C_{\mathrm{ox}}\right)}\right)}{t_{\mathrm{Si}}^2\left(1+2\dfrac{C_{\mathrm{Si}}}{2C_{\mathrm{rsd}}+C_{\mathrm{ox}}}\right)}, \tag{33}$$

$$n_{\mathrm{f,b}} = \frac{qN_{\mathrm{a}}}{\varepsilon_{\mathrm{Si}}}+2\frac{\left[\left(V_{\mathrm{FB1}}\right)\left(\dfrac{C_{\mathrm{ox}}\left(C_{\mathrm{Si}}+2C_{\mathrm{rsd}}+C_{\mathrm{box}}\right)}{C_{\mathrm{Si}}\left(2C_{\mathrm{rsd}}+C_{\mathrm{ox}}\right)}\right)-\left(V_{\mathrm{DS}}-2V_{\mathrm{FB2}}\right)\left(\dfrac{2C_{\mathrm{rsd}}}{2C_{\mathrm{rsd}}+C_{\mathrm{box}}}\right)\right)\left(-\left(V_{\mathrm{SUB}}-V_{\mathrm{FB3}}\right)\left(\dfrac{2C_{\mathrm{box}}}{2C_{\mathrm{rsd}}+C_{\mathrm{box}}}\right)\right]}{t_{\mathrm{Si}}^2\left(1+2\dfrac{C_{\mathrm{Si}}}{2C_{\mathrm{rsd}}+C_{\mathrm{ox}}}\right)}, \tag{34}$$

and finally, the threshold voltage V_{th} of Re-S/D SOI MOSFETs could be given as follows:[4]

$$V_{\mathrm{th}} = \begin{cases} V_{\mathrm{thf}}, & \text{for } \phi_{\mathrm{f,min}} > \phi_{\mathrm{b,min}}, \\ V_{\mathrm{thb}}, & \text{for } \phi_{\mathrm{f,min}} < \phi_{\mathrm{b,min}}. \end{cases} \tag{35}$$

3.2. Derivation of $V(x)$

The electric field lines that originate from the bottom of the gate and enter into the source and drain through the spacer induce electrostatic charges in source and drain region. The surface charge density, σ_i ($i = 1$ and 2 for source and drain, respectively) due to fringing electric field lines is given in Fig. 2.[20]

$$\sigma_i = \left(\frac{(C_{\mathrm{bot}})V_{\mathrm{pi}}}{W\cdot t_{\mathrm{sp}}}\right), \quad i = 1,2, \tag{36}$$

where $V_{\mathrm{p1}} = V_{\mathrm{bi}} - V_{\mathrm{GS}} + V_{\mathrm{FB2}}$ and $V_{\mathrm{p2}} = V_{\mathrm{bi}} + V_{\mathrm{DS}} - V_{\mathrm{GS}} + V_{\mathrm{FB2}}$ are the source and drain region potential respectively, W is width of gate and t_{sp} is spacer thickness between gate sidewall and source/drain contacts.

The parasitic internal fringe capacitances associated with bottom edge of gate electrode can be calculated as[20]

$$C_{\mathrm{bot}} = \frac{(0.3)\varepsilon_{\mathrm{eff}}W}{\pi}, \tag{37}$$

where

$$\varepsilon_{\mathrm{eff}} = \frac{\varepsilon_k\varepsilon'_{\mathrm{sp}}}{\varepsilon_k-\varepsilon'_{\mathrm{sp}}}\ln\left(\frac{\varepsilon_k}{\varepsilon'_{\mathrm{sp}}}\right), \quad \varepsilon'_{\mathrm{sp}} = \left(1+\frac{t'_{\mathrm{ox}}}{L}\right)\varepsilon_{\mathrm{sp}}$$

is the effective permittivity of spacer material, $\varepsilon_{\mathrm{ox}}$ and $\varepsilon_{\mathrm{sp}}$ are the permittivity values of gate dielectric and spacer material respectively, t_{ox} is the gate oxide thickness, and L is the gate length.

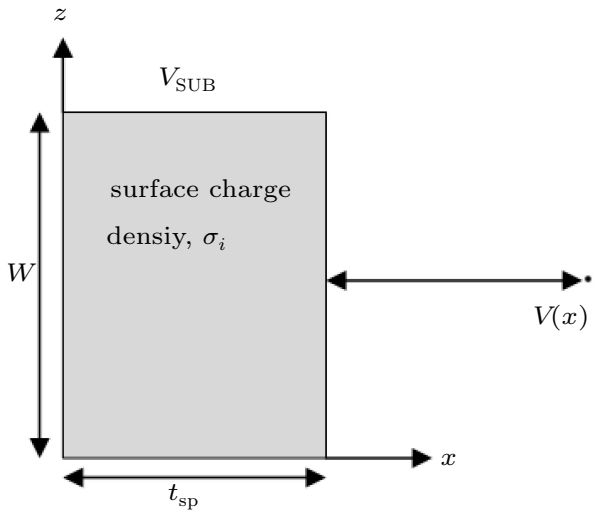


Fig. 2. Potential due to uniformly surface-charged plate.

Now, the potential at a distance 'x' from uniformly charged plate is given by[20]

$$V(x,\sigma_i) = \frac{1}{2}\int_0^{t_{\mathrm{sp}}}\int_{-W/2}^{W/2}\frac{\sigma_i\,\mathrm{d}x_1\,\mathrm{d}x_2}{4\pi\varepsilon_{\mathrm{Si}}\sqrt{(x+x_1)^2+(x_2)^2}}, \tag{38}$$

$$V_{\mathrm{f}}(x,\sigma_i) = \frac{\sigma_i}{8\pi\varepsilon_{\mathrm{Si}}}\left[(x+t_{\mathrm{sp}})\cdot\ln\left\{\frac{\sqrt{(x+t_{\mathrm{sp}})^2+(W^2/4)}+(W/2)}{\sqrt{(x+t_{\mathrm{sp}})^2+(W^2/4)}-(W/2)}\right\}-x\cdot\ln\left\{\frac{\sqrt{(x+t_{\mathrm{sp}})^2+(W^2/4)}+(W/2)}{\sqrt{(x+t_{\mathrm{sp}})^2+(W^2/4)}-(W/2)}\right\}\right.$$
$$\left.+W\cdot\ln\left\{\frac{\sqrt{(x+t_{\mathrm{sp}})^2+(W^2/4)}+t_{\mathrm{sp}}+\sqrt{x^2+t_{\mathrm{sp}}^2+2t_{\mathrm{sp}}\sqrt{x^2+(W^2/4)}}}{\sqrt{x^2+(W^2/4)}+x}\right\}\right]. \tag{39}$$

Similarly, the closed form expression of $V_{\mathrm{b}}(x,\sigma_i)$ can be obtained by replacing x_1 limits to $\int_0^{t_{\mathrm{rsd}}}$ in Eq. (38).

3.3. Threshold voltage model including quantum mechanical effects (QMEs)

The model accuracy has been improved for ultrathin body structure by adding the following quantum effects induced correction term ΔV_{th} in the threshold voltage model of Eq. (35).[33,34]

$$\Delta V_{\mathrm{th}} = \Delta E_0\left(1+\frac{\varepsilon_{\mathrm{si}}t'_{\mathrm{ox}}}{\varepsilon_k t_{\mathrm{si}}+\varepsilon_{\mathrm{Si}}t_{\mathrm{box}}}\right), \tag{40}$$

where ΔE_0 is the difference between the first discrete energy level and the lowest conduction band energy level.[33,34]

4. Results and discussion

In this section, the results obtained from theoretical models of surface potential and threshold voltage are compared with the numerical simulation results. Following the constant current method of threshold voltage extraction, $V_{\rm th}$ is obtained from the drain current–gate voltage curve by considering the value of the gate voltage at drain current magnitude given by $I_{\rm d} = (w/L) \times 10^{-7}$ A/μm,[35] where w and L are width and length of the channel, respectively. It should be noted that the gate oxide thickness shown in the figure is actually the electrical (or effective) thickness $t'_{\rm ox}$ where $t'_{\rm ox} = t_{\rm ox}\left(\varepsilon_{\rm SiO_2}/\varepsilon_k\right)$, with $\varepsilon_{\rm SiO_2}$ being the permittivity of silicon dioxide and ε_k being the permittivity of high-k material. The front and back channel surface potentials of a Re-S/D SOI MOSFET along the channel length direction are displayed in Fig. 3 with considering HfO_2 as a gate dielectric. The other device parameters are $\phi_{\rm M} = 4.8$ eV, $N_{\rm a} = 10^{16}$ cm^{-3}, $N_{\rm d} = 10^{20}$ cm^{-3}, $t_{\rm box} =$ 100 nm, $t_{\rm Si} = 8$ nm, $t_{\rm rsd} = 30$ nm, $t'_{\rm ox} = 1.5$ nm, $V_{\rm DS} = 0.1$ V, $V_{\rm GS} = 0.1$ V, and $L = 45$ nm. It is noticed from the figure that back-channel minimum surface potential is 30 mV higher than the front-channel minimum surface potential for the selected device dimensions and the channel-doping level. Therefore, the device threshold voltage is mainly under the control of the back-channel rather than the front channel, which is in contrast to the conventional SOI MOSFET. It should be noted that in the case of a highly doped channel, although not considered in this work, Re-S/D SOI MOSFET behaves like a conventional SOI MOSFET, i.e., the front surface of the device becomes inverted at first.

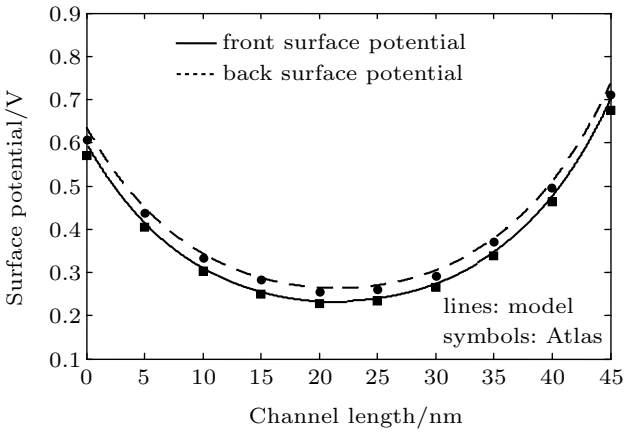


Fig. 3. Surface potentials versus the channel length in front and back channel. The other device parameters are: $\phi_{\rm M} = 4.8$ eV, $N_{\rm a} = 10^{16}$ cm^{-3}, $N_{\rm d} = 10^{20}$ cm^{-3}, $t_{\rm box} = 200$ nm, $t_{\rm Si} = 8$ nm, $t_{\rm rsd} = 30$ nm, $t'_{\rm ox} = 1.5$ nm, $\varepsilon_k = 22$, $V_{\rm GS} = 0.1$ V, $V_{\rm DS} = 0.1$ V.

Figure 4 displays the back surface potential variation against the channel length for different values of gate dielectric constant (ε_k). The minimum of the back surface potential is found to increase as the gate dielectric constant increases. This increase in the minimum of back surface potential leads to the lowering of the source-channel barrier height, which subsequently results in change in the threshold voltage. It could be safely concluded here that fringing field lines considerably modulate the threshold voltage of a Re-S/D SOI MOSFET.

Figure 5 shows the threshold voltages of Re-S/D SOI MOSFETs versus channel length for the BOX thickness values of 100 nm and 200 nm. It is observed that the device with a thinner BOX has a higher threshold voltage and is also less prone to short-channel effects (SCEs).

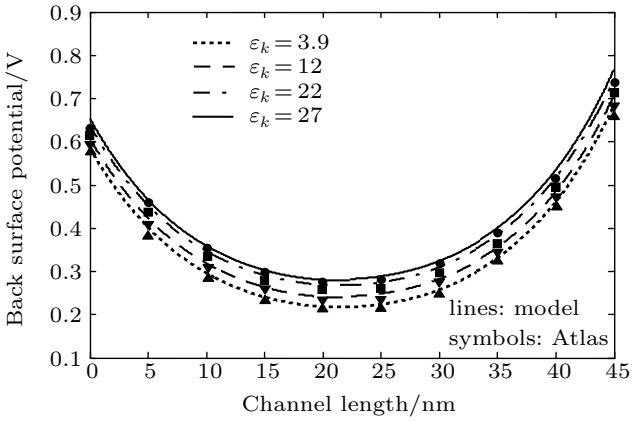


Fig. 4. Back surface potentials versus channel length for various values of gate-dielectric constant (ε_k). The other device parameters are the same as those in Fig. 3.

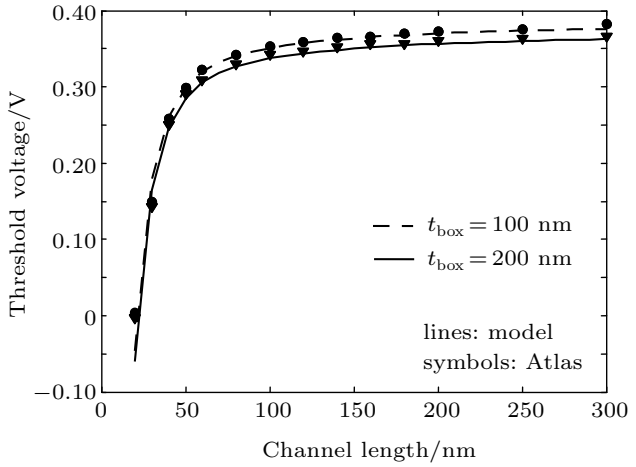


Fig. 5. Threshold voltages versus gate length for buried oxide thickness values. The other device parameters are the same as those in Fig. 3.

Figure 6 shows the variations of threshold voltage with channel length for the values of oxide thickness, $t'_{\rm ox} = 1.5$ nm and 3 nm. It is observed that a device with lower effective oxide thickness suffers less variation for short channel device due to increase in electric field control in the channel region.

Figure 7 shows the variations of threshold voltage with channel length while $t_{\rm rsd}$ serves as a variable parameter with HfO_2 as a dielectric material. The selected thickness values for source and drain penetration in the BOX are $t_{\rm rsd} = 0$ nm, 30 nm, and 100 nm. It should be noted that for $t_{\rm rsd} = 0$ the device acts as a conventional SOI MOSFET, and as a result, the threshold voltage remains higher than the case of $t_{\rm rsd} = 30$ nm

and 100 nm. This may be attributed to the fact that at lower channel doping, the back surface may turn inverted at first if the channel length is too short ($L < 70$ nm). And, since the back channel is partially controlled by source and drain extension, the subthreshold characteristics of the device are deteriorated.

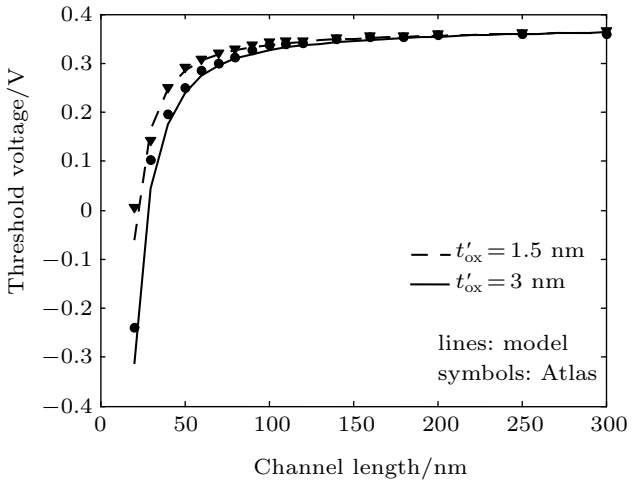


Fig. 6. Threshold voltages versus gate length for different gate oxide thickness values. The other device parameters are the same as those in Fig. 3.

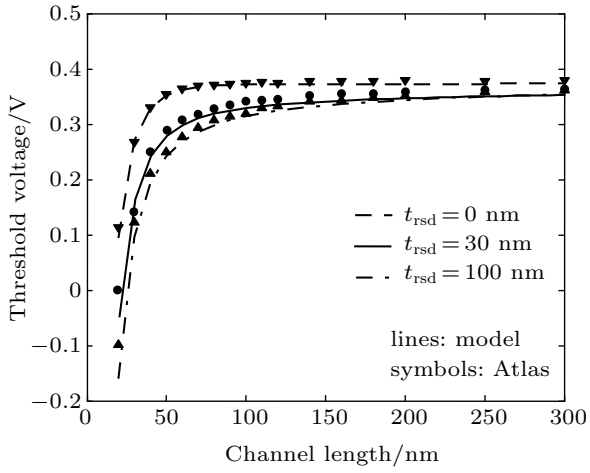


Fig. 7. Threshold voltages versus gate length for different recessed oxide thickness values. The other device parameters are the same as those in Fig. 3.

Figure 8 shows the variation of threshold voltage with the dielectric constant of gate-dielectric, whereas the other device parameters are $\phi_M = 4.6$ eV, $N_a = 10^{16}$ cm^{-3}, $N_d = 10^{20}$ cm^{-3}, $t_{Si} = 8$ nm, $t_{rsd} = 30$ nm, $N_d = 200$ nm, $V_{GS} = 0.1$ V, and $L = 45$ nm. The threshold voltage of the device is found to decrease with the increase of dielectric constant. This observation is in line with the case of Fig. 4, where a minimum of surface potential is found to increase with the increase of the dielectric constant, ε_k. It should be noted that the source channel barrier height becomes lower with the increase of the minimum of the surface potential and, as a result, charge carriers from the source may be easily injected into the channel region, which is an indication of lowering the threshold voltage.

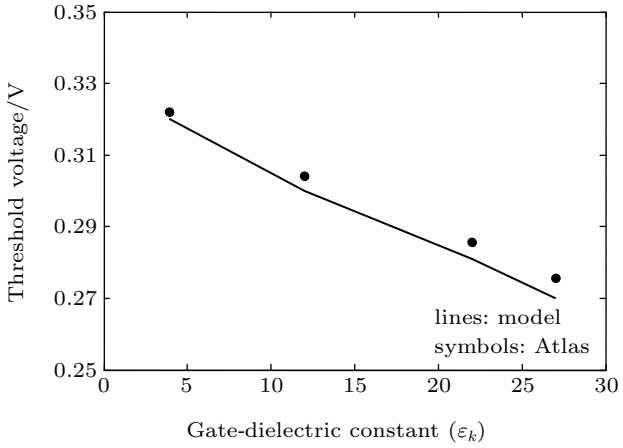


Fig. 8. Threshold voltage versus gate-dielectric constant (ε_k). The other device parameters are described in the text.

5. Conclusions

A 2D threshold voltage model of FD recessed-source/drain (Re-S/D) SOI MOSFET with high-k gate dielectric material is presented for the first time. The present model includes the effect of high-k dielectric induced fringing field lines in terms of capacitance C_{bot}, which appears to be due to the electrostatic interaction between the bottom of the gate-electrode and source/drain. It is found that the present model predicts the threshold voltage of Re-S/D SOI MOSFET correctly in wide ranges of gate-dielectric materials and other device parameters. The derived model results are compared with simulation results which are obtained from ATLAS^{TM} (Silvaco), showing that they are in good agreement with each other in a wide variation range of device parameters.

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