Fermi level pinning effects at gate–dielectric interfaces influenced by interface state densities*

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The dependences of Fermi-level pinning on interface state densities for the metal–dielectric, ploycrystalline silicon–dielectric, and metal silicide–dielectric interfaces are investigated by calculating their effective work functions and their pinning factors. The Fermi-level pinning factors and effective work functions of the metal–dielectric interface are observed to be more susceptible to the increasing interface state densities, differing significantly from that of the ploycrystalline silicon–dielectric interface and the metal silicide–dielectric interface. The calculation results indicate that metal silicide gates with high-temperature resistance and low resistivity are a more promising choice for the design of gate materials in metal-oxide semiconductor (MOS) technology.

Keywords: interface state density, Fermi-level pinning, MIS structure, effective work function

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1. Introduction

With aggressive down-scaling of complementary metal-oxide-semiconductor (CMOS) transistors, traditional polycrystalline silicon gates have been replaced by metal gates on a high-k dielectric layer to optimize the threshold voltage by reducing the gate depletion effect.[1,2] However, the desirable effective metal work function $\phi_{\mathrm{m,eff}}$ for the metal gate remains a challenge because of stronger Fermi-level pinning effects at the metal–dielectric interface, which has been well explained by the metal-induced gap state (MIGS) model.[3] The pinning factor S is used to reflect the distortion slope of the vacuum level of the metal gate by the dielectric screening, which can be evaluated by the interface state density of the unoccupied donor-like states above the metal Fermi level E_{fm} for a given metal–dielectric interface. Charges transfer across the metal–dielectric interface to create a dipole by these unoccupied donor-like states. The interface dipole drives the metal Fermi level toward the charge neutrality level $E_{\mathrm{cnl,d}}$ on the dielectric side to give a zero dipole charge. Consequently, the effective metal work function differs from the vacuum metal work function $\phi_{\mathrm{m,vac}}$.

In the MIGS model, the wave functions of the electrons will decay exponentially in the dielectric layer but they will keep continuity at the metal–dielectric interface, generating intrinsic states in the band gap.[3] The pinning factor S depends on the density of interface states around the charge neutrality level of the high-k dielectric layer $D_{\mathrm{dm}}(E_{\mathrm{cnl}})$ and the width of the dipole layer δ as[4]

$$S = \frac{1}{1 + e^2 D_{\mathrm{dm}}(E_{\mathrm{cnl}})\delta/\varepsilon_0}. \tag{1}$$

The parameter $D_{\mathrm{dm}}(E_{\mathrm{cnl}})\delta$ is related to the electronic polarizability $(\varepsilon_\infty - 1)$ of the high-k dielectric layer. The empirical relationship between S and $(\varepsilon_\infty - 1)$ has been given by[5]

$$S = \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2}. \tag{2}$$

There are two limits: (i) the pinning factor $S = 1$ suggests that the effective metal work function equals metal work function in vacuum, indicating no pinning in the band gap; and, (ii) the pinning factor $S = 0$ indicates that the Fermi-level of the interface is strongly pinned at the charge neutrality level of the high-k dielectric layer, which can be regarded as a semiconductor with a wide band gap,[6] making the effective work function depend entirely on the characteristic of interface. Effective metal work functions on high-k dielectrics such as SiO_2, Al_2O_3, Si_3N_4, ZrO_2, and HfO_2 are achieved to differ from their values in vacuum with the empirical model.[5,7,8] In fact, if the high-k dielectric is definite, then the same value of S for each metal would be determined according to the empirical model. Furthermore, the deviation between the slope of the MIGS line in metal–dielectric-semiconductor stacks and the experimental data indicates that there are other factors that influence the Fermi-level pinning effect.[9,10] It has been observed that the Fermi-level pinning effect is also influenced by the electron state density of the metal gate induced by the image charge of the interface charge. The pinning factor S can be further calculated by the continuity of the vacuum level and charge neutralization conditions.[11] The calculation provides a more precise value of S than that in MIGS. However, there are still few results concerning the change of the electron state density and interface state density.

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Although a polysilicon gate suffers gate depletion, high poly-sheet resistance, boron penetration, and other problems, the high-temperature resistant and the natural oxide layer allow the polysilicon gates to be more meaningful than metal gate in some respects. In this work, the dependences of Fermi-level pinning on interface state densities for the metal–dielectric, ploycrystalline silicon–dielectric, and metal silicide–dielectric interfaces are investigated to understand the Fermi-level pinning effects of gate–dielectric interfaces. The calculation results of the pinning factors and effective work functions of gate materials indicate that a metal silicide would be a more appropriate option for designing the gate materials in MOS technology.

2. Method

When a metal connects to a high-k dielectric, the electrons of the metal gate will flow from the metal into the dielectric layer, exchanging charges with the interface states in the dielectric layer created by metal-induced gap states and external defects.[12–15] This drives the metal Fermi-level $E_{\rm fm}$ to move toward a position at the high-k dielectric so that the net dipole charge would become neutral and the system would become balanced. The position at the high-k dielectric is known as the charge neutrality level $E_{\rm cnl,d}$.[7,8] The equilibrium Fermi-level $E_{\rm fm,eff}$ is at the position of Fermi-level pinning.

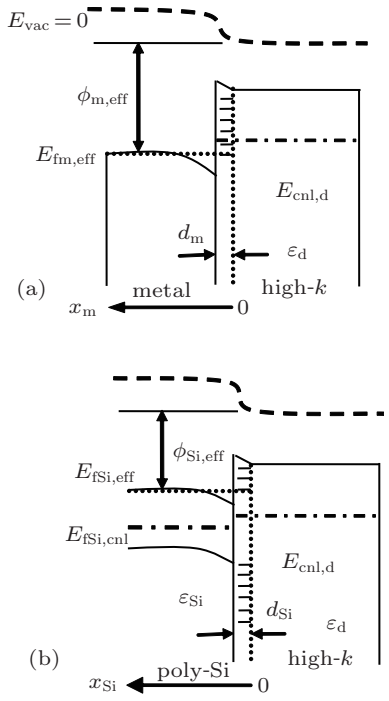


Fig. 1. Schematic diagrams of the band alignment of the formed metal–dielectric and ploycrystalline silicon–dielectric gate stacks.

As shown in Fig. 1, a dipole will be formed at the metal–dielectric interface as a negative charge builds up on the dielectric side and an image positive charge builds up on the metal side. An electrostatic potential induced by the dipole will give rise to the deformation of the vacuum level, especially for the vacuum level of the metal $U_{\rm m}$ and metal–dielectric interfacial layer $U_{\rm dm}$. The net charge density of the metal–dielectric interface $\rho_{\rm dm}(x)$ is determined by the states between $E_{\rm cnl,d}$ and $E_{\rm fm,eff}$, while the image charge density of the metal $\rho_{\rm m}(x)$ depends on the states between $E_{\rm fm}$ and $E_{\rm fm,eff}$. The charge density is determined by the following equations:[11,12]

$$\rho_{\rm dm}(x) = eD_{\rm dm}(U_{\rm dm} + E_{\rm cnl,d} - E_{\rm fm,eff}), \tag{3}$$

$$\rho_{\rm m}(x) = eD_{\rm m}(U_{\rm m} + E_{\rm fm} - E_{\rm fm,eff}), \tag{4}$$

where e is the elementary charge, $D_{\rm dm}$ and $D_{\rm m}$ are the interface state density of metal–dielectric interface and electron state density of the metal, respectively. As shown in Fig. 1(b), the connection of high-k dielectric with ploycrystalline silicon is similar to that of the metal with high-k dielectric. In fact, the principles of connections are derived from the semiconductor heterojunction interfaces given by Tersoff.[16] However, the critical characteristic that differentiates the ploycrystalline silicon–dielectric interface from metal–dielectric interface is the absence of interface states at the overlapping band gap.[7,8] As the charge neutrality level in ploycrystalline silicon $E_{\rm cnl,Si}$ moves toward $E_{\rm cnl,d}$, the net charge density $\rho_{\rm dSi}(x)$ at the ploycrystalline silicon–dielectric interface is produced by the states which are induced by the alignment of $E_{\rm cnl,Si}$ and $E_{\rm cnl,d}$ as well as by the position of Fermi-level $E_{\rm fSi}$ in vacuum and equilibrium Fermi-level $E_{\rm fSi,eff}$ for ploycrystalline silicon, while the image charge density of ploycrystalline silicon $\rho_{\rm Si}(x)$ depends on the states between $E_{\rm fSi}$ and $E_{\rm fSi,eff}$. The vacuum level of ploycrystalline silicon $U_{\rm Si}$ and the ploycrystalline silicon–dielectric interface $U_{\rm dSi}$ are continuous, the charge density is given by the following equations:[11,12]

$$\rho_{\rm Si}(x) = eD_{\rm Si}(U_{\rm Si} + E_{\rm fSi} - E_{\rm fSi,eff}), \tag{5}$$

$$\rho_{\rm dSi}(x) = eD_{\rm dSi}(U_{\rm dSi} + E_{\rm cnl,d} - E_{\rm cnl,Si} + E_{\rm fSi} - E_{\rm fSi,eff}), \tag{6}$$

where $D_{\rm dSi}$ and $D_{\rm Si}$ are the interface state density of ploycrystalline silicon–dielectric interface and electron state density of the ploycrystalline silicon, respectively. Since the charge density $\rho(x)$, vacuum level U, and electrostatic potential ϕ have the equations $U=-e\phi$ and $\mathrm{d}^2\phi/\mathrm{d}x^2=-\rho(x)/\varepsilon$ (ε is the permittivity of material), the equilibrium Fermi-levels can be calculated by using the boundary conditions of $U(0)=0$, $U(x)$, and $\mathrm{d}U/\mathrm{d}x$ continuous at $x=d_{\rm m/Si}$ ($d_{\rm m}$ or $d_{\rm Si}$ is the thickness of metal–dielectric or ploycrystalline silicon–dielectric interfacial layer, respectively).[12] The effective work functions $\phi_{\rm m}=0-E_{\rm fm}$ and $\phi_{\rm Si,eff}=0-E_{\rm fSi,eff}$ of the metal and ploycrystalline silicon are expressed, respectively, as

$$\phi_{\rm m,eff} = S_{\rm m}\cdot(\phi_{\rm m} - \phi_{\rm cnl,d}) + \phi_{\rm cnl,d}, \tag{7}$$

$$\phi_{\mathrm{Si,eff}} = (S_{\mathrm{Si}} - 1) \cdot (\phi_{\mathrm{cnl,Si}} - \phi_{\mathrm{cnl,d}}) + \phi_{\mathrm{Si}}, \quad (8)$$

in which $\phi_{\mathrm{cnl,d}} = 0 - E_{\mathrm{cnl,d}}$ and $\phi_{\mathrm{cnl,Si}} = 0 - E_{\mathrm{cnl,Si}}$ are the charge neutrality levels of the dielectric and ploycrystalline silicon with respect to the vacuum level. Consequently, the pinning factor $S_{\mathrm{m/Si}}$ of a metal or ploycrystalline silicon gate can be described by

$$S_{\mathrm{m/Si}} = \frac{2k_{\mathrm{d}} - \Delta k_{v/\mathrm{Si}} \cdot (\mathrm{e}^{\sqrt{b_{\mathrm{dm/Si}}} d_{\mathrm{dm/Si}}} + \mathrm{e}^{-\sqrt{b_{\mathrm{dm/Si}}} d_{\mathrm{dm/Si}}})}{a_{\mathrm{m/Si},+} \cdot \mathrm{e}^{\sqrt{b_{\mathrm{dm/Si}}} d_{\mathrm{dm/Si}}} + a_{\mathrm{m/Si},-} \cdot \mathrm{e}^{-\sqrt{b_{\mathrm{dm/Si}}} d_{\mathrm{dm/Si}}} - 2\Delta k_{v/\mathrm{Si}}}, \quad (9)$$

where

$$a_{\mathrm{m/Si},\pm} = \left(k_{\mathrm{d}} \pm \sqrt{\frac{D_{\mathrm{dm/Si}}}{D_{\mathrm{m/Si}}}} \cdot \sqrt{k_{\mathrm{d}} k_{v/\mathrm{Si}}} \right)$$

and $b_{\mathrm{m/Si}} = \mathrm{e}^2 D_{\mathrm{dm/Si}} / \varepsilon_{\mathrm{d}}$ are the parameters associated with materials dielectric, k_{d} and $k_{v/\mathrm{Si}}$ are the relative permittivity of the high-k and vacuum or ploycrystalline silicon, and $\Delta k_{v/\mathrm{Si}} = (k_{\mathrm{d}} - k_{v/\mathrm{Si}})$ is the relative permittivity difference between the high-k and vacuum or ploycrystalline silicon.

3. Results and discussion

In order to obtain an insight into the role of the electron state density and the interface state density, we calculate pinning factors S_{m} and S_{Si} by deriving Eq. (9) with the value of high-k dielectric Al_2O_3, in which the elementary charge is $e \sim 1.6 \times 10^{-19}$ C, the relative permittivity $k_v \sim 1$, the interface thickness $d_{\mathrm{m/Si}} \sim 0.25$ nm,[17] the relative permittivity $k_{\mathrm{d}} \sim 9$, and charge neutrality level $\phi_{\mathrm{cnl,d}}$ of $Al_2O_3 \sim 4.3$ eV. Figure 2(a) demonstrates that the Fermi-level pinning and effective work function of metal are influenced largely by the density of interface states D_{dm} at the metal–dielectric interface and the electron state density D_{m} of the metal gate. With the increase of D_{dm}, the pinning factor S_{m} decreases rapidly from 1 to negative and then tends toward zero. A transition interface state density D_{dm0} would make $S_{\mathrm{m}} \sim 0$ before perfect pinning, which only depends on the permittivity of dielectric. In the MIGS model, the Fermi-level in the interface cannot pass over the charge neutrality level, so that pinning factor S_{m} would not be negative.[17] However, when D_{dm} is greater than the transition density D_{dm0}, the S_{m} derived from our model becomes negative because of the larger relative permittivity of dielectrics than that of metals ($k_v \sim 1$). The negative S_{m} has also been observed physically on narrow gap semiconductors and experimentally on MoS_2.[17,18] Additionally, the metal with higher electron state density D_{m} has a larger range of S_{m}, implying the weaker pinning of metal work function toward $\phi_{\mathrm{cnl,d}}$. The linear relationships between calculated effective metal work function and vacuum metal work function are illustrated in Fig. 2(b) with $D_{\mathrm{m}} \sim 10^{23}$/eV·cm^3 and different values of D_{dm}. The effective work function approximately equals vacuum work function with a small interface state density. Increasing the interface state density D_{dm} makes the slope of $\phi_{\mathrm{m,eff}}$ decrease positively and then increase negatively. The scope of $\phi_{\mathrm{m,eff}}$ is also reduced. This suggests that the effective metal work function will be pinned at the charge neutrality level of Al_2O_3 eventually, which is independent of the vacuum metal work function. This tendency is consistent with the metal pinning factor curve in Fig. 2(a). Furthermore, the intersection in Fig. 2(b) shows $\phi_{\mathrm{m,eff}} = \phi_{\mathrm{m}} = \phi_{\mathrm{cnl,d}} \sim 4.3$ eV for Al_2O_3, and the intersection is only influenced by the high-k dielectric layer, no matter what the change of D_{dm} is.

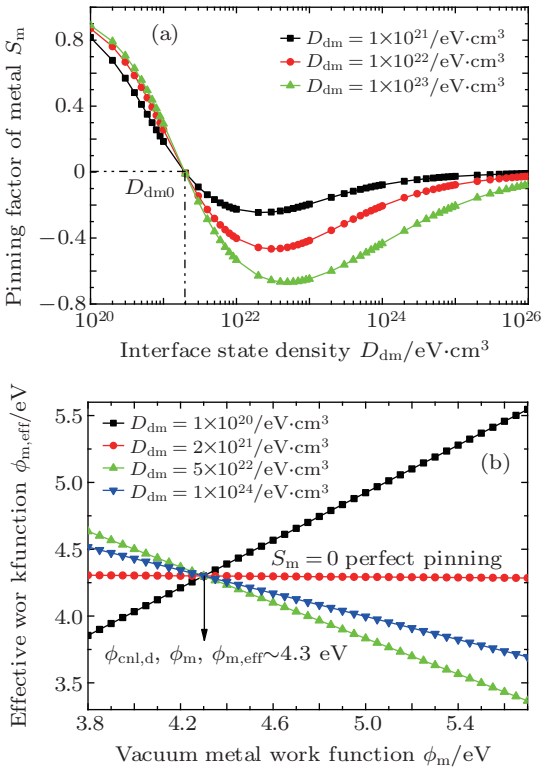


Fig. 2. (color online) (a) Pinning factors of metal S_{m} versus interface state density D_{dm} for different values of D_{m}. The large D_{dm} enables S_{m} to be pinned at zero. (b) Effective work functions versus vacuum metal work function for different values of D_{dm}. The smaller S_{m} leads to more pinning of $\phi_{\mathrm{m,eff}}$ to $\phi_{\mathrm{cnl,d}}$, as plotted in the $\phi_{\mathrm{m,eff}}$–ϕ_{m} diagram.

The pinning factor S_{Si} of ploycrystalline silicon–Al_2O_3 is plotted as a function of D_{dSi} and D_{Si} in Fig. 3(a). S_{Si} changes rapidly from 1 to 0 with the increase of the interface state density D_{dSi}, while increasing the electron state density of ploycrystalline silicon D_{Si} has much less influence. The effective work function of ploy-Si, $\phi_{\mathrm{Si,eff}}$, derived by Eq. (8) should be close to ϕ_{Si} as $S_{\mathrm{Si}} \sim 1$. The ploycrystalline silicon-Al_2O_3

stack with $S_{Si} \sim 0$ would tend to pin $\phi_{Si,eff}$ more effectively to $\phi_{cnl,Si} - \phi_{cnl,d} + \phi_{Si}$, which is the Fermi-level pinning position for ploycrystalline silicon. Yet for ploycrystalline silicon–HfO_2 ($\phi_{cnl,d} \sim 4.7$ eV), the more negative S_{Si} in Fig. 3(b) shows that the curve change is similar to the metal pinning factor curve in Fig. 2(a). The reason for this is that the relative permittivity of HfO_2 ($k_d \sim 20$) is larger than that of Si ($k_{Si} \sim 11.9$) while the relative permittivity of Al_2O_3 ($k_d \sim 9$) is smaller than that of Si.

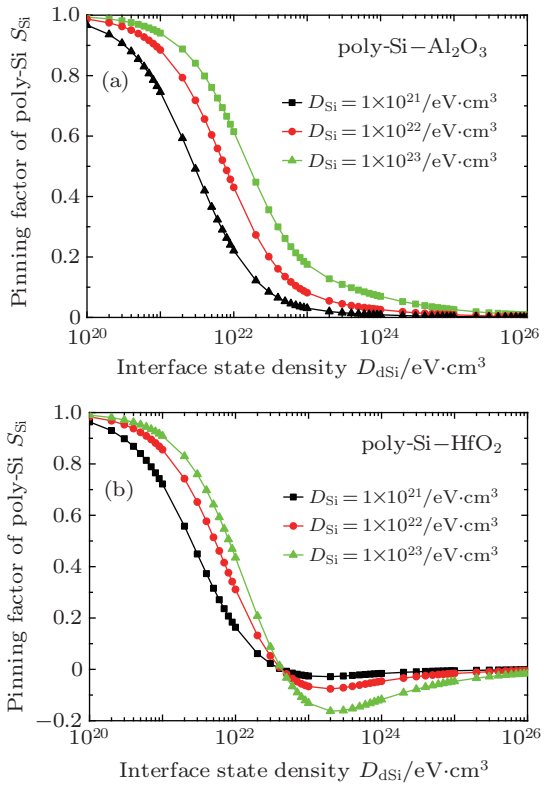


Fig. 3. (color online) (a) Plots of semiconductor pinning factor S_{Si} for ploycrystalline silicon–Al_2O_3 versus interface state density D_{dSi} with various values of D_{Si}. The large D_{dSi} enables S_{Si} to be pinned at 0. (b) Plots of pinning factor of poly-Si S_{Si}versus interface state density D_{dSi}. S_{Si} for ploycrystalline silicon–HfO_2 become negative with the large D_{dSi}.

Recently, fully silicided metal silicides such as NiSi and Hf-silicide have been intensively evaluated as an alternative to metal gates due to their CMOS compatibility with polycrystalline silicon gate process and no process-induced damage to the gate dielectric. Moreover, a full silicidation gate can eliminate the ploycrystalline silicon depletion and enhance carrier mobility.[19–21] Furthermore, the rare earth silicide gate materials have been used to reduce the Schottky barrier height because the pinning factors of rare earth silicide gates are steeper than those of the pure metal gates.[22–24] Experimental data and *ab-initio* calculations have indicated that metal silicide gates such as NiSi, $HfSi_2$, and $PdSi_2$ have weaker Fermi level pinning than the pure metal gates.[25,26] The pinning factor S_{m-Si} of NiSi–Al_2O_3 as a function of the interface state density D_{dm-Si} and electron state density D_{m-Si} is calculated by Eq. (9). Since the relative permittivity of NiSi ($k_{NiSi} \sim 24.74$) is larger than that of Al_2O_3,[26] the values of S_{m-Si} are positive. As shown in Fig. 4, S_{m-Si} changes rapidly from 1 to 0 with the increase of D_{dm-Si}, which is similar to the pinning factor of ploycrystalline silicon in Fig. 3(a). We can observe from Figs. 2(a), 3(a), and 4 that the values of the pinning factor for metal–Al_2O_3, ploycrystalline silicon–Al_2O_3, and NiSi–Al_2O_3 interfaces are ~ 0.293, ~ 0.940, and ~ 0.995 respectively when $D_m = D_{Si} = D_{m-Si} \sim 10^{23}$/eV·cm^3 and $D_{dm} = D_{dSi} = D_{dm-Si} \sim 10^{21}$/eV·cm^3. The pinning factors of a metal gate are much smaller than those of a metal silicide gate and a ploycrystalline silicon gate, which leads to a higher degree of pinning of metal Fermi level. This also holds true for other state densities.

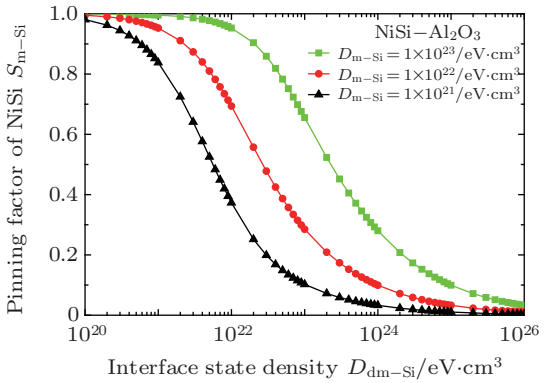


Fig. 4. (color online) Plots of pinning factor of metal silicide S_{m-Si} versus interface state density D_{m-Si} for NiSi–Al_2O_3 with various values of D_{dm-Si}.

Table 1 summarises some of the basic physical parameters for dielectrics, including relative permittivity k, energy band gap E_g, electron affinity χ, the extracted $(E_{cnl} - E_v)$ values, and charge neutrality level ϕ_{cnl} measured from the vacuum level. The band gap for high-k dielectric is known from the ellipsometry and absorption data.[27,28] The electron affinity of HfO_2 is 2.4 eV from Sayan *et al.*[29] The extracted $(E_{cnl} - E_v)$ values of Al_2O_3, HfO_2, ZrO_2 are obtained by using the tight-binding method given by Robertson.[27,28] The extracted $(E_{cnl} - E_v)$ values of Si_3N_4 is 2.6 eV given by Xu and Ching.[30] The charge neutrality levels of dielectrics in Table 1 are deduced from $\phi_{cnl} = \chi + E_g - (E_{cnl} - E_v)$ according to the energy band gap E_g, electron affinity χ, and the extracted $(E_{cnl} - E_v)$ values. Figure 5 shows the effective work functions of these three gates on various dielectrics versus the relative permittivity of dielectrics with parameters of Table 1. It can be observed that the changes of effective work functions are compared for different metal–dielectric stacks with $\phi_m = 4.05$ eV, n^+ ploycrystalline silicon–dielectric stacks with $\phi_{Si} = 4.05$ eV, and metal silicide–dielectric stacks with $\phi_{m-Si} = 4.00$ eV ($HfSi_2$, $k \sim 20.56$).[26] As shown in Fig. 5, the metal gate tends to pin their effective work function to ϕ_{cnl} of the dielectrics, while the effective work functions

of ploycrystalline silicon gate and metal silicide gate wave around their vacuum work functions. This implies that the metal gate is more susceptible to interface state than a ploycrystalline silicon gate or a metal silicide gate. This is also true for metal–dielectric stacks with $\phi_{\rm m} = 5.17$ eV, p^+ ploycrystalline silicon–dielectric stacks with $\phi_{\rm Si} = 5.17$ eV, and metal silicide–dielectric stacks with $\phi_{\rm m-Si} = 5.16$ eV (NiSi, $k \sim 24.74$). Since a metal silicide gate has advantages, including high-temperature resistant and low resistivity at the same time, it would be a more appropriate option for designing gate materials in MOS technology.

Table 1. Basic physical parameters for several dielectrics.

Materials	k	$E_{\rm g}$/eV	χ/eV	$E_{\rm cnl} - E_{\rm v}$/eV	$\phi_{\rm cnl}$/eV	Reference
Si	11.90	1.12	4.05	0.36	4.81	[27], [28]
Ge	16.00	0.66	4.13	0.18	4.61	[27], [28]
SiO_2	3.90	9.00	0.95	4.50	5.45	[27], [28]
Si_3N_4	7.50	5.30	2.10	2.60	4.80	[27], [28], [30]
Al_2O_3	9.00	8.80	1.00	5.50	4.30	[27], [28]
HfO_2	20.00	6.00	2.40	3.70	4.70	[27], [28], [29]
ZrO_2	25.00	5.80	2.50	3.60	4.70	[27], [28]

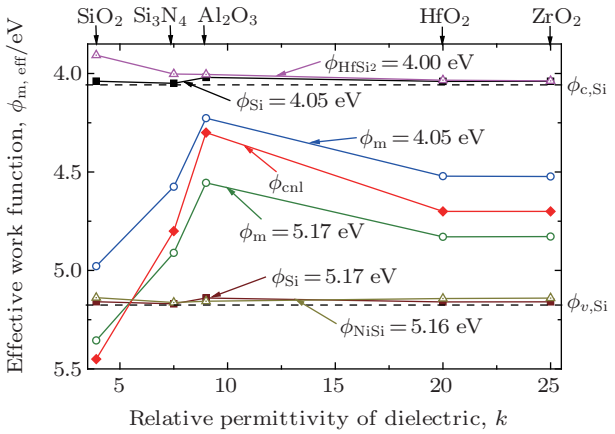


Fig. 5. (color online) Effective work functions of ploycrystalline silicon gate, metal gate, and metal silicide gate on various dielectric layers versus the relative permittivity of dielectric with $D_{\rm m} = D_{\rm Si} \sim 10^{23}$/eV·cm^3 and $D_{\rm dm} = D_{\rm dSi} \sim 10^{21}$/eV·cm^3.

4. Conclusions

In this paper, the dependences of the Fermi-level pinning effect on the electron state density and the interface state density are studied by comparing the metal–dielectric, ploycrystalline silicon–dielectric, and metal silicide–dielectric interfaces. The relation curves of the pinning factors with the electron state density and interface state density can reflect the Fermi-level pinning effect intuitively. The Fermi-level pinning factors and effective work functions of the metal–dielectric interfaces are observed to be significantly different, with increasing interface state density, from those of ploycrystalline silicon–dielectric interface and metal silicide–dielectric interface, implying that the metal gate is more susceptible to the interface states than a ploycrystalline silicon gate and a metal silicide gate. The calculation results indicate that a metal silicide gate would be a more appropriate option for designing the gate materials in MOS technology.

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