GaSb p-channel metal-oxide-semiconductor field-effect transistor and its temperature dependent characteristics*

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GaSb p-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) with an atomic layer deposited Al_2O_3 gate dielectric and a self-aligned Si-implanted source/drain are experimentally demonstrated. Temperature dependent electrical characteristics are investigated. Different electrical behaviors are observed in two temperature regions, and the underlying mechanisms are discussed. It is found that the reverse-bias pn junction leakage of the drain/substrate is the main component of the off-state drain leakage current, which is generation-current dominated in the low temperature regions and is diffusion-current dominated in the high temperature regions. Methods to further reduce the off-state drain leakage current are given.

Keywords: GaSb, metal-oxide-semiconductor field-effect transistor, temperature dependent characteristics, drain leakage current

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1. Introduction

As silicon based transistor scaling is now close to its physical limits, III–V compound semiconductors have attracted lots of attention for replacing silicon as the channel materials, due to their excellent carrier transport properties.[1,2] Although most III–V compound semiconductors have very high electron mobility, such as GaAs, InAs, and InGaAs,[3,4] their hole mobility is relatively low. GaSb has very high hole mobility (~ 1000 cm$^2\cdot$V$^{-1}\cdot$s^{-1}), making it attractive as an alternative to silicon for channel material, especially for the application in the p-channel metal-oxide-semiconductor field-effect transistor (MOSFET).[1,5] Many efforts have been made to enable GaSb MOSFET applications, in such areas as source/drain technology[6,7] and interface passivation techniques.[8–10] However, technologies for GaSb MOSFET application have not been fully developed yet. Although there are some reports on GaSb MOSFETs,[11,12] studies of the characteristics of GaSb MOSFETs are still far from sufficient. Modern integration circuits usually operate at elevated temperatures, due to the power dissipation of the circuit.[13] Consequently, investigations of the temperature dependent electrical characteristics of MOSFETs are of great importance. Although there are studies of temperature dependent characteristics of devices fabricated with other materials,[14] the temperature dependent characteristics of GaSb MOSFETs have not been investigated yet. In this paper, GaSb p-channel MOSFETs with an atomic layer deposited Al_2O_3 gate dielectric and a self-aligned Si-ion-implanted source/drain are experimentally demonstrated. Temperature dependent electrical characteristics of the fabricated GaSb p-channel MOSFETs are systematically investigated. The fabricated GaSb MOSFETs show different electrical characteristic behaviors in two temperature regions. The mechanisms of the off-state drain leakage current ($I_{\rm off}$) are discussed, and methods to further reduce $I_{\rm off}$ are given.

2. Experimental

Figure 1(a) shows the cross-sectional schematic of a GaSb p-channel MOSFET structure fabricated in this work. GaSb p-channel MOSFETs were fabricated using a self-aligned gate-first process flow. Two-inch Te-doped n-type GaSb (100)-oriented wafers with a doping concentration of $(4–8)\times10^{16}$ cm^{-3} were used as starting substrates for MOSFET fabrication. After initial surface cleaning by sequential immersion for 5 min each in acetone, ethanol, and isopropanol, and for 1 min in 9% HCl aqueous solution, the substrates were passivated by 20% $(NH_4)_2S$ aqueous solution for 15 min. After that, a 10-nm Al_2O_3 dielectric layer was deposited by atomic layer deposition (ALD) at 200 °C using a Beneq TFS 200 ALD system. Trimethylaluminum (TMA) and water were used as precursors. Ni/Au gate metal was then deposited and patterned using a lift-off process. Research has shown that Si dopant ions act as acceptors in GaSb, which makes the material suitable for the formation of p^+ regions for the source/drain in the n-type substrate.[11,12] Thus, the source and drain regions were selectively implanted using Si ions with an implant dose of 2×10^{14} cm^{-2} at 30 keV. Rapid thermal annealing at 650 °C for 30 s was performed for dopant activation. After removing the Al_2O_3 encapsulation layer by 30% KOH/isopropanol aqueous solution, the source and drain

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metals were deposited and patterned by electron beam evaporation of Ni/Au using a lift-off process. Figure 1(b) shows a microscopic image of the fabricated GaSb MOSFETs. The gate length of these MOSFETs is 10 μm. Temperature dependent electrical characteristics were recorded using an Agilent B1500A semiconductor device analyzer and a Cascade Summit 11000 AP probe system.

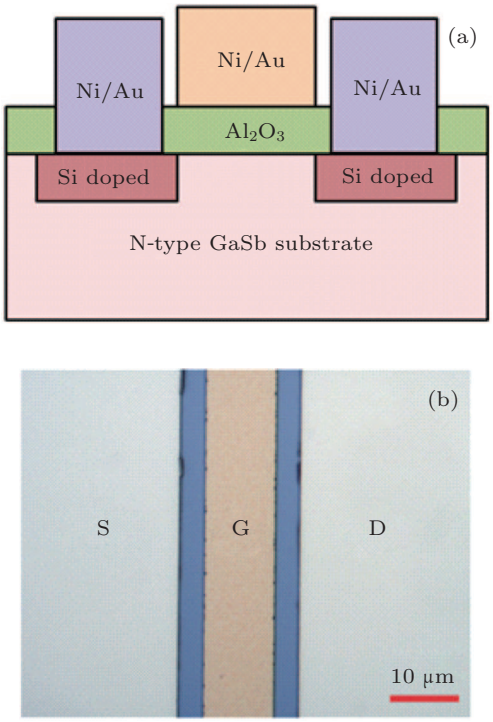


Fig. 1. (color online) (a) Cross-sectional schematic of the fabricated GaSb p-channel MOSFET structure. (b) Microscopic image of a fabricated GaSb p-channel MOSFET.

3. Results and discussion

Figure 2 shows the transfer characteristics of the MOSFETs. The I_{on}/I_{off} ratios, as large as ~ 450, are determined from the drain current I_d with drain bias V_d at -1 V. The threshold voltage V_t was determined as -0.325 V from the transfer characteristics measured at $V_d = -50$ mV, using the linear extrapolation method.[15] Low V_t is favorable in modern integrated circuits, especially for low power applications. The subthreshold swing (SS) of the device at $V_d = -50$ mV is ~ 880 mV/dec. The inset of Fig. 2 shows the gate leakage current characteristics of the samples. For comparison purposes only, gate leakage current is divided by gate width. Compared with the transfer characteristics at $V_d = -50$ mV, the gate leakage current is more than 3 orders of magnitude smaller than the off-state drain current at $V_g = 1$ V, which means the gate leakage current is not a main contributor to the off-state drain leakage current. Figure 3 shows the dc output characteristics of the MOSFETs. Maximum drain current I_d of ~ 1.1 mA/mm is obtained at a gate bias $V_g = -4$ V and a drain bias $V_d = -2.5$ V.

Temperature dependent electrical characteristics of the MOSFETs are also investigated. Figure 4 shows typical transfer characteristics of the MOSFETs for temperatures ranging from 240 K to 390 K at $V_d = -1$ V. As temperature increases, on-state drain current increases slightly, due to the change in V_t. According to semiconductor device physics theory, dV_t/dT is positive for p-channel MOSFETs,[16] which can also be clearly seen in Fig. 4. The MOSFET drain current I_d in the saturation region can be expressed as $I_d \propto \mu(T)\left(V_g - V_t(T)\right)^2$. When temperature increases, the increase of the drain current by the increase of $\left|V_g - V_t\right|$ surmounts the mobility degradation. Similar findings are also reported by other researchers.[17] On the other hand, as temperature increases, the off-state drain leakage current I_{off} increases dramatically, greatly influencing the performance of these MOSFETs. When the device operates at 240 K, I_{off} is as small as $\sim 10^{-4}$ mA/mm. When the device operates at 390 K however, I_{off} increases by about three orders of magnitude, reaching $\sim 10^{-1}$ mA/mm. As temperature increases, the significant increase in I_{off} leads to a marked deterioration in I_{on}/I_{off} ratio characteristics. Figure 5 shows the temperature dependent I_{on}/I_{off} ratio characteristics of the MOSFETs. The I_{on}/I_{off} ratio decreases from ~ 4000 at 240 K to ~ 450 at room temperature (300 K) and to less than 20 at 390 K.

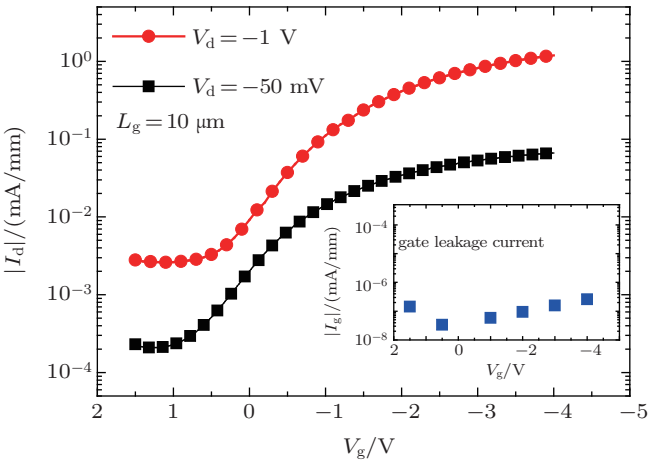


Fig. 2. (color online) Transfer (I_{ds}–V_{gs}) characteristics of the fabricated GaSb p-channel MOSFETs. The inset shows the gate leakage current characteristics of the samples.

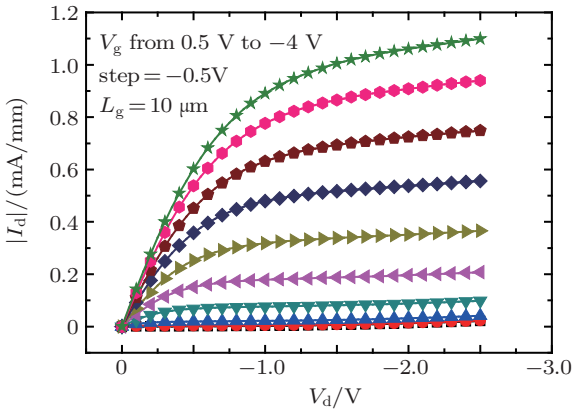


Fig. 3. (color online) Output (I_{ds}–V_{ds}) characteristics of the fabricated GaSb p-channel MOSFETs.

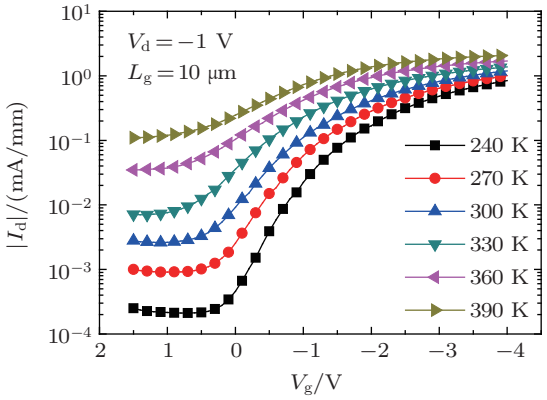


Fig. 4. (color online) Temperature dependent transfer (I_{ds}–V_{gs}) characteristics of the fabricated GaSb p-channel MOSFETs.

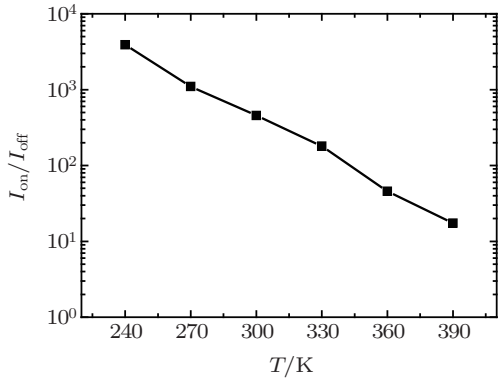


Fig. 5. Temperature dependent I_{on}/I_{off} ratio characteristics of the fabricated GaSb p-channel MOSFETs.

The temperature dependent off-state drain leakage current has a great influence on the performance of these MOSFETs. Consequently, investigations of the mechanism of the off-state drain leakage current are of great importance. Many factors can contribute to I_{off}, such as the reverse-bias pn junction leakage of the drain/substrate, the gate-induced drain leakage, and the channel punch-through current. In long-channel devices, I_{off} is dominated by leakage from the reverse-bias pn junctions of the drain/substrate,[13] and this is especially pronounced for the devices designed in this work, which have large source/drain regions. Figure 6 shows the off-state drain leakage current versus measurement temperature curve. It can be clearly seen that I_{off} increases with rising temperature, and the $\lg(I_{off})$ is linear to $1/T$, with different slopes in two temperature regions. The slope of the curve in the temperature region from 330 K to 450 K is steeper than that of the curve in the temperature region from 220 K to 330 K. Hereafter we refer to these two temperature regions as the high temperature region and the low temperature region, respectively. The difference in curve slopes in the two temperature regions indicates two different leakage current mechanisms. I_{off} is diffusion-current dominated in the high temperature region, and is generation-current dominated in the low temperature region. This explanation is confirmed by the temperature dependent measurements and by Shockley–Read–Hall (SRH) generation-recombination theory, as discussed below.

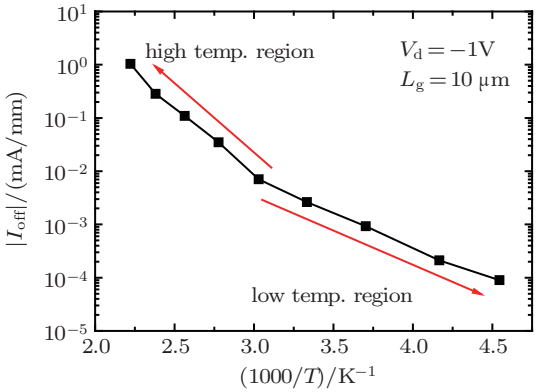


Fig. 6. (color online) Temperature dependent off-state drain leakage current characteristics of the fabricated GaSb p-channel MOSFETs.

According to the Shockley–Read–Hall (SRH) generation-recombination theory,[16,18] the current of the reverse-biased pn junction consists of two components: the diffusion current J_{dA} and the generation current J_{gA}, which can be written as follows:

$$J_{dA} = qn_i^2 \frac{D_n}{L_n N_A}, \tag{1}$$

$$J_{gA} = \frac{qn_i W_A}{\tau_g}, \tag{2}$$

where q is elementary charge, n_i the intrinsic carrier concentration, D_n the diffusion coefficient of electrons in the p side, W_A the volume depletion width, τ_r the recombination lifetime, τ_g the generation lifetime, and $L_n = \sqrt{D_n \tau_r}$ is the electron diffusion length.

Given $n_i \propto \exp\left(-E_g/2kT\right)$ and $\tau_g = \tau_r \exp\left(|E_t - E_i|/kT\right)$, J_{dA} and J_{gA} should be given by

$$J_{dA} \propto \exp\left(-\frac{E_g}{kT}\right), \tag{3}$$

$$J_{gA} \propto \exp\left(-\frac{E_t}{kT}\right), \tag{4}$$

where E_g is the band gap and E_t is the trap energy level. Since E_t is smaller than E_g, the slope of an Arrhenius plot of I_{off} versus $1/kT$ should be larger when I_{off} is diffusion-current dominated than that when I_{off} is generation-current dominated.

Figures 7(a) and 7(b) plot the $\ln(I_{off})$ versus $1/kT$ curves in the high temperature region and low temperature region, respectively. The slopes of the curves are extracted as -0.52 and -0.252 respectively, within reasonable standard errors. The finding that the slope of the curve in the high temperature region is steeper than that of the curve in the low temperature region confirms that I_{off} is diffusion-current dominated in the high temperature region and is generation-current dominated in the low temperature region. The slope of -0.52 in the high

temperature region is smaller than the band-gap E_g of GaSb, which is due to the simultaneous influence of the generation current component.

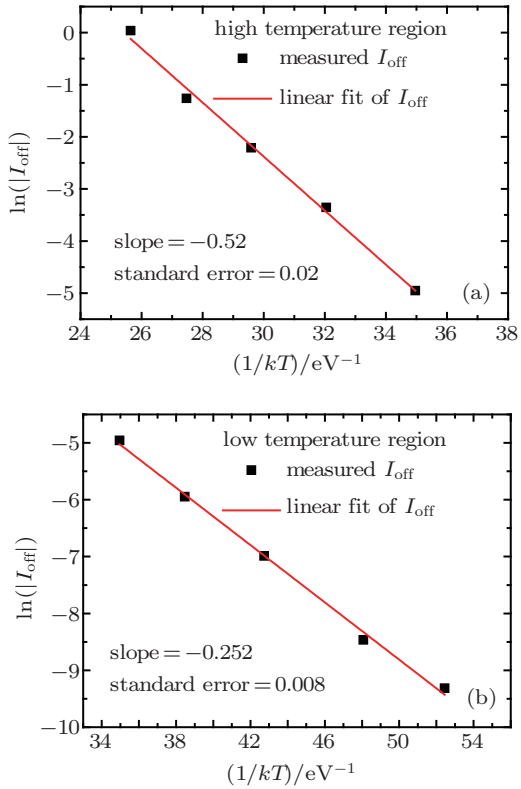


Fig. 7. (color online) (a) Off-state drain leakage current in the high temperature regions. (b) Off-state drain leakage current in the low temperature regions.

In long-channel devices, the reverse-bias pn junction leakage of the drain/substrate is a main contributor to the off-state drain leakage current.[13] To obtain a low off-state drain leakage current, special attention should be given to the ion-implanted source/drain regions. For example, the sectional area of the drain/substrate pn junction should be kept small. Another method to reduce the off-state drain leakage current is to increase the generation/recombination lifetime of the minority carriers in the drain/substrate pn junctions, which can be achieved by reducing the number of defects present in the pn junctions. Since modern integrated circuits usually operate at elevated temperatures and I_{off} is diffusion-current dominated in the high temperature region, increasing the recombination lifetime is more important than increasing the generation lifetime.

4. Conclusions

In conclusion, we have experimentally demonstrated GaSb p-channel MOSFETs with an atomic layer deposited Al_2O_3 gate dielectric and a self-aligned Si-ion-implanted source/drain. Temperature dependent characteristics of the MOSFETs were investigated. The mechanism of the off-state drain leakage current was analyzed. It is found that the reverse-bias pn junction leakage of the drain/substrate is a main contributor to the off-state drain leakage current, which is generation-current dominated in the low temperature region and is diffusion-current dominated in the high temperature region. Methods to further reduce the off-state drain leakage current are given.

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