An analytic model for gate-all-around silicon nanowire tunneling field effect transistors*

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An analytical model of gate-all-around (GAA) silicon nanowire tunneling field effect transistors (NW-TFETs) is developted based on the surface potential solutions in the channel direction and considering the band to band tunneling (BTBT) efficiency. The three-dimensional Poisson equation is solved to obtain the surface potential distributions in the partition regions along the channel direction for the NW-TFET, and a tunneling current model using Kane's expression is developed. The validity of the developed model is shown by the good agreement between the model predictions and the TCAD simulation results.

Keywords: gate-all-round nanowire tunneling field effect transistor, band to band tunneling, analytic model

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1. Introduction

Tunneling field effect transistors (TFETs) have received much attention in the semiconductor academic research and industry fields for their superior performance in the sub-threshold region. Compared with the conventional metal–oxide–semiconductor field-effect transistors (MOSFETs), the TFETs are competitive and chosen due to their high ON-OFF current ratio, below 60 mV/dec sub-threshold swing (SS), and low leakage power consumption.[1–5] However, the TFETs have a small band to band tunneling (BTBT) efficiency in the large band gap of silicon, leading to a low ON current. To obtain a high ON current and a small SS, the gate-all-around (GAA) silicon nanowire TFET (NW-TFET) is considered. In recent years, since the NW-TFET process technology and fabrication methods have become mature, many research papers have been published.[6–8] However, the compact model of NW-TFET for circuit performance prediction and simulation has made little progress. Most works only focus on the NW-TFET empirical model development.[6,9–12] So far, there is no complete analytical model of GAA NW-TFET for device scientists and circuit designers to test and simulate such a device.

In this paper, an analytical model of GAA silicon NW-TFET is developed based on the three-dimensional (3D) potential solution and Kane's expression. For studying the validity of the model and observing the impact of the different structure parameters on the device performance, we also compare the analytical model prediction with the TCAD SenTaurus simulation results.

2. Structure and model

2.1. Structure of GAA NW-TFETs

Figure 1 shows the structure of a GAA TFET with a silicon nanowire body. As is shown in Fig. 1(a), the source electrode length is L_s (10 nm), the drain electrode length is L_d (10 nm), the gate electrode length is L_g (50 nm), the oxide (SiO_2) thickness is t_{ox}, and the channel radius is R. Figure 1(b) shows the cross-section of the n-channel device. In this paper, the n-TFET is considered, the doping profile along the axis direction of the nanowire is p^+ doping in the source ($N_s = 10^{20}$ cm^{-3}), intrinsic doping in the channel ($N_{ch} = 10^{10}$ cm^{-3}), and n^+ doping in the drain ($N_d = 10^{20}$ cm^{-3}). Band to band tunneling (BTBT) occurs in the P–N junction at the source–channel region. According to the drift-diffusion (DD) theory, the electrons move toward the drain, thus the device can be divided into three regions: the depletion region I ($-L_1 \le x < 0$), the tunneling region II ($0 \le x < L_2$), and the remaining channel region III ($L_2 \le x \le L_g$).

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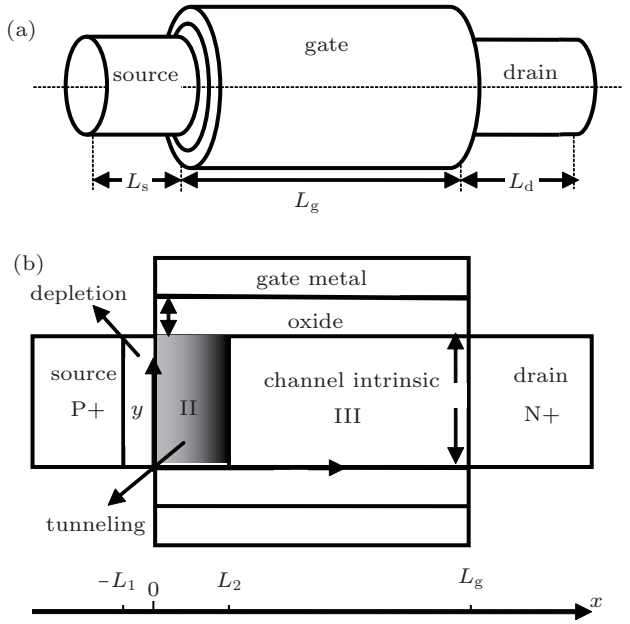


Fig. 1. (a) The 3D structure of an n-channel GAA silicon NW-TFET. (b) Cross-section of the device and the division into a depletion region (I), a tunneling region (II), and a conventional GAA MOSFET region (III).

The energy band with electron and hole quasi-Fermi energies along the x direction from the device simulator TCAD SenTaurus is demonstrated in Fig. 2. The structure parameters of the device are $t_{ox} = 2$ nm, $R = 5$ nm, and $N_s/N_d = 10^{20}$ cm^{-3} as used in a typical example. Figure 2 suggests that the surface potential of the GAA NW-TFET along the channel direction can be solved separately in the divided regions.

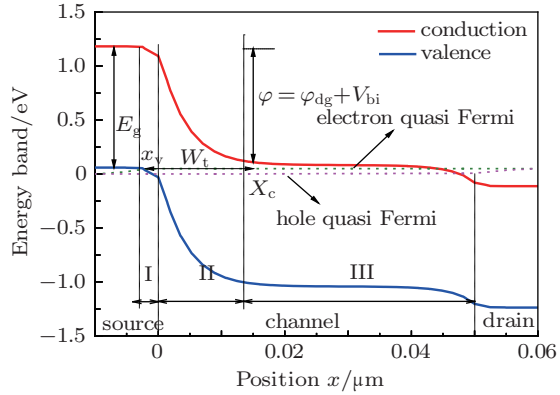


Fig. 2. (color online) Energy band diagram with electron and hole quasi-Fermi energies along the x direction from TCAD Sentaurus device simulation.

2.2. Potential distribution model

Only the depletion charge is considered in the subthreshold region as discussed above, thus the Poisson equation can be written as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \varphi(r,x)}{\partial r}\right)+\frac{\partial^2 \varphi(r,x)}{\partial x^2}=\frac{qN_i}{\varepsilon_{Si}}, \tag{1}$$

where $\varphi(r,x)$ is the two-dimensional (2D) potential, N_i are the different doping densities in the partition regions, and ε_{Si} is the silicon dielectric constant. In Eq. (1), r varies from zero to R ($0 \le r \le R$), and x varies from the source to the drain ($-L_s \le x \le L_d$). Since the potential is parabolic in the radius direction, it can be solved using the 2D polynomial approximation[11,13,14]

$$\varphi(r,x) = d_0(x)+d_1(x)r+d_2(x)r^2. \tag{2}$$

The parameters in Eq. (2) are obtained by using the following assumptions.

i) At the interface between the SiO_2 oxide and the silicon nanowire,

$$\varphi(R,x) = \varphi_s(x). \tag{3}$$

ii) The electric flux must be continuous between the surrounding gate oxide and the silicon nanowire,

$$\varepsilon_{Si}\frac{\partial \varphi(r,x)}{\partial r}|_{r=R} = C_{ox}[V_{gs}-V_{fb}-\varphi_s(x)], \tag{4}$$

where C_{ox} is the capacitance of the gate oxide, $C_{ox} = \varepsilon_{ox}/R\ln(1+t_{ox}/R)$.

iii) At the centre of the channel ($r = 0$), the electric field is zero because the potential is symmetrical along the radius direction,

$$\left.\frac{\partial \varphi(r,x)}{\partial r}\right|_{r=0} = 0. \tag{5}$$

Thus the solution of Eq. (2) is obtained as

$$\varphi(r,x) = \varphi_c(x)+\frac{C_{ox}(V_{gs}-V_{fb}-\varphi_s(x))}{2\varepsilon_{Si}R}r^2, \tag{6}$$

where $\varphi_c(x)$ and $\varphi_s(x)$ are the center and the surface potentials in the channel direction, respectively, and the relationship between them is

$$\varphi_s(x) = \varphi_c(x)+\frac{2C_{ox}R(V_{gs}-V_{fb}-\varphi_s(x))}{\varepsilon_{Si}}. \tag{7}$$

In this paper, we consider the surface potential $\varphi_s(x)$ in the channel direction using the Wenzel Kramer Brillouin (WKB) approximation of the inter-band tunneling probability.[9] It is assumed that the GAA silicon NW-TFET can be described by a modified Poisson equation, generating a characteristic length scale λ for the surface potential variation.[10,15] From Eqs. (1)–(5), the modified Poisson equation is acquired as

$$\frac{\partial^2 \varphi_s(x)}{\partial x^2}+\frac{\varphi_s(x)}{\lambda^2} = \eta, \tag{8}$$

where

$$\eta = \frac{qN_i}{\varepsilon_{Si}}-\frac{V_{gs}-V_{fb}}{\lambda^2},$$

and $\lambda = \varepsilon_{Si}R/2C_{ox}$ is the characteristic length of the GAA NW-FET. The general solution of Eq. (8) is

$$\varphi_s(x) = C_A\exp\left(\frac{x}{\lambda}\right)+C_B\exp\left(-\frac{x}{\lambda}\right)-\lambda^2\eta. \tag{9}$$

In region I ($-L_1 \le x < 0$), it is assumed that the region is fully depleted, and the equivalent gate oxide thickness is $t'_{ox} = \pi t_{ox}/2$ for the gate fringing field.[10,16,17] So

$$\varphi_{s1}(x) = C_A \exp\left(\frac{x}{\lambda_1}\right) + C_B \exp\left(-\frac{x}{\lambda_1}\right) - \lambda_1^2 \eta_1. \quad (10)$$

By using the Taylor expansion and the equivalent t'_{ox} in the source region, the equation is simplified to

$$\varphi_{s1}(x) \approx A_1\left(1 + \frac{x^2}{2\lambda_1}\right) - \lambda_1^2 \eta_1, \quad (11)$$

where

$$\lambda_1 = \sqrt{\frac{\varepsilon_{Si} R^2 \ln(1 + \pi t_{ox}/2R)}{2\varepsilon_{ox}}}$$

is the characteristic length of region I, and

$$\eta_1 = \frac{qN_s}{\varepsilon_{Si}} - \frac{V_{gs} - V_{fbs}}{\lambda_1^2}.$$

The boundary conditions for the solution of Eq. (11) are as follows.

i) At position $x = -L_1$, the surface potential is the silicon intrinsic voltage

$$\varphi_{s1}(-L_1) = -V_{bi}, \quad (12)$$

where V_{bi} is the built-in voltage of the source/channel junction.

ii) At position $x = -L_1$, the electric field is zero

$$E_{s1}(-L_1) = 0. \quad (13)$$

From Eqs. (11)–(13), the solution of the surface potential in region I is expressed as

$$\varphi_{s1}(x) = A_1(x + L_1)^2 - V_{bi}, \quad (14)$$

where $A_1 = qN_{seff}/2\varepsilon_{Si}$,

$$N_{seff} = 2\frac{\varepsilon_{Si}}{q}\left[\frac{qN_s}{2\varepsilon_{Si}} - \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \cdot \frac{V_{gs} - V_{fbs}}{R^2 \ln(1 + \pi t_{ox}/2R)}\right],$$

$V_{fbs} = W_{fg} - W_{fs}$ is the flat-band voltage, and W_{fg} and $W_{fs} = 4.05 + V_{bi}$ are the work functions. In Eq. (14), the value of L_1 is unknown.

In region II ($0 \le x < L_2$), the solution of Eq. (8) can be approximated as

$$\varphi_{s2}(x) = B_1 \exp\left(\frac{x}{\lambda_2}\right) + B_2 \exp\left(-\frac{x}{\lambda_2}\right) + V_{gs} - V_{fbs}, \quad (15)$$

where $\lambda_2 = \sqrt{\frac{\varepsilon_{Si} R^2 \ln(1 + t_{ox}/R)}{2\varepsilon_{ox}}}$ is the characteristic length of region II. The coefficients B_1 and B_2 can be calculated by making use of the following boundary conditions.

i) At position $x = -L_2$, the surface potential is

$$\varphi_{s2}(L_2) = V_{bi} + \varphi_{dg}. \quad (16)$$

ii) At position $x = -L_2$, the electric field is approximately zero

$$E_{s2}(L_2) = \left.\frac{\partial \varphi_{s2}(x)}{\partial x}\right|_{x=L_2} \approx 0. \quad (17)$$

With Eqs. (15)–(17), the surface potential of region II can be solved as

$$\varphi_{s2}(x) = (V_{gs} - V_{fbs}) - [V_{gs} - V_{fbs} - (V_{bi} + \varphi_{dg})] \times n \cosh\left(\frac{x - L_2}{\lambda_2}\right), \quad (18)$$

where length L_2 is also unknown. Then we need to find the values of L_1 and L_2 using the following boundary conditions between regions I and II:

$$\varphi_{s1}(0) = \varphi_{s2}(0), \quad (19)$$

$$\frac{\partial \varphi_{s1}(x)}{\partial x}|_{x=0} = \frac{\partial \varphi_{s2}(x)}{\partial x}|_{x=0}. \quad (20)$$

Eventually, the compact solutions of the potential model are obtained with the following values of L_1 and L_2:

$$L_1 = \sqrt{\frac{2\varepsilon_{Si}[\varphi_s(0) + V_{bi}]}{qN_{seff}}}, \quad (21)$$

$$L_2 = \lambda_2 \cosh^{-1}\left(-\frac{V_{gs} - V_{fbs}}{V_{gs} - V_{fbs} - V_{bi} - \varphi_{dg}}\right), \quad (22)$$

$$\varphi_s(0) = -[(V_{gs} - V_{fbs} - V_{bi} - \varphi_{dg})^2 + 2(V_{gs} - V_{fbs})\zeta + \zeta^2 + 2V_{bi}\zeta]^{1/2} + (V_{gs} - V_{fbs} + \zeta), \quad (23)$$

where $\varphi_s(0)$ stands for the surface potential at position $x = 0$, and $\zeta = qN_{seff}\lambda_2^2/\varepsilon_{Si}$ is an intermediate variable. By bringing L_1 and L_2, the lengths of regions I and II into Eqs. (14) and (18), we obtain the compact 2D analytical model of the potential distribution for the GAA silicon NW-TFET.

2.3. Analytic current model

Usually the BTBT is described using an introducing generation term in the drift and diffusion equation.[18] When the BTBT current is dominating, the total current can be calculated by summarizing the charge generated in the device

$$I_{ds} = q\int G \mathrm{d}V = q \cdot \pi R^2 \int G \mathrm{d}x, \quad (24)$$

where G is the generation rate of carriers per unit volume per unit time, and $\mathrm{d}V$ is an elementary volume of the device.

As shown in Fig. 2, the BTBT has different paths between the source and the body junction, and the tunneling points x_c and x_v vary on different paths, so the tunneling width $W_t = x_c - x_v$ must have a minimum value. The carrier generation rate due to the BTBT has a peak value G_{max} along the tunneling path, which has the minimum tunneling distance $W_{t,min}$ because of the largest tunneling probability.[19] The minimum tunneling width can be obtained with the following equations:

$$\begin{cases} \varphi_{s2}(x_c) = \phi_t, \\ \varphi_{s1}(x_v) = \phi_t - E_g/q, \\ \mathrm{d}W_t/\mathrm{d}\phi_t = 0, \end{cases} \quad (25)$$

where ϕ_t is the potential on the conduction band when the tunneling width is minimum, and E_g is the band gap. It is assumed that position x_v is in region I and x_c is in region II. From Eq. (25), the minimum tunneling width is

$$W_{\mathrm{t,min}} = L_2 + \lambda_2 \cosh^{-1}\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{fbs}} - \varphi_{\mathrm{t}}}{V_{\mathrm{gs}} - V_{\mathrm{fbb}} - \varphi_{\mathrm{dg}}}\right) - \sqrt{\frac{\phi_{\mathrm{t}} - E_{\mathrm{g}}/q + V_{\mathrm{bi}}}{A_1}} + L_1, \tag{26}$$

$$\phi_{\mathrm{t}} = (V_{\mathrm{gs}} - V_{\mathrm{fbs}}) + 2A_1\lambda_2^2 - \sqrt{(V_{\mathrm{gs}} - V_{\mathrm{fbb}} - \varphi_{\mathrm{dg}})^2 + (2A_1\lambda_2^2)^2 + 4A_1\lambda_2^2(V_{\mathrm{gs}} - V_{\mathrm{fbs}} - E_{\mathrm{g}}/q + V_{\mathrm{bi}})}. \tag{27}$$

With Kane's model,[20,21] the generation rate can be calculated as

$$G(E) = A\frac{E^D}{E_{\mathrm{g}}^{1/2}}\exp\left(-\frac{BE_{\mathrm{g}}^{3/2}}{|E|}\right), \tag{28}$$

where A and B are the parameters of Kane's model and depend on the effective mass of the valence and conduction bands. In this paper, $A = 3.5\times10^{21}\ \mathrm{eV}^{1/2}/(\mathrm{s}\cdot\mathrm{V}^2)$, $B = 22.5\times10^6\ \mathrm{V}/(\mathrm{cm}\cdot\mathrm{eV}^{3/2})$, and D takes a default value of 2.[22]

When the maximum electric field across the tunneling junction is approximated by $|E| = E_{\mathrm{g}}/(qW_{\mathrm{t,min}})$, the maximum carrier generation rate is obtained as

$$\begin{aligned} G_{\max} &= A\frac{E_{\mathrm{g}}^{3/2}}{q^2}\frac{1}{W_{\mathrm{t,min}}^2}\exp(-BqW_{\mathrm{t,min}}E_{\mathrm{g}}^{1/2}) \\ &= A\frac{E_{\mathrm{g}}^{3/2}}{q^2}\frac{1}{W_{\mathrm{t,min}}^2}\exp\left(-\frac{W_{\mathrm{t,min}}}{\lambda_{\mathrm{D}}}\right), \end{aligned} \tag{29}$$

where $\lambda_{\mathrm{D}} = 1/(BqE_{\mathrm{g}}^{1/2})$ is the tunneling decay length.

From the Kane model discussed above, it is observed that the generation rate is an exponential function depending on the linear tunneling width, so it can be assumed that the electron generation rate satisfies the following function:

$$G(x) = G_{\max}\exp\left(-\frac{|x - x_{\mathrm{c,min}}|}{\lambda_{\mathrm{D}}}\right). \tag{30}$$

As a consequence, equation (24) is easily computed as

$$\begin{aligned} \int_{-\infty}^{+\infty} G(x)\,\mathrm{d}x &= \int_{-\infty}^{+\infty} G_{\max}\cdot\exp\left(-\frac{|x - x_{\mathrm{c,min}}|}{\lambda_{\mathrm{D}}}\right)\mathrm{d}x \\ &= 2\lambda_{\mathrm{D}}G_{\max}, \end{aligned} \tag{31}$$

$$I_{\mathrm{ds}} = 2q\cdot\pi R^2\lambda_{\mathrm{D}}G_{\max}. \tag{32}$$

We then use a current correction factor F_{Fermi} produced from Landauer's formula to make sure that the tunneling current is zero when the drain voltage is zero[23]

$$F_{\mathrm{Fermi}} = 1 - 2\frac{1}{1+\exp(qV_{\mathrm{ds}}/\xi_{\mathrm{n}}kT)}, \tag{33}$$

where ξ_{n} is acquired from experience. Finally, the tunneling current model is given by

$$I_{\mathrm{ds}} = 2q\cdot\pi R^2\lambda_{\mathrm{D}}G_{\max}F_{\mathrm{Fermi}}. \tag{34}$$

3. Result and discussion

The analytical model is validated by comparing the model prediction with the TCAD simulation results.

Figure 3 shows the surface potential profiles $\varphi_{\mathrm{s}}(x)$ along the channel direction with different gate voltages from 0.1 V to 0.7 V and the same drain voltage $V_{\mathrm{ds}} = 0.05$ V. It is evident that with the reduction of the gate voltage, the length of the depletion region, L_1, becomes smaller, and the length of the tunneling region, L_2, becomes larger.

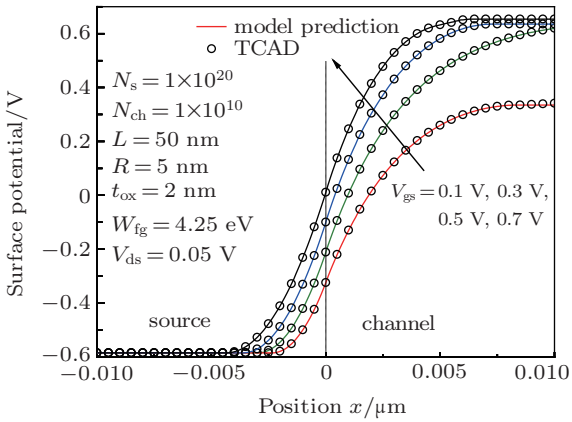


Fig. 3. (color online) The surface potential profiles φ_{s} along the channel direction in a GAA NW-TFET with different gate voltages V_{gs} and the same drain voltage $V_{\mathrm{ds}} = 0.05$ V.

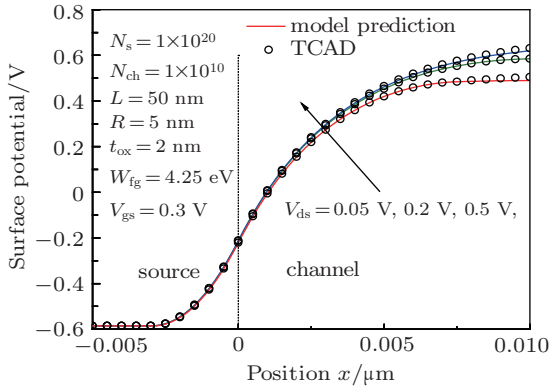


Fig. 4. (color online) The surface potential profiles φ_{s} along the channel direction in a GAA NW-TFET with the same gate voltage $V_{\mathrm{gs}} = 0.3$ V and different drain voltages V_{ds}.

Figure 4 shows the surface potential profiles $\varphi_{\mathrm{s}}(x)$ along the channel direction in a GAA NW-TFET device with the same gate voltage $V_{\mathrm{gs}} = 0.3$ V and different drain voltages V_{ds}. It is observed that with the decrease of the drain voltage, the length of the tunneling region, L_2, becomes smaller, leading to a significant increase in the tunneling probability which can re-

markably enhance the drain current. The model results match well with the TCAD simulation results.

The potential profiles along the radius direction at a certain channel position in a GAA NW-TFET with different gate voltages V_{gs} obtained by the surface potential model are shown in Fig. 5. Good agreements between the model predication and the results of TCAD are clearly observed.

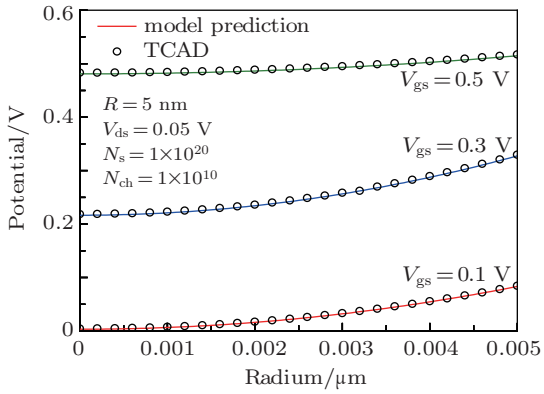


Fig. 5. (color online) The potential profiles φ along the radius direction at a certain channel position $x = L_2$ in a GAA NW-TFET with different gate voltages V_{gs}.

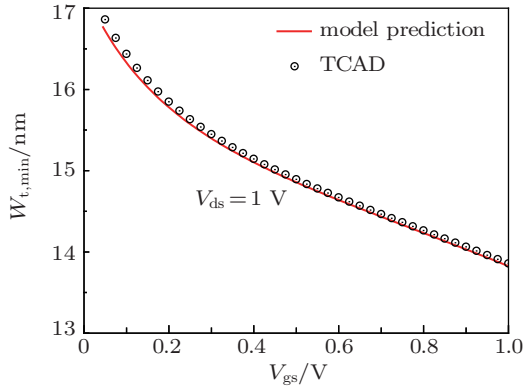


Fig. 6. (color online) The dependence of minimum tunneling width $W_{t,min}$ on the gate voltage V_{gs} with a comparison of the model prediction and the TCAD simulation results.

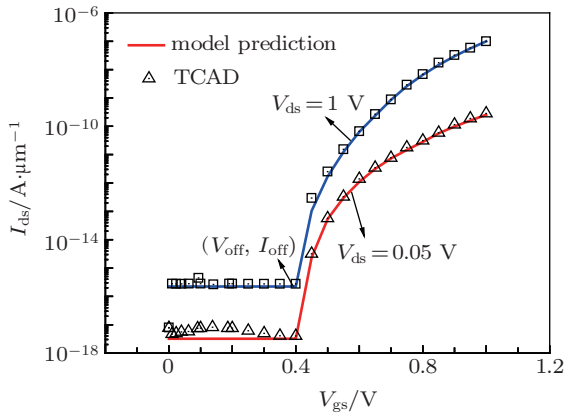


Fig. 7. (color online) Transfer characteristics of I_{ds}–V_{gs} in a log scale with different drain voltages for a GAA-TFET device.

Figure 6 shows the dependence of the minimum tunneling width $W_{t,min}$ on the gate voltage V_{gs}. With the gate voltage increasing, the minimum tunneling width reduces, then a smaller gate bias is needed for the tunneling. It clearly certifies the reduction of the tunneling distance with decreasing V_{gs} observed in Fig. 3.

The transfer characteristics of I_{ds}–V_{gs} are presented in Fig. 7 in a log scale, and the output characteristics of I_{ds}–V_{ds} are shown in Fig. 8 in a linear scale. Good agreements between the model predication and the device simulations are obtained in all regions.

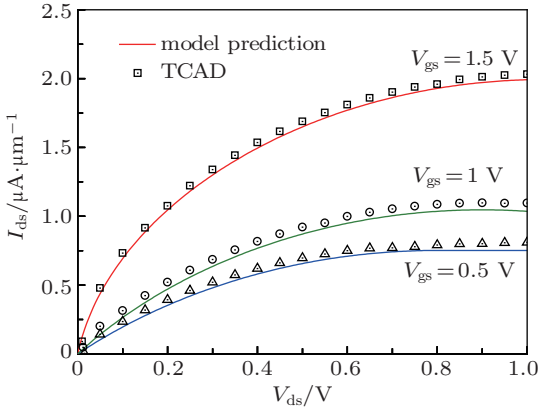


Fig. 8. (color online) Output characteristics of I_{ds}–V_{ds} in a linear scale with different gate voltages for a GAA-TFET device.

The dependences of off-state current I_{off} and subthreshold swing on the drain voltage V_{ds} are shown in Fig. 9. We can see that the SS is much smaller than the traditional MOSFET limit 60 mV/dec and both I_{off} and SS increase almost linearly

$$SS = \frac{dV_{gs}}{d\log(I_{ds})}. \tag{35}$$

The reason is that in GAA NW-TFETs with a larger drain voltage, the tunneling width is also increased, which reduces the BTBT electron generation rate and the tunneling current.

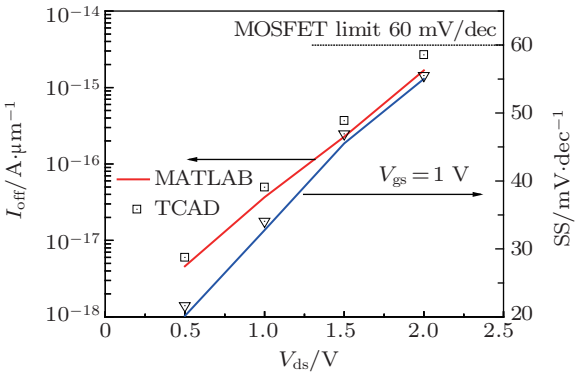


Fig. 9. (color online) Dependences of off-state current I_{off} and subthreshold swing SS on the drain voltage V_{ds}.

4. Conclusion

An analytical current model based on the surface potential solution for the GAA silicon NW-TFETs has been developed in this paper. The model predictions are validated by using the TCAD results, and good agreements between the model prediction and the TCAD simulation results are obtained. It can be expected that this potential based current model can be also extended to study the charge model and some transport properties of the GAA NW-TFETs if more parasitic effects are considered.

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