Estimation of pulsed laser-induced single event transient in a partially depleted silicon-on-insulator 0.18-μm MOSFET

Bi Jin-Shun(毕津顺)†, Zeng Chuan-Bin(曾传滨), Gao Lin-Chun(高林春), Liu Gang(刘 刚), Luo Jia-Jun(罗家俊), and Han Zheng-Sheng(韩郑生)

Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, *China*

(Received 26 November 2013; revised manuscript received 21 February 2014; published online 10 June 2014)

In this paper, we investigate the single event transient (SET) occurring in partially depleted silicon-on-insulator (PDSOI) metal–oxide–semiconductor (MOS) devices irradiated by pulsed laser beams. Transient signal characteristics of a 0.18-μm single MOS device, such as SET pulse width, pulse maximum, and collected charge, are measured and analyzed at wafer level. We analyze in detail the influences of supply voltage and pulse energy on the SET characteristics of the device under test (DUT). The dependences of SET characteristics on drain-induced barrier lowering (DIBL) and the parasitic bipolar junction transistor (PBJT) are also discussed. These results provide a guide for radiation-hardened deep sub-micrometer PDSOI technology for space electronics applications.

Keywords: laser test, single event transient, charge collection, partially depleted silicon on insulator

PACS: 85.30.Tv, 61.80.Ed, 94.05.Dd **DOI:** 10.1088/1674-1056/23/8/088505

1. Introduction

When an energetic particle or photon hits a very large scale integration (VLSI) device, it will induce momentary voltage/current perturbation in a circuit node. This phenomenon is called the single event transient (SET). The SET is becoming a major issue for advanced semiconductor processes as the clock frequency increases continuously.[1–4]

Because the soft error rate of a logic VLSI chip increases with increasing SET pulse width, many researchers have measured and simulated heavy-ion-induced or pulsed-laser-induced SET width in logic cells or combinational circuits.[5–8] They obtained SET pulse width distribution information, but not enough to explain the physical mechanism or to develop device/process-level mitigation methods. Therefore, researchers also carried out experiments on transient current in a high frequency packaged single MOSFET[9–14] or conducted technology computer-aided design (TCAD) simulations. However, few results on SET characteristics in PDSOI 0.18-μm devices at wafer level have been given. Furthermore, the detailed relationship between SET characteristics and device physics such as DIBL and PBJT has not been discussed.

This paper is to investigate the SET of highly integrated elementary transistors based on 0.18-μm PDSOI complementary metal–oxide–semiconductor (CMOS) technology with a focused laser. To the best of our knowledge, this is the first domestic report on this topic. In the first part of the paper, the tested devices and experimental setup are described. In the second part, experimental results of laser irradiation on a single transistor are shown. Detailed SET characteristics are investigated, including pulse width, pulse maximum, and collected charge. It is shown that SET characteristics in a single transistor are greatly influenced by supply voltage and pulse energy. The dependence of SET characteristics on device physics is also discussed. These results are useful for laser evaluation of the relative soft error vulnerabilities and provide a guide for radiation-hardened PDSOI technology.

2. Descriptions of tested devices and experimental setup

2.1. Tested devices

Transistors were fabricated at the Institute of Microelectronics, Chinese Academy of Sciences (IMECAS), with 0.18-μm PDSOI CMOS technology. The transistors were processed on standard 10 Ω · cm–20 Ω · cm p-type 8 inch (1 inch = 25.4 mm) UNIBOND silicon-on-insulator (SOI) substrates. The top silicon film thickness value is 300 nm and the buried oxide (BOX) layer thickness value is 400 nm in the SOI wafers. These devices each have a 0.18-μm long gate and a 3.6-μm wide channel. The equivalent gate oxide thickness value is about 3 nm. A polysilicon layer forms the gate electrode. Each tested device has two-body contacts at each edge of the devices along the channel width direction. The process also involves $CoSi_2$ silicide, six layers of aluminum metal and shallow trench isolation (STI). The standard supply voltage is 1.8 V. This PDSOI CMOS technology is designed for low power applications, with a relatively high threshold voltage and an OFF-state current less than 5 pA · μm^{-1}. Figure 1 illustrates an SEM cross-section of a tested PDSOI MOSFET.

†Corresponding author. E-mail: bijinshun@ime.ac.cn

© 2014 Chinese Physical Society and IOP Publishing Ltd

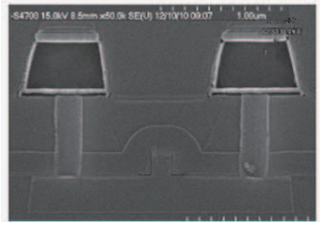


Fig. 1. An SEM picture of a tested PDSOI MOSFET.

Device layout is illustrated in Fig. 2. The source region and drain region of a single transistor are partially covered by six layers of metal lines. The overlapping distance between contacts/vias and metal lines obeys relevant design rules. The source–drain metal spacing is 3 μm, which is much larger than the spot size of the focused laser to avoid laser reflection. The polysilicon gate is right in the middle of the gap between the metal lines.

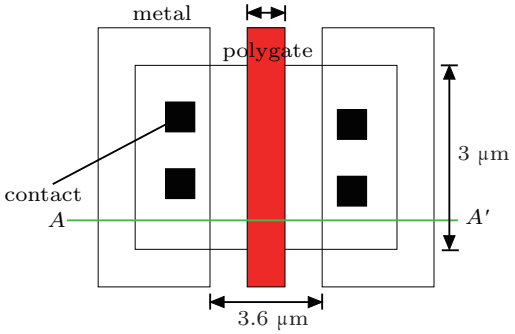


Fig. 2. (color online) Device layout (unscaled). The source–drain metal spacing is 3 μm.

Transistors in the experiments are irradiated in the OFF-state, with the drain bias set at the supply voltage and the other electrodes grounded. This is the most sensitive bias condition for the SET effect on transistors.[11–13]

2.2. Experimental setup

The pulsed laser experiments are performed at IMECAS. The single photon absorption (SPA) experimental setup is shown in Fig. 3. An amplified titanium sapphire laser system (GKPQL-532-20-01) delivers optical pulses centered at 532 nm (2.3 eV) with a duration of 15 ps and 1 kHz repetition rate. The single photon energy is greater than the silicon bandgap (1.12 eV) so that an electron in the valence band will be excited to the conduction band, and leaves a hole there after SPA. The strong laser light beam is attenuated and passes through a waveplate–polarizer combination to precisely control the pulse energy incident on the DUT.

The optical laser beam is focused on the DUT with a 100× Mitutoyo microscope objective, resulting in a 1.2-μm Gaussian spot at FWHM (full width at half maximum). The wafer is loaded on a motorized *xyz* stage with a 100-nm resolution. A 12.5-GHz Tektronix DSA71254B oscilloscope with 50-Ω impedance is used to visualize and record transients. The transistors have ground signal (GS) pad structures which are contacted with the GS probe. Figure 4 shows a simplified schematic diagram of the transient current measurement setup.

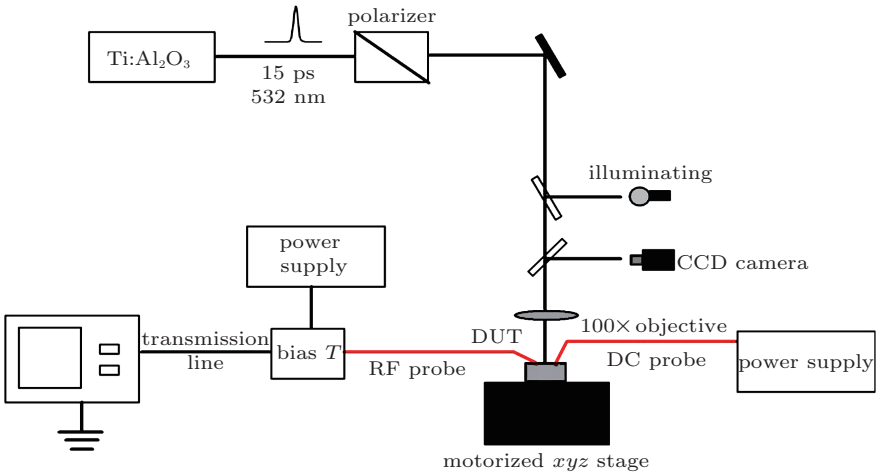


Fig. 3. (color online) Experimental configuration used for on-wafer SPA experiment, where Ti:Al_2O_3 is an amplified titanium sapphire laser system, and a silicon CCD camera is used for image capture.

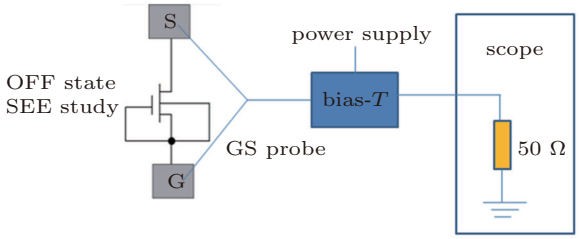


Fig. 4. (color online) Schematic plot of the transient current measurement setup. Transistors are irradiated in the OFF-state, with the drain bias set at supply voltage and the other electrodes grounded. The transient response of the transistor is measured on the drain electrode by using an oscilloscope.

3. Experimental results and discussion

SET curves in tested devices are shown in Fig. 5. The optical pulse energy reaching the device surface varies from 10.4 to 98.5 pJ. The power supply voltage is 1.8 V here. The laser is focused in the middle of the transistor, which is the most sensitive region of the SET for the PDSOI device in this work. The transient current value is negative because current flows from the scope ground into the drain terminal of the n-channel MOSFET. The voltage value, which is shown on the oscilloscope, across the 50 Ω impedance, is negative. The $T = 0$ point is defined as the time when the pulsed laser hits the DUT.

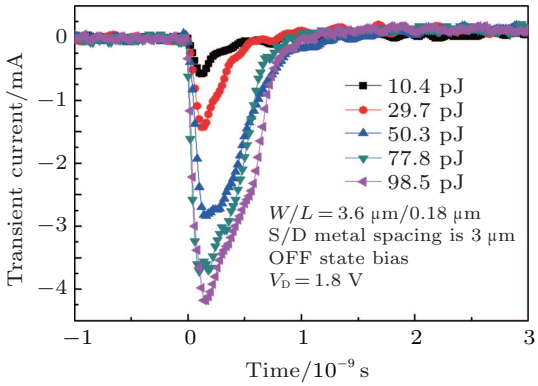


Fig. 5. (color online) Variations of the transient current with time at different values of pulse energy. The supply voltage is 1.8 V. The laser pulse energy increases from 10.4 to 98.5 pJ.

Figure 6 shows that transient current in the DUT is also a function of time and supply voltage. The laser pulse energy used here is 98.5 pJ. The peak of the transient current curve is fairly flat when the supply voltage is 0.2 V. The transient current maximum value increases from 0.88 to 4.18 mA, but the SET pulse width shrinks from 1.1 ns to 565 ps, when the supply voltage steps up from 0.2 to 1.8 V.

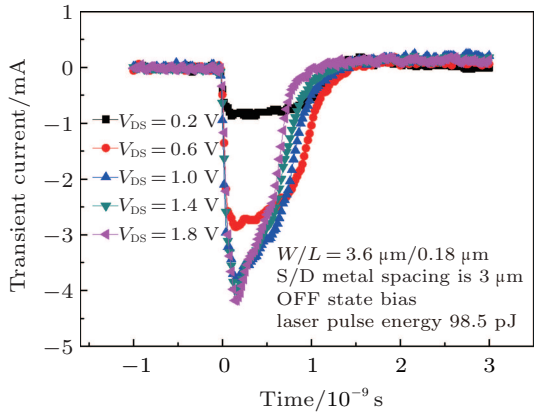


Fig. 6. (color online) Variations of the transient current with time at different values of supply voltage. The laser pulse energy is 98.5 pJ.

Transient current pulse width and maximum value are shown in Figs. 7 and 8 respectively as a function of supply voltage and pulse energy. It is obvious that transient current pulse width and maximum value both increase with increasing laser pulse energy. The SET current pulse maximum ranges from several hundred microamperes to more than 4 mA. The SET current pulse width ranges from 100 ps to more than 1 ns. These values in this paper are in accordance with the recently published results.[15–17]

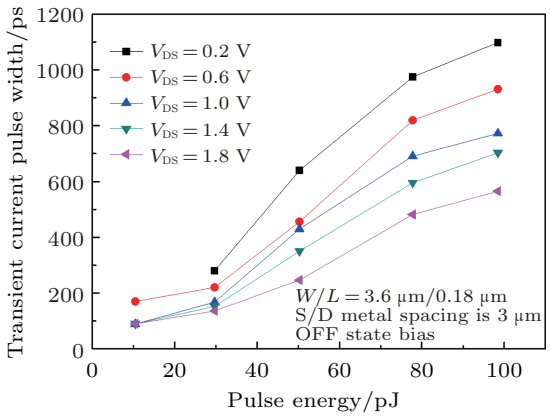


Fig. 7. (color online) Variations of transient current pulse width in PDSOI n-channel MOSFETs with pulse energy at different values of supply voltage.

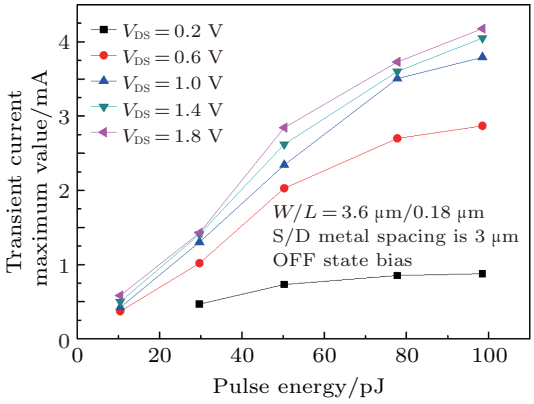


Fig. 8. (color online) Variations of transient current maximum value in PDSOI n-channel MOSFETs with pulse energy at different values of supply voltage.

It is interesting that the trends in pulse width in Fig. 7 and maximum value in Fig. 8 with respect to supply voltage are opposite. The transient current pulse width is the longest and the maximum value is the smallest when the supply voltage is 0.2 V. For a given pulse energy here, the charge quantities deposited in devices are the same no matter what the supply voltage is. The transient current pulse width and maximum value are related to excessive carrier drift velocity, which is determined by lateral electrical field simplified to V_{ds}/L, where L is the channel length of the PDSOI n-channel MOSFETs. The lateral electrical field is smallest when the supply voltage is 0.2 V, so the excessive carrier drift velocity is lowest under bias conditions. The time needed to collect the extra charge is extended. This is why the transient current pulse width shrinks with increasing supply voltage, but the transient current maximum value increases with increasing drain bias.

The collected charge quantity measured on the drain terminal of the PDSOI n-channel MOSFET is given as a function of time and supply voltage in Fig. 9, which is the integration of transient currents in Fig. 6. The curves of the SET collected charge quantity increase start from the moment when the laser hits the device (zero point in time axis) to the point when saturation values are achieved. The point on the time axis where the saturation value is achieved corresponds to the completion of charge collection which is deposited by the pulsed laser. SET collected charge saturation values are 0.87 pC when $V_D = 0.2$ V; 2.52 pC when $V_D = 0.6$ V; 2.69 pC when $V_D = 1$ V; 2.36 pC when $V_D = 1.4$ V; and 2.09 pC when $V_D = 1.8$ V. It is obvious that the SET collected charge increases with increasing supply voltage when $V_D \leq 1.0$ V. However, the growth rate slows down and finally becomes negative.

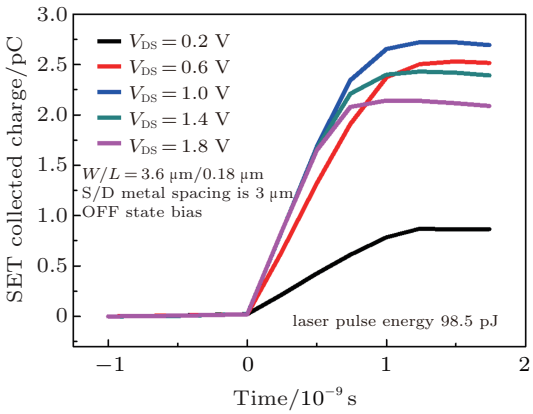


Fig. 9. (color online) Variations of collected charge quantity measured on the drain terminal of PDSOI n-channel MOSFETs with time at different values of supply voltage.

The possible physical explanations for this phenomenon are drain-induced barrier lowering (DIBL) and the parasitic bipolar junction transistor (PBJT), as illustrated in Fig. 10. According to Refs. [18]–[21], heavy ions and a pulsedlaser will generate electron–hole pairs in the body region of the SOI device. The generated electron–hole pairs in the heavily doped source–drain regions which reach the silicon/BOX interface will recombine quickly, so they will not be taken into consideration. The deposited electrons are collected by the drain terminal. Some of the holes in the body will be collected by body contacts in the width direction along the highly resistive path. Some of the holes in the body will cross the source–body junction barrier. The remaining holes in the body will trigger the PBJT due to the relatively long carrier lifetime. For a deep sub-micrometer device, DIBL is a serious problem. The rise of supply voltage will lower the source–body potential barrier and threshold voltage in the device. More holes cross the source–body junction barrier initially and fewer remaining holes in the body will amplify the excessive carriers. This is a piece of good news for radiation hard design application, because the higher the supply voltage is the greater the charge quantity stored in nodal capacitance will be. At the same time, the SET collected charge quantity is lower. This means that circuits based on this technology are more SET resistant. However, there also exists a tradeoff. If the threshold voltage is too low due to DIBL, the leakage current of the device will be unacceptable.

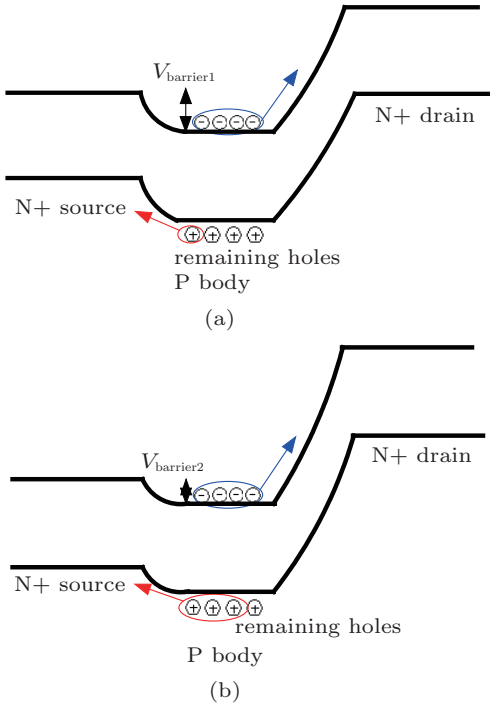


Fig. 10. (color online) Energy band diagram during the SET process with DIBL and PBJT taken into consideration: (a) $V_D \leq 1.0$ V; (b) $V_D = 1.8$ V. The $V_{barrier2}$ is less than the $V_{barrier1}$ due to the DIBL effect. Therefore, there are fewer remaining holes to trigger PBJT in case (b).

After the derivation of electron and hole continuity equations with boundary conditions as given in Refs [22] and [23], the transient current I_p introduced by heavy ions or a pulsed laser in the PDSOI transistor could be modeled as follows:

$$I_P(x_s,t) = \frac{1.3Q}{t_p} \times \left[\sin\left(\frac{2\pi}{5}\right) \exp\left(-\frac{t}{t_p}\right) - 3\sin\left(\frac{\pi}{5}\right) \exp\left(-\frac{9t}{t_p}\right) + \left(3\sin\left(\frac{\pi}{5}\right) - \sin\left(\frac{2\pi}{5}\right)\right) \times \exp\left(-\frac{49t}{t_p}\right) \right], \quad (1)$$

where x_s is the heavy ion or pulsed laser strike location, t is the time, and Q is the collected charge quantity. The integration of transient current with respect to time will approach to Q if t is assumed to be infinite. t_p is the characteristic time constant and is defined as

$$t_p = \frac{4x_s^2}{\pi^2 D}, \quad (2)$$

where D is the bipolar diffusion coefficient during high level injection (electron density is equal to hole density) and is defined as follows:

$$D = \frac{2D_{\rm n}D_{\rm p}}{D_{\rm n}+D_{\rm p}}, \tag{3}$$

where $D_{\rm n}$ is the electron diffusion coefficient and $D_{\rm p}$ is the hole diffusion coefficient.

The relationship between $I_{\rm p}(x_{\rm s},t)$ and drain bias is implicit by the factor Q, which means that Q is a strong and nonlinear function of drain bias, as shown in Fig. 9.

4. Conclusions

In this paper, we study SET in a PDSOI 0.18-μm single MOSFET, which is introduced by a pulsed laser. SET characteristics such as pulse width, pulse maximum, and collected charge are strongly related to optical pulse energy and supply voltage. The SET current pulse maximum ranges from several hundred microamperes to more than 4 mA. The SET current pulse width ranges from 100 ps to more than 1 ns, which is comparable to the operating clock period for a modern digital circuit. It is found that the charge collection process is also influenced by electrical field related carrier velocity. The smaller the supply voltage is, the longer the SET pulse width and the smaller the maximum value will be. The trend of variation in SET collected charge is also determined by DIBL and PBJT. DIBL lowers the source–body junction barrier to mitigate the amplification of deposited charge quantity. These results are useful for developing the radiation-hardened deep sub-micron PDSOI technology for space electronics applications.

References

[1] Buchner S, Baze M, Brown D, McMorrow D and Melinger J 1997 *IEEE Trans. Nucl. Sci.* **44** 2209

[2] Gadlage M J, Schrimpf R D, Benedetto J M, Eaton P H, Mavis D G, Sibley M, Avery K and Turflinger T L 2004 *IEEE Trans. Nucl. Sci.* **51** 3285

[3] Benedetto J M, Eaton P H, Avery K, Mavis D, Gadlage M, Turflinger T, Dodd P E and Vikelethyd G 2004 *IEEE Trans. Nucl. Sci.* **51** 3480

[4] Baumann R C 2005 *Proc. IEEE Nuclear and Space Radiation Effects Conf. Short Course*

[5] Benedetto J M, Eaton P H, Mavis D G, Gadlage M and Turflinger 2005 *IEEE Trans. Nucl. Sci.* **52** 2114

[6] Narashimham B, Bhuva B L, Schrimpf R D, Massengill L W, Gadlage M J, Amusan O A, Holman W T, Witulski A F, Robinson W H, Benedetto J M and Eaton P H 2007 *IEEE Trans. Nucl. Sci.* **54** 2506

[7] Dodd P E, Shaneyfelt M R, Felix J A and Schwank J R 2004 *IEEE Trans. Nucl. Sci.* **51** 3278

[8] Makino T, Kobayashi D, Hirose K, Yanagawa Y, Saito H, Ikeda H, Takahashi D, Ishii S, Kusano M, Onoda S, Hirao T and Ohshima T 2009 *IEEE Trans. Nucl. Sci.* **56** 202

[9] Bi J S, Liu G, Luo J J and Han Z S 2013 *Acta Phys. Sin.* **62** 208501 (in Chinese)

[10] Zhang J X, Guo H X, Guo Q, Wen L, Cui J W, Xi S B, Wang X and Deng W 2013 *Acta Phys. Sin.* **62** 048501 (in Chinese)

[11] Qin J R, Chen S M, Li D W, Liang B and Liu B W 2012 *Chin. Phys. B* **21** 089401

[12] Ferlet-Cavrois V, Paillet P, McMorrow D, Torres A, Gaillardin M, Melinger J S, Knudson A R, Campbell A B, Schwank J R, Vizkelethy G, Shaneyfelt M R, Hirose K, Fayout O, Jahan C and Tosti L 2005 *IEEE Trans. Nucl. Sci.* **52** 2104

[13] Kobayashi D, Saito H and Hirose K 2007 *IEEE Trans. Nucl. Sci.* **54** 1037

[14] Kobayashi D, Hirose K, Yanagawa Y, Ikeda H, Saito H, Ferlet-Cavrois V, McMorrow D, Gaillardin M, Paillet P, Arai Y and Ohno M 2008 *IEEE Trans. Nucl. Sci.* **55** 2872

[15] Ahlbin J, Gadlage M, Atkinson N, Narasimham B, Bhuva B, Witulski A, Holman W, Eaton P and Massengill L 2011 *IEEE Transactions on Device and Material Reliability* **11** 401

[16] Huang P C, Chen S M, Chen J J and Liu B W 2013 *Sci. China: Technol. Sci.* **56** 271

[17] El-Mamouni F, Zhang E X, Pate N D, Hooten N, Schrimpf R D, Reed R A, Gallaway K F, McMorrow D, Warner J, Simoen E, Claeys C, Griffoni A, Linten D and Vizkelethy G 2011 *IEEE Trans. Nucl. Sci.* **58** 2563

[18] Musseau O, Ferlet-Cavrois V, Pelloie J L, Bucher S, McMorrow D and Cambell A B 2000 *IEEE Trans. Nucl. Sci.* **47** 2196

[19] Massengill L W, Kerns D V, Kerns S E and Alles M L 1990 *IEEE Electron Dev. Lett.* **11** 98

[20] Fulkerson D E and Vogt E E 2005 *IEEE Trans. Nucl. Sci.* **52** 2168

[21] Roy T, Witulski A F, Schrimpf R D, Alles M L and Massengill L W 2008 *IEEE Trans. Nucl. Sci.* **55** 2948

[22] Fulkerson D E and Liu H 2004 *IEEE Trans. Nucl. Sci.* **51** 275

[23] Fan Z H, Bi J S and Luo J J 2011 *Microelectronics & Computer* **28** 40 (in Chinese)