SPECIAL TOPIC — International Conference on Nanoscience & Technology, China 2013

Comparison between N_2 and O_2 anneals on the integrity of an $Al_2O_3/Si_3N_4/SiO_2/Si$ memory gate stack*

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(Received 4 September 2013; revised manuscript received 16 December 2013; published online 10 June 2014)

In this paper the endurance characteristics and trap generation are investigated to study the effects of different post-deposition anneals (PDAs) on the integrity of an $Al_2O_3/Si_3N_4/SiO_2/Si$ memory gate stack. The flat-band voltage (V_{fb}) turnarounds are observed in both the programmed and erased states of the N_2-PDA device. In contrast, this turnaround is observed only in the erased state of the O_2-PDA device. The V_{fb} in the programmed state of the O_2-PDA device keeps increasing with increasing program/erase (P/E) cycles. Through the analyses of endurance characteristics and the low voltage round-trip current transients, it is concluded that in both kinds of device there are an unknown type of pre-existing characteristic deep traps and P/E stress-induced positive oxide charges. In the O_2-PDA device two extra types of trap are also found: the pre-existing border traps and the P/E stress-induced negative traps. Based on these four types of defects we can explain the endurance characteristics of two kinds of device. The switching property of pre-existing characteristic deep traps is also discussed.

Keywords: charge trapping memory, post deposition anneal, endurance, traps

PACS: 85.30.–z **DOI:** 10.1088/1674-1056/23/8/088501

1. Introduction

As flash memory devices continue to be scaled down, a charge trapping memory device has been proposed to replace the floating gate memory due to its discrete charge storage and smaller capacitance coupling between neighboring cells.[1,2] The high-k Al_2O_3 is the most widely blocking layer material in charge trapping memory due to its relatively large dielectric constant value and energy band gap, which make it possible to have a higher electric field in the SiO_2 tunneling layer to enhance the program/erase speed and a higher electron barrier to suppress the gate back-tunneling during an erase operation. However, compared with thermally grown SiO_2, Al_2O_3 usually contains a lot of defects even using atomic layer deposition.[3] The defects in Al_2O_3 material can form trap sites and result in poor data retention due to the trap-assisted tunneling leakage current.[4] Post-deposition annealing (PDA) is usually adopted to reduce trap density and to densify the gate stack structure.[5–7] However, endurance characteristics are also strongly affected by the trap generation in program/erase (P/E) cycling.[8] Optimizing the PDA process (temperature, ambient, etc.) may change the microscopic structure of the dielectric and thus may reduce the speed of the trap generation. Indeed in our previous study,[9] we have found that compared with the low temperature N_2 PDA, the high temperature N_2 annealing can improve the memory performance significantly. Other researchers also reported that the O_2-PDA was better than N_2 PDA in improving the quality of $A1_2O_3$.[10] However, a systematic investigation of the effects of different PDA environments on the endurance characteristic is still lacking, let alone the study on the underlying physical mechanism. In this paper we measure the endurance characteristics of a MANOS gate stack under different PDA environments. Then through the capacitance–voltage (CV) and current–voltage (IV) measurements, we analyze the pre-existing traps and the P/E stress-induced traps, and explain the underlying physical origins of endurance behaviors under different PDA environments.

2. Experiments

Our experiments are performed on the MOS capacitor with the MANOS structure. Devices are fabricated on p-type (100) Si substrates of the resistivity values in a range of 1 Ω·cm–10 Ω·cm. After a standard cleaning process, 4-nm SiO_2 is thermally grown in 900 °C as the tunnel oxide, then a 7-nm Si_3N_4 is deposited by low pressure chemical vapor deposition (LPCVD) as a charge trapping layer. A 15-nm Al_2O_3 is deposited by atomic layer deposition as a blocking

*Project supported in part by the National Basic Research Program of China (Grant Nos. 2010CB934200 and 2011CBA00600), the National Natural Science Foundation of China (Grant Nos. 61176073 and 61176080), and the Director's Fund of the Institute of Microelectronics, Chinese Academy of Sciences.

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layer at 250 °C. On devices splitting both N_2 and O_2 PDA are performed at 1000 °C for 60 s. Then a 100 μm×100 μm Al electrode with a thickness of about 200 nm is deposited using electron beam evaporation and patterned through the lift-off process. Finally, Al back-gate electrode deposition is done followed by N_2-annealing at 400 °C for 10 min to form Ohmic contact. The electrical characteristics are measured using an Agilent B1500A semiconductor device analyzer. Without drain and source terminals, light illumination is used to assist the minority carrier generation during program speed measurement.[11] CV curves are measured at 1 MHz. The corresponding parameters such as the flatband voltage (V_{fb}) and surface potential are extracted using the popular CVC program developed by Hauser *et al.* at North Carolina State University.[12]

3. Results and discussion

Figure 1 shows the comparison between the current density versus gate voltage (J_g–V_g) curve of the MANOS device under N_2 PDA and that under O_2 PDA. Compared with the device with N_2-PDA, the MANOS device with O_2-PDA shows a low leakage current in a high voltage region, which is in agreement with the result from Rothchild *et al.*[8] When gate voltage is positive ($V_g > 0$), substrate minority carrier injection takes place. The MANOS device with O_2-PDA has a lower saturation current in a range of V_g higher than 10 V. It is due to the very slow minority carrier (electron) generation time in the MANOS device with O_2-PDA, which has been proved by our previous measurement[11] and is further supported by a larger take-off time in a program speed curve of the O_2-PDA device as shown in Fig. 2. The MANOS devices with O_2-PDA show slightly faster erase transients, which is consistent with the lower leakage currents of Al_2O_3 in these devices.

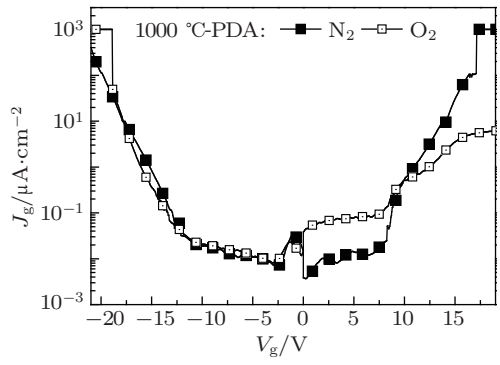


Fig. 1. Curves of leakage current density versus gate voltage for 1000-°C annealed MANOS devices in the dark.

Figure 3 shows the variations of V_{fb} with the number of P/E cycles in both the programmed (P) and erased (E) state. The conditions of program and erase are 16 V/40 ms and −18 V/80 ms, respectively. In the MANOS device with N_2-PDA, V_{fb} shows turnaround phenomena both in the P-state and in the E-state.[13] In comparison, V_{fb} in the MANOS device with O_2-PDA shows the turnaround phenomenon only in the erase state. It can be seen that the V_{fb} values in the fresh devices with either of N_2 and O_2 PDA are all about −2.0 V. After one P/E cycle, the V_{fb} value in the E state cannot return to −2.0 V any more: it is about 1 V. It will be shown in the following that this phenomenon is due to the existence of characteristic deep traps of this unknown type in the fresh device and then these deep traps are charged by electrons during the first program operation. To understand the data in Fig. 3 in detail, we measure the round-trip leakage current transient in the fresh and P/E stressed MANOS devices.[14]

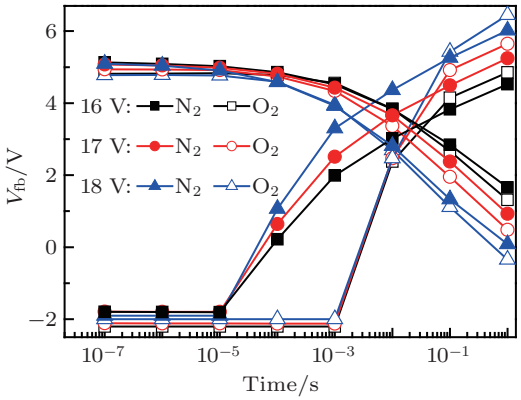


Fig. 2. (color online) Curves of flatband voltage (V_{fb}) versus time, showing the comparison among program/erase speeds in MANOS devices with 1000-°C PDA. The program operation is assisted by light illumination.

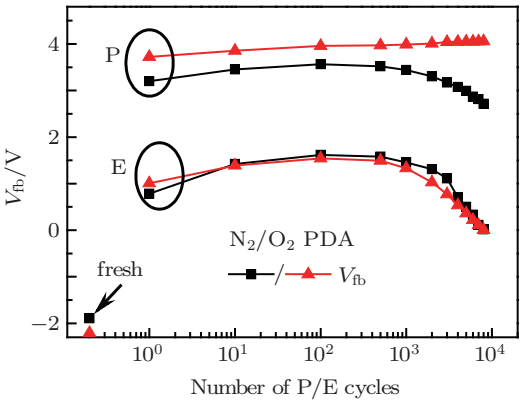


Fig. 3. (color online) Curves of flatband voltage (V_{fb}) versus the number of P/E cycles, showing the endurance characteristics of MANOS devices with 1000-°C N_2 and O_2 PDA.

Figure 4 shows the comparison between the leakage current density in fresh MANOS devices with N_2 PDA and with O_2 PDA. In the N_2-PDA device, a current spike with an amplitude of 0.77 μA/cm^2 is observed around $V_g = 0$ V. Similarly a current spike with an amplitude of 0.38 μA/cm^2 is also seen in the device with O_2-PDA. There is a difference between the two kinds of device. In the device with O_2-PDA, a current plateau appears following the current spike in the positive gate voltage. Figures 5 and 6 show the current transients in both

P-states and E-states for the N_2-PDA and O_2-PDA devices, respectively. The current spikes are clearly seen in the E-states, but not in the P-states. A comparison between the fresh devices shows that the amplitudes of the current spikes decrease a lot in the E1-state for both kinds of devices. With further increasing the number of P/E cycles, the amplitudes of the current spikes in two kinds of devices and the current plateau in the O_2-PDA devices grow gradually. We attribute the current spike to the characteristic deep oxide traps of an unknown type and the current plateau to the border traps in the O_2-PDA device. Border traps are the near-interfacial oxide traps located within approximately 3 nm of the SiO_2/Si interface.[15] A comparison between the current transient in the positive trip and that in the negative trip shows the border traps can charge and discharge very fast. For the characteristic deep oxide traps, the situation is slightly more complicated. In order to explain the amplitude changes of the current spike in fresh and cycled devices, we propose that the characteristic deep traps have two switching atom configurations corresponding to two different trap levels (denoted as C1 and C2). In fresh devices with two kinds of PDAs, the characteristic deep traps are at configuration C1. However, after one program operation, most of the characteristic deep traps are converted into configuration C2, in which the speeds of the electron emission and capture are both thought to be very slow. With further increasing the number of P/E cycles, the characteristic deep traps then gradually are converted back into configuration C1. When at configuration C1, charging the characteristic deep traps is very fast, but discharging them is still slow, which can be seen from the lack of current spikes in the current transients in the negative trips in Figs. 5(b) and 6(b). From past experience, it is reasonable to assume that the total density of characteristic deep traps at either C1 or C2 decreases during P/E cycling. In the N_2-PDA device, there are not many border traps. As all characteristic deep traps are filled with electrons in the P-states, so the V_{fb} turnaround in the P-state must be due to other newly generated positive charges. The V_{fb} turnaround in the E-state is steeper than that in the P-state. It is due to the combining effect of the newly generated positive charges, the conversion of characteristic deep traps from configuration C2 into configuration C1 with increasing P/E cycles and the subsequent discharges in the E-states. For the O_2-PDA devices, the V_{fb} turnaround in the E-states is due to the same reasons; the absence of the V_{fb} turnaround in the P-states should be due to the faster generation of negative traps than the generation of positive charges. Unlike the above-mentioned border traps, these negative traps can be charged only through a program operation and discharged through an erase operation, so they are not observable in the low-voltage roundtrip current transients. In addition, these P/E stress-induced negative traps should be located more deeply in the SiO_2 layer than the border traps.

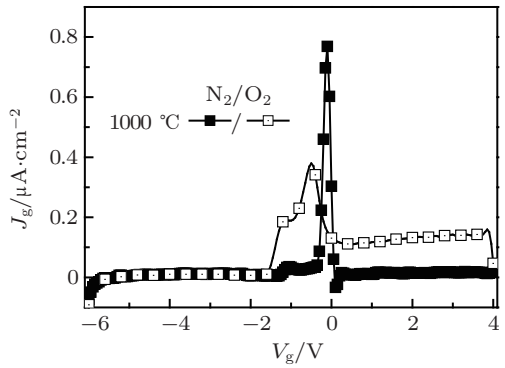


Fig. 4. The leakage current densities versus gate voltage in fresh MANOS devices with N_2 and O_2 PDA.

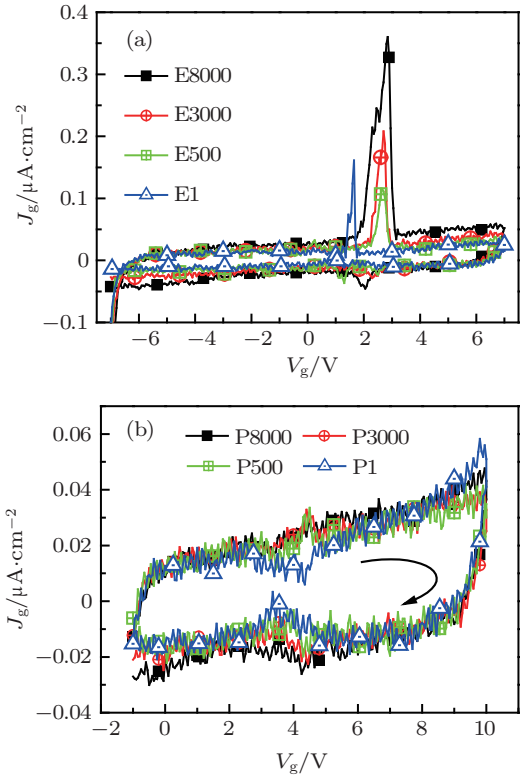


Fig. 5. (color online) Curves of round-trip leakage current transient versus the number of P/E cycles in (a) E-states and (b) P-states of the MANOS device with 1000-°C N_2-PDA.

To determine the energy position of the characteristic deep trap responsible for the current spike, we analyze the 1-MHz CV curve in the fresh MANOS device. At the gate voltage where the current spike appears, a small hump in the 1-MHz CV curve is observed in Fig. 7. By fitting the measured CV curve with the CVC program, we extract the surface potential and the ideal low-frequency CV curve. From the surface potential curve, the energy level of the deep trap at configuration C1 is determined to be ~ 0.08 eV below the Si conduction band edge for the O_2-PDA device. A similar energy level of the deep trap (~ 0.11 eV below the Si conduction band edge) is also obtained for the N_2-PDA device. The energy level of the deep trap at configuration C2 could not be determined due to its inactivity to exchange carriers with Si substrate.

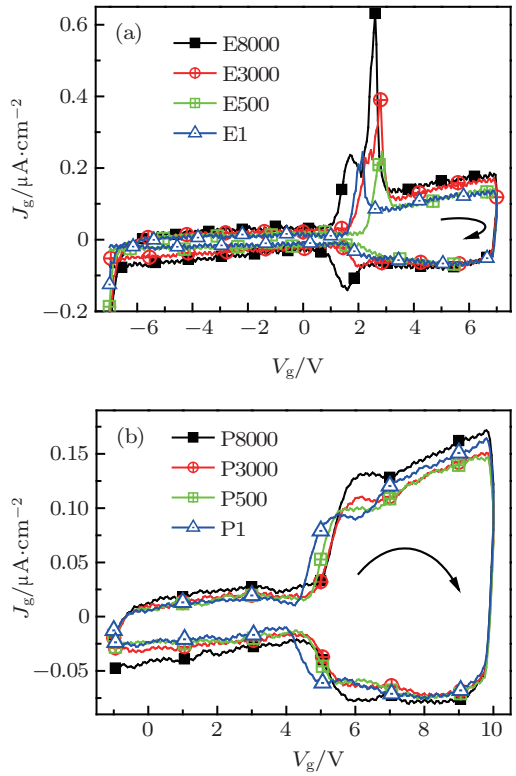


Fig. 6. (color online) Curves of round-trip leakage current transient versus the number of P/E cycles in (a) E-states and (b) P-states of the MANOS device with 1000-°C O_2-PDA.

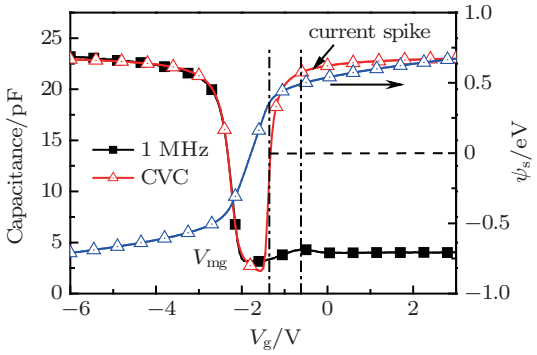


Fig. 7. (color online) Comparison between the measured 1-MHz CV curve and the simulated low frequency CV and surface potential curves from CVC program in O_2-PDA devices.

Why does the O_2-PDA result in a high density of border traps and a long minority carrier generation time in Si substrate? A well-known fact is that during the O_2-anneal, oxygen atoms can replace some N atoms in the silicon nitride layer, and some excess N atoms will diffuse out.[16] According to this, we propose that during O_2-PDA, some N atoms may move into the SiO_2/Si interface forming some dangling silicon bonds. The diffusion of N atoms through the SiO_2 layer may also be responsible for the P/E stress-induced negative traps in the O_2-PDA device. Finally we explain the generation of the positive oxide charges using the anode hole injection, which happens at high stress voltage,[17,18] and is responsible for the V_{fb} turnaround during P/E cycling.

Now we summarize the types of defects in the two kinds of device. In both the N_2-PDA and O_2-PDA devices, there are the pre-existing characteristic deep traps responsible for the current spike and the P/E stress-induced positive charges. In the O_2-PDA device, there are two more types of traps: the pre-existing border traps and the P/E stress-induced negative traps. Figure 8 shows a schematic illustration of the energy and space locations of four types of defects in gate dielectric stacks. Both border traps and the pre-existing characteristic deep traps at configuration C1 are able to exchange carriers with the Si substrate through capture and emission processes.

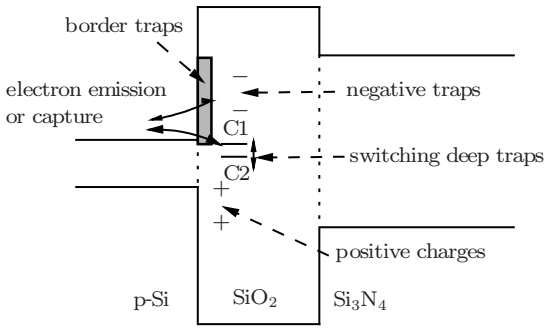


Fig. 8. Schematic illustration of border traps, positive oxide charges, negative traps, and the characteristic deep traps responsible for the current spike. C1 and C2 are two switching levels of characteristic deep traps.

4. Conclusions

We have observed the V_{fb} turnaround phenomena in the endurance degradation in metal/Al_2O_3/ Si_3N_4/SiO_2/Si memory devices with N_2- and O_2-PDA. By combining CV and IV measurements, we are able to analyze pre-existing and P/E stress-induced traps in the devices. In the N_2-PDA and O_2-PDA devices, there are the pre-existing characteristic deep traps responsible for the current spike and the stress-induced positive charges. In the O_2-PDA devices, there are two more types of traps: the pre-existing border traps and the stress-induced negative traps. We propose that the pre-existing characteristic deep traps can switch between two atom configurations (denoted as C1 and C2). Only at configuration C1 are these characteristic deep traps able to exchange electrons with Si substrate efficiently. From the CV measurement, the trap energy level at configuration C1 is determined to be about 0.1 eV below the Si conduction band edge. Although our experimental results show that the O_2-PDA has improved the quality of Al_2O_3, it also induces two extra types of oxide traps in the SiO_2 tunneling layer: the pre-existing border traps and the stress-induced negative oxide traps. So it is important to optimize the PDA condition not only to improve the quality of each individual dielectric layer, but also to keep the integrity of the whole gate dielectric stack.

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