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Quantum transport characteristics in single and multiple N-channel junctionless nanowire transistors at low temperatures*

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Single and multiple n-channel junctionless nanowire transistors (JNTs) are fabricated and experimentally investigated at variable temperatures. Clear current oscillations caused by the quantum-confinement effect are observed in the curve of drain current versus gate voltage acquired at low temperatures (10 K–100 K) and variable drain bias voltages (10 mV–90 mV). Transfer characteristics exhibit current oscillation peaks below flat-band voltage (V_{FB}) at temperatures up to 75 K, which is possibly due to Coulomb-blocking from quantum dots, which are randomly formed by ionized dopants in the just opened n-type one-dimensional (1D) channel of silicon nanowires. However, at higher voltages than V_{FB}, regular current steps are observed in single-channel JNTs, which corresponds to the fully populated subbands in the 1D channel. The subband energy spacing extracted from transconductance peaks accords well with theoretical predication. However, in multiple-channel JNT, only tiny oscillation peaks of the drain current are observed due to the combination of the drain current from multiple channels with quantum-confinement effects.

Keywords: junctionless nanowire transistors (JNT), quantum transport, current oscillations, low temperatures

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1. Introduction

Multi-gate three-dimensional (3D) metal–oxide–semiconductor field-effect transistors (MOSFETs) are considered as having a most promising structure, which is likely to push the limits of silicon integrated circuits beyond the bound of classical planar technologies.[1,2] Compared with the gate in traditional planar field-effect transistors, the gate in a multi-gate FET surrounds the conductive channel in different directions to obtain a good control of the conductive channel.[3] Consequently, the advantages of the device structure are obvious in reducing short channel effects and leakage currents.[4] However, in extremely short-channel devices ($L = 10$ nm or less), the fabrication of an ultra-sharp doping concentration gradient p–n junction between source/drain and channel requires an extremely complex manufacturing process. Recently, the junctionless nanowire transistor (JNT) has been proposed to provide an alternative to simplify the fabrication process. In the JNT there are no p–n junctions between source and channel, nor between drain and channel.[5,6] The JNT is normally-off device in which the carriers in the narrow channel are fully depleted due to plenty of surface states. Above the gate threshold voltage, the conductive path first emerges in the center of the nanowire and then gradually expands to the whole nanowire. This property provides an opportunity to study the quantum transport characteristics of one-dimensional (1D) structures in silicon material. It has been reported that JNTs show clear current oscillations at 77 K at a drain voltage of 100 mV and more marked conductance oscillations than the inversion-mode devices.[7] In addition, in a heavily doped nanowire, the random distribution of impurity ions will affect the device transport characteristics by forming a series of small quantum dots.[8,9] Dopant engineering is promising for the deep understanding of single-dopant devices.[10] In this paper, we report low-temperature quantum transport characteristics in single and multiple n-channel JNTs in a temperature range of 10 K–295 K. Our objective is to present the different quantum behaviors of drain current in single and multiple-n-channel JNTs. The quantum-confinement effect in single-channel JNT induces current oscillations below the flatband voltage V_{FB} at temperatures up to 75 K, and current steps above V_{FB} at temperatures down to 50 K. In multiple-channel JNT, however, only tiny oscillation peaks of drain current are observed due to the combination of the drain current from multiple channels with quantum-confinement effects.

2. Device fabrication

A boron-doped (10^{15} cm^{-3}) (100)-oriented SOI wafer with a top Si thickness of 55 nm and a buried oxide (BOX) layer thickness of 145 nm was used as the starting substrate. In the first place, the SOI wafer was heavily doped by phosphorus ion implantation with a dose of 5×10^{13} cm^{-2} at an en-

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ergy of 33 keV after thermal oxidation for the formation of a 15-nm-thick silicon dioxide. Then silicon nanowires were fabricated by electron beam lithography (EBL) and inductively coupled plasma (ICP) etching. Sacrificial oxidation was used to remove the etch damage of the edges. The 22-nm-thick gate oxide was grown at 900 °C in dry oxygen. A 200-nm-thick polysilicon layer was then deposited by low-pressure chemical-vapor deposition (LPCVD) on the gate oxide. After being heavily doped by boron ion implantation and rapidly annealed in ambient nitrogen, the polysilicon gates 280 nm were defined by EBL and ICP etching. The followed process was the deposition of 200-nm SiO_2 for passivation. Transitional aluminum/silicon metallization technology was used to complete the process. Figure 1 shows the schematic three-dimensional (3D) layouts of the device and the top view SEM. Figure 1(a) shows the scanning electron microscopy (SEM) image of a single-channel JNT with a 1000-nm-long and about 75-nm-wide fin connecting the source and drain regions. The effective diameter of the silicon nanowire in the core of the fin is about 30 nm. Figure 1(b) shows the SEM image of a multiple-channel JNT with five fins of 500-nm length and various widths from 60 nm to 75 nm. The width difference between the five fins comes from the processing deviation. The effective widths of five silicon nanowires should be in a range from 15 nm to 30 nm. The effective height of silicon nanowires is estimated to be about 30 nm. The devices were placed in a vacuum chamber which can be cooled down to $\sim$ 6 K with the help of Lakershore-340 temperature controller. The drain current characterizations were measured by an Agilent B1500 semiconductor parameter analyzer.

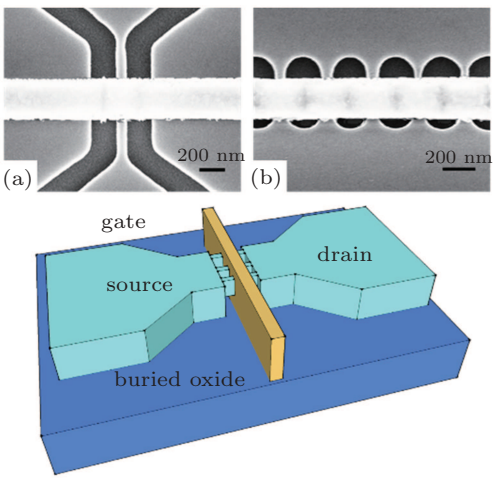


Fig. 1. (color online) Schematic 3D layouts of the device and top-view SEM of (a) single-channel JNT and (b) multi-channel JNT, and the illustration of the device (below).

3. Results and discussion

At room temperature, both single and multiple n-channel JNTs exhibit nearly ideal transfer and output characteristics. The transfer (I_{DS}–V_{GS}) curves in Fig. 2 show that single and multiple n-channel JNTs operate as normally-off devices, have a low gate leakage of about 10 pA each. The on/off current ratio is larger than 1×10^5 in a range of V_{GS} from 0.2 V

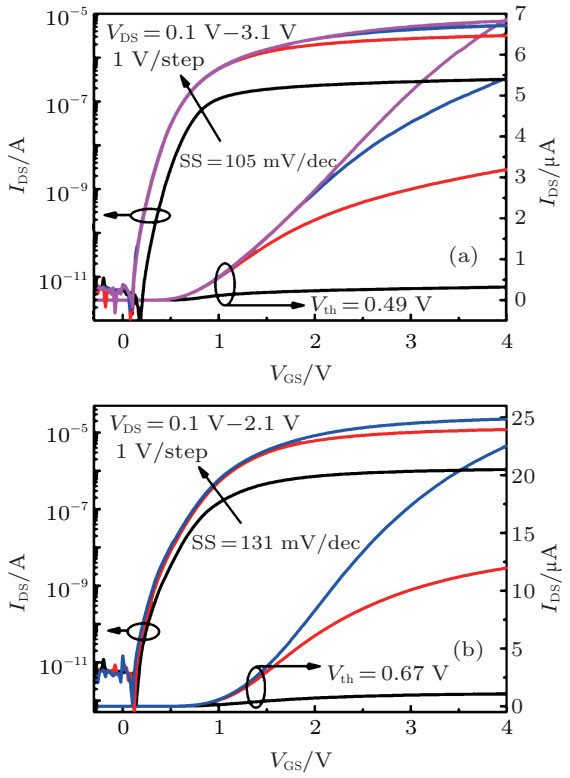


Fig. 2. (color online) I_{DS}–V_{GS} curves of (a) single and (b) multiple n-channel JNTs at room temperature.

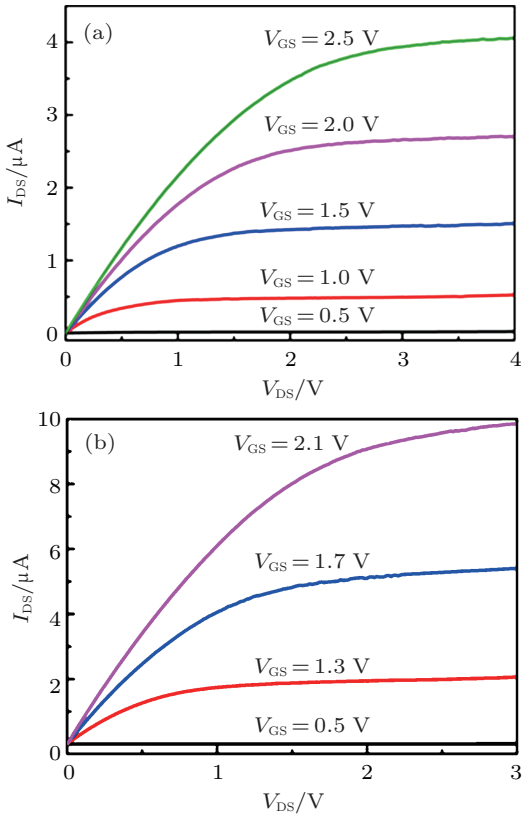


Fig. 3. (color online) I_{DS}–V_{DS} curves of (a) single and (b) multiple n-channel JNTs at room temperature.

to 1.5 V. The single-channel device has a threshold voltage V_{TH} of ~ 0.49 V, subthreshold swing (SS) of $\sim$110 mV/dec, and drain-induced barrier lowering (DIBL) of $\sim$100 mV/V. The multiple-channel device has a threshold voltage V_{TH} of $\sim$0.67 V, SS of $\sim$131 mV/dec, and DIBL of $\sim$50 mV/V. The positive threshold voltage for the n-type JNT indicates that the conductive channel is completely cutoff when the gate voltage is not applied. The positive threshold voltage in a multiple-channel JNT with narrower silicon nanowires is larger than that of a single-channel JNT.[11] The output curves in Fig. 3 demonstrate excellent gate controlability in our devices. The multiple-channel JNT allows the drive current to be enhanced by increasing the number of nanowire channels. The saturate drain currents are 2.5 μA for the single-channel device at $V_{GS} = 2.0$ V and 10 μA for the five-channel device at $V_{GS} = 2.1$ V.

As the temperature is reduced to lower than 100 K, some interesting current oscillations are observed in the n-channel JNTs. Figure 4(a) shows the I_{DS}–V_{GS} characteristics of single-channel JNT at bias voltage $V_{DS} = 10$ mV and different temperatures. The dotted line indicates the flat-band gate voltage V_{FB}. When the gate voltage is beyond V_{FB}, the regular steps of drain current are observed at the temperatures up to 50 K and completely disappear at temperatures beyond 75 K. The steps of drain current come from the 1D quantum confinement effects. Each step of drain current corresponds to a discrete fully populated subband in the 1D nanowire.[12] With the temperature increasing, thermal fluctuation is higher than the subband energy spacing ΔE. The Fermi–Dirac distribution of electrons could cover a series of subbands, smearing out the oscillations. We notice that the current curves of 10 K, 15 K, and 20 K are staggered together, which is due to the interaction between the thermal activation and the impurity scattering at low temperatures.[13] Figure 4(b) shows the I_{DS}–V_{GS} characteristics of a single-channel JNT at the temperature $T = 15$ K and different values of V_{DS}. The amplitudes of regular steps of drain current are weakened with V_{DS} increasing. In addition, when the gate voltage is below V_{FB}, some drain current oscillations could be obviously observed. As in a heavily doped nanowire, the impurity ions are randomly distributed. In this case, a nearly linear array of multiple electron islands can be formed to strongly affect the characteristics of the whole device.[8] Incident electrons are able to co-tunnel through the multiple barriers while the electron energy matches the discrete energy level in the quantum dot array.[14] With the increase of the gate voltage, the channel of electron transport opens widely, thereby reducing dopant barrier potential. The transport behavior of electrons evolves from that of quantum dots to quantum wires. The step-like current is observed beyond V_{FB}, where electrons go through a quantum wire. The plateau of the drain current becomes smooth with V_{DS} increasing.

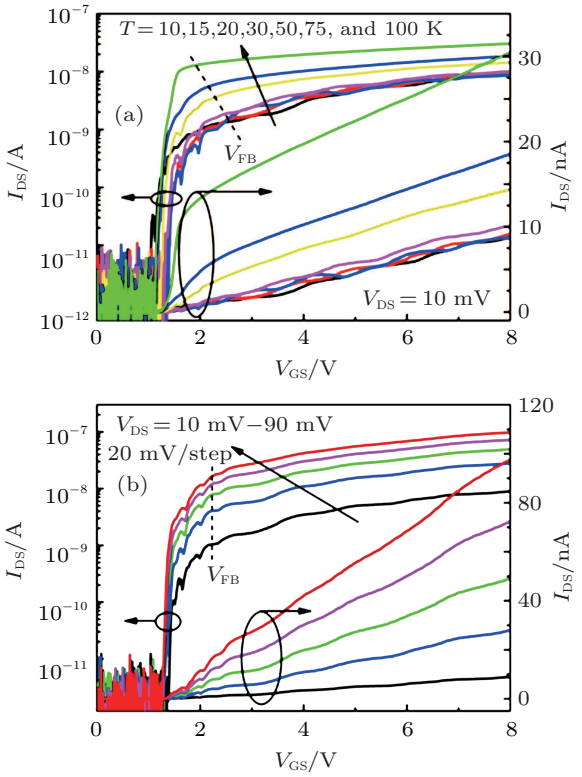


Fig. 4. (color online) I_{DS}–V_{GS} characteristics of a single channel JNT for (a) different temperatures at $V_{DS} = 10$ mV and (b) different drain voltages at $T = 15$ K.

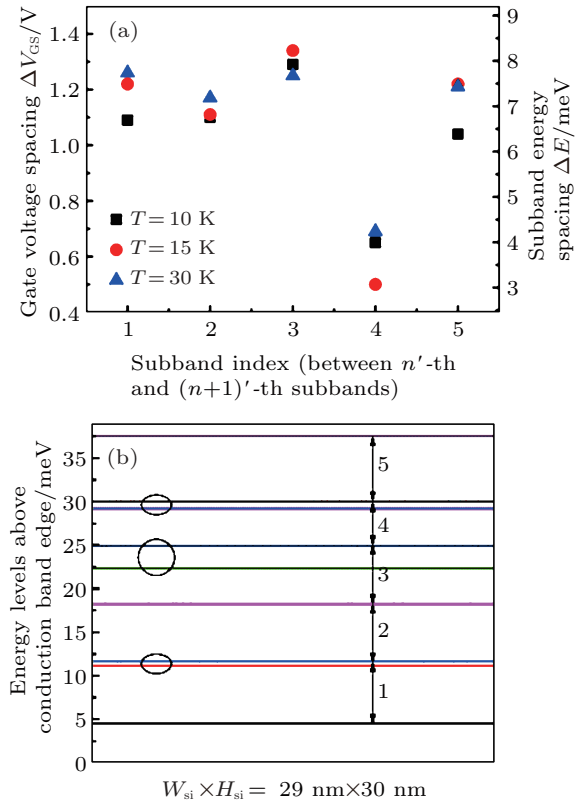


Fig. 5. (color online) (a) Gate voltage spacing ΔV_{GS} and subband energy spacing ΔE between adjacent transconductance peaks at 10 K, 15 K, and 30 K. (b) Discrete energy levels for a nanowire with a width of 29 nm and height of 30 nm, where the degenerated subbands are marked by numbers and double-arrow lines.

In order to understand the quantum behavior in the 1D channel, we estimate the subband energy spacing in Fig. 5(a) from the gate voltage spacing between adjacent transconductance peaks at 10 K, 15 K, and 30 K. The subband energy spacing is given by[15]

$$\Delta E_{\rm exp} = \frac{\pi\hbar^2 \cdot C_{\rm ox} \cdot \Delta V_{\rm GS}}{2q \cdot m^*}, \tag{1}$$

where m^* is the effective electron mass ($= 0.19m_0$), $C_{\rm ox}$ is the gate capacitance per unit area and is estimated to be 1.56×10^{-7} F/cm^2 (≈ 22 nm gate oxide). Using the rectangular well approximation, the discrete energy levels above the conduction band edge can be worked out. Figure 5(b) shows the discrete energy levels for silicon nanowire with a width of 29 nm and height of 30 nm. The spacing of the circled energy levels is within the thermal fluctuation at low temperatures. These adjoining subbands are indicated by numbers and double-arrow lines. The theoretical subband energy spacing is nearly equal to the experimental value.

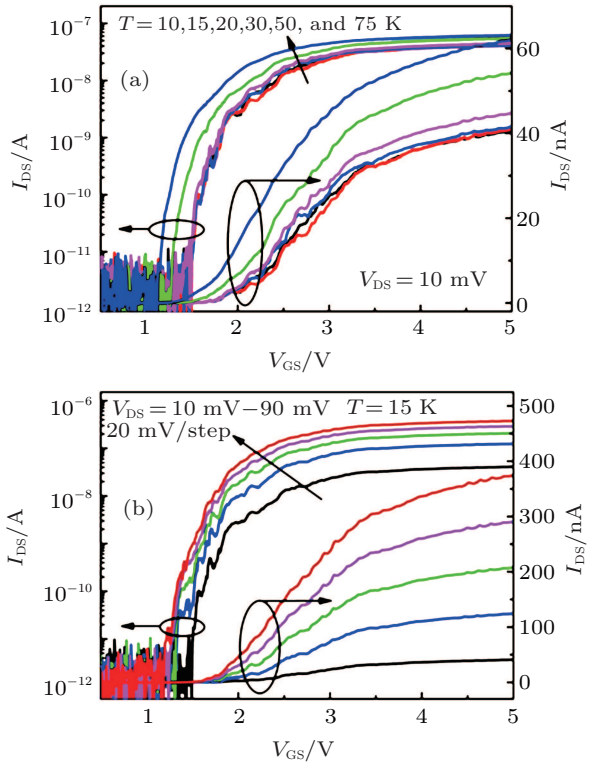


Fig. 6. (color online) $I_{\rm DS}$–$V_{\rm GS}$ characteristics of the five-channel JNT with an effective gate length of ~280 nm and (a) different temperatures (10 K, 15 K, 20 K, 30 K, 50 K, 75 K) at $V_{\rm DS} = 10$ mV and (b) different drain voltages at $T = 15$ K. Only tiny current oscillations are observed at high gate voltages.

In comparison with the single channel JNT, the multiple-channel JNT exhibits quite different drain current characteristics. Figure 6(a) shows the $I_{\rm DS}$–$V_{\rm GS}$ characteristic of the five-channel JNT at $V_{\rm DS} = 10$ mV and over temperatures ranging from 10 K to 75 K. Clear current oscillations below $V_{\rm FB}$ are observed at temperatures up to 75 K. At room temperature, as shown in Fig. 2(b), the drain current oscillations disappear and the curve of the $I_{\rm DS}$–$V_{\rm GS}$ becomes smooth. Figure 6(b) shows the $I_{\rm DS}$–$V_{\rm GS}$ characteristics of the five-channel JNT at $T = 15$ K and different drain voltages ranging from 10 mV to 90 mV with steps of 20 mV. In the multiple-channel JNT, each channel could form several electron islands at a low gate voltage. The current oscillations in the multiple-channel device originate from a superposition of oscillations from each nanowire. The current oscillations are dominated by the narrowest silicon nanowire in the five fins. At higher voltages than $V_{\rm FB}$, only tiny oscillation peaks of the drain current emerge, which is possibly due to the combination of the drain current from multiple channels with 1D quantum-confinement effects. Quantized energy levels are generated in all five nanowire channels. The positions of energy levels, which depend on the sizes of nanowires, are different in each channel. As clearly shown in Fig. 1(b), the width of each nanowire has an uncertain deviation in our multiple-channel JNT. Using the rectangular well approximation, quantized energy levels above the conduction band edge for nanowires with a height of 30 nm and widths of 15 nm, 20 nm, 25 nm, and 30 nm are shown as an example in Fig. 7. All quantized energy levels in the four nanowire channels are displayed together in the right-most column. Each energy level corresponds to a subband. Only tiny oscillation peaks of the drain current are observed as the actual subband spacing becomes small after collecting all the energy subbands. More subbands will be allowed to transport electrons with the increase of drain voltage in Fig. 6(b). The tiny oscillation peaks will be mixed together to make the drain current curve smooth.

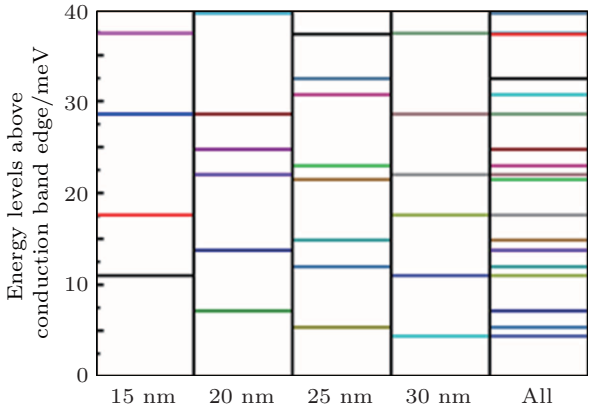


Fig. 7. (color online) Discrete energy levels for nanowires with a height of 30 nm and widths of 15 nm, 20 nm, 25 nm, and 30 nm. All discrete energy levels are displayed together in the right-most column.

4. Conclusions

In this paper, we have experimentally investigated quantum transport behaviors of single and multiple n-channel JNTs through temperature-dependent I–V characterizations. At lower voltages than $V_{\rm FB}$, the drain current oscillations are attributed to the Coulomb-blocked effect from quantum dots,

which are randomly formed in the just opened n-type 1D channel of silicon nanowires. The superposition of the drain current oscillations from multiple channels is dominated by the narrowest silicon nanowire. At voltages higher than V_{FB} 1D quantum characteristics are demonstrated by regular current steps in the single-channel JNT. However, only tiny oscillation peaks of the drain current are observed in the multiple-channel JNT. The JNTs with quantum-confinement effects provide novel building blocks for future quantum computers.

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