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Thermal effect of $Ge_2Sb_2Te_5$ in phase change memory device*

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In the fabrication of phase change random access memory (PRAM) devices, high temperature thermal processes are inevitable. We investigate the thermal stability of $Ge_2Sb_2Te_5$ (GST) which is a prototypical phase change material. After high temperature process, voids of phase change material exist at the interface between $Ge_2Sb_2Te_5$ and substrate in the initial open memory cell. This lower region of $Ge_2Sb_2Te_5$ is found to be a Te-rich phase change layer. Phase change memory devices are fabricated in different process conditions and examined by scanning electron microscopy and energy dispersive X-ray. It is found that hot-chuck process, nitrogen-doping process, and lower temperature inter-metal dielectric (IMD) deposition process can ease the thermal impact of line-GST PRAM cell.

Keywords: phase change memory, $Ge_2Sb_2Te_5$, thermal effect, failure analysis

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1. Introduction

Phase-change random access memory (PRAM) has drawn much attention as a promising nonvolatile memory for device applications, because of its faster data-storage speed and lower unit cost.[1,2] It operates based on the difference in resistance between amorphous and crystalline states. Accompanied by repetitive phase change programming, composition of phase change material changes and a significant volume change also happens which can result in considerable stress.[3]

Hong and Lee[4] introduced the failure mechanism of $Ge_2Sb_2Te_5$ (GST)-based phase change switching process and found a delaminated interface with decomposed GST chalcogenide. Shin *et al.*[5] performed the thermal stress analyses of $Ge_1Sb_4Te_7$-based PRAM devices, and predicted that failure was prone to occurring at the interface between phase change film and substrate SiO_2 film.

Besides the Joule heating during operation cycles, high temperature processes also subject PRAM cell to harsh thermal conditions and determine the characteristics of phase change materials during the fabrication of PRAM devices. As a consequence, research of thermal process impact on PRAM device is significant. In this paper, we discuss the thermal impact of high temperature processes on the PRAM device and find that thermal processes may result in GST decomposition and void. After a series of experiments, it is found that hot-chuck process, nitrogen-doping process, and lower-temperature inter-metal dielectric (IMD) deposition process could ease the thermal impact of GST film.

The rest of this article is organized as follows. In Section 2 we describe the experimental details of fabricating PRAM devices, whereas the defect resulting from thermal process and solutions to reduce the thermal impact of PRAM devices are presented in Section 3. Conclusions are presented in Section 4.

2. Experimental details

GST (TiN) thin films, each with a thickness of 100 nm (40 nm), were prepared on SiO_2 (Si) substrates by RF magnetron sputtering at ambient temperature (Orelikon CLN300 II). 100 nm–120 nm sized GST lines were fabricated using advanced standard 40-nm complementary metal–oxide–semiconductor device fabrication processes. For electrical and thermal passivation between the devices, a 20-nm linear SiN layer and a 500-nm IMD oxide layer were deposited using chemical vapor deposition (CVD) process. These IMD deposition processes were high temperature processes and had thermal impact on the line-GST PRAM devices. Finally, a top electrode contact (TEC) of copper was prepared after via contacts had formed.

Samples of PRAM cell were prepared using an FEI

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Dual Beam 835 focused ion beam (FIB). Cross-sectional microstructures within the device operating region were observed using a scanning electron microscope (SEM) (Hitachi S-5200) and tunneling electron microscope (TEM) (FEI TECNAI F20). The TEM included an energy-dispersive X-ray spectroscope (EDS) system, which was then used to investigate the composition of each region in the prepared structure.

3. Results and discussion

Figure 1(b) shows the cross-sectional TEM image of fabricated PRAM cell. GST lines are capped with a linear SiN and IMD SiO_2 layer using BEOL CVD process. After these thermal processes, GST is observed to be divided into two remarkable regions with different contrasts. These are an upper region beneath the top TiN layer marked as region 1, a lower small region 2 near the interface between GST and SiO_2 substrate. The different contrast of region 2 in the high-resolution bright-field image strongly implies that void formation is closely related to the decomposition of the GST layer.

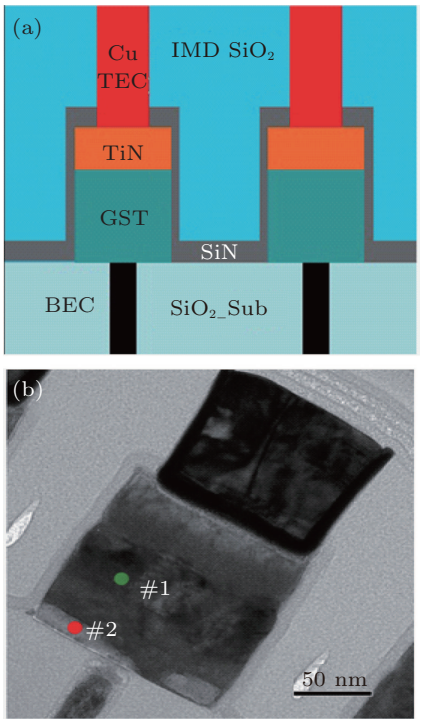


Fig. 1. (color online) (a) Schematic cross-sectional diagram and (b) TEM image of fabricated phase-change memory device, in which GeSbTe-based phase-change material films are coated with linear SiN and IMD SiO_2.

To compare compositional changes of the phase change material, EDS analysis is conducted in each of the regions. As shown in Fig. 2, there is a noticeable difference in element composition between the top (region 1) and bottom (region 2) regions. Ge, Sb, and Te are detected in region 1 as shown in Fig. 2(a). The compositions in region 2 are mainly Sb and Te while Ge peak nearly disappears as shown in Fig. 2(b). Meanwhile, the signal intensities of Sb and Te are stronger. This indicates that region 2 is formed by decomposition of the GST compound and out-diffusion of Ge.[6]

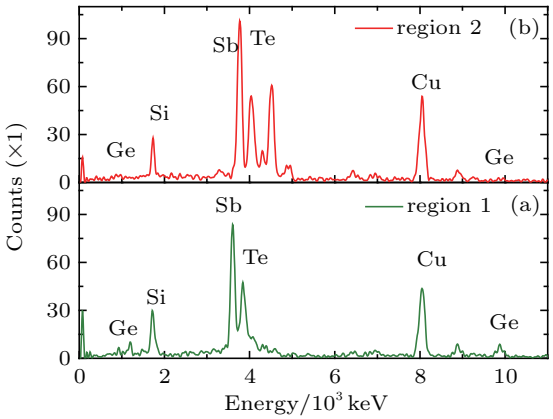


Fig. 2. (color online) EDS spectra of the regions 1 (a) and 2 (b) in Fig. 1(b).

Cross-sectional FIB-SEM characterizations are conducted along the GST line direction as shown in Fig. 3. Phase change layer is delaminated from substrate. This defect causes the initial open observed in PRAM device and can be explained by the thermal-induced motion and elemental segregation, occurring in the condition of high temperature thermal CVD process.[7] Voids form at the interface between phase change layer and bottom electrode, and grow at the interface between phase change layer and SiO_2 substrate under the thermal stress.

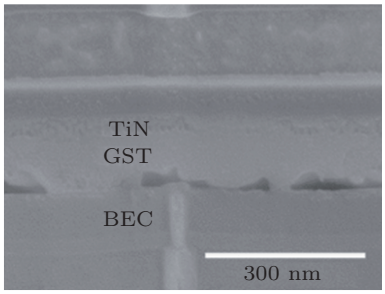


Fig. 3. Cross-sectional FIB-SEM of initial open PRAM cell.

There are two terms contributing to the mechanical stress in GST films according to their origins: the thermal stress and the phase-change stress. The thermal stress originates from the mismatch in the coefficient of thermal expansion (CTE) between one film and its surrounding materials. And the phase-change stress is induced by the change in the density due to phase transition from the amorphous to the crystalline phase. CTEs of GST measured by II-Mok Park[8] from substrate curvature method are $(13.3 \pm 1.39) \times 10^{-6}$ K^{-1} for the amorphous state and $(17.4 \pm 1.21) \times 10^{-6}$ K^{-1} for the crystalline state. Density change from amorphous to face centered cubic crystal structure, measured by Walter K. Njoroge,[7] is 6.86%. This kind of defect is different from that caused by Joule-heating. For Joule-heating-induced phase change progress, the thermal

stress is mainly confined at the interface between GST and bottom electrode by thermal boundary resistance (TBR).[5,9] The dissimilarity is the thermal distribution at wafer level for high temperature CVD process is more even than by Joule heating. It is acceptable that the stress distributions are also different. Different thermal and stress distributions cause the distinction between two kinds of defects.

There has been much effort to attempt to address this problem such as nitrogen doping process, hot chuck process, and lower temperature IMD deposition process. The doping process is regarded as an effective strategy to modify the various material properties of conventional GST materials for PRAM applications. It was reported that the properties of GST had been improved by nitrogen doping.[10,11] The hot chuck process employed a chuck heating process to obtain an as-deposited crystalline state GST. The temperature of IMD oxide deposition process is 430 °C, which is much higher than the crystallization temperature of GST. A 350-°C IMD deposition process is developed to try to reduce the thermal budget for GST process integration.

Phase change films are deposited by sputtering GST targets onto SiO_2(Si) substrates using a magnetron sputtering deposition system. Figures 4(a)–4(c) show the changes in the micro-structure of the GST films with increasing chuck temperature which was controlled at 25 °C, 230 °C, and 260 °C, respectively. Both films deposited at 230 °C and 260 °C show crystal structures which are characterized using X-ray diffraction analysis. As-deposited crystalline state GST makes sure that crystallization-induced volume change happens before the SiN coating process, in which way thermal stress in the following CVD process is reduced. For nitrogen-doped GST (NGST), films were deposited in the mixture of N_2 and Ar gases with a flow rate ratio N_2/Ar of 1:5. Microstructures of the NGST films each as a function of chuck temperature are shown in Figs. 4(d)–4(f). Each of the NGST films shows a retarded crystallization at a higher temperature[12,13] without noticeable difference between room temperature and high temperature.

In order to characterize the effect of N-concentration, line-NGST memory cells are fabricated each as a function of N_2/Ar gas ratio (Fig. 5). Voids form in the GST line after the thermal process when N_2/Ar gas ratio is 1:14 (Fig. 5(a)). As the N_2/Ar gas ratio increases, performance of PRAM cell is improved. The grain size of crystalline GST film is also refined by nitrogen implantation. The major reason may be that the formed Ge_3N_4 nitrides condense near grain boundaries of Ge–Sb–Te micro-crystals and suppresses the micro-material flow.[10,14] As the nitrogen concentration increases, the total volume of the nitrides increases and the atomic migration can be suppressed, which results in smaller grain size and more grain boundaries. When the N_2/Ar ratio reaches 1:3, memory cell shows no voids with refined grain as shown in Fig. 5(d).

Figure 6 shows the practicality of hot chuck process and low temperature IMD deposition process. The effect of hot chuck process is proved by a comparison between Fig. 6(a) and Fig. 6(c). N-doped (N_2:Ar = 1:5) GST films are deposited at 25 °C and 230 °C, respectively. Within the PRAM cells fabricated using ambient temperature-deposited NGST, a few cracks can be observed at the interface between NGST and SiO_2 substrate. IMD deposition processes with hot chuck (230 °C) N-doped (N_2:Ar = 1:5) GST PRAM cells at high

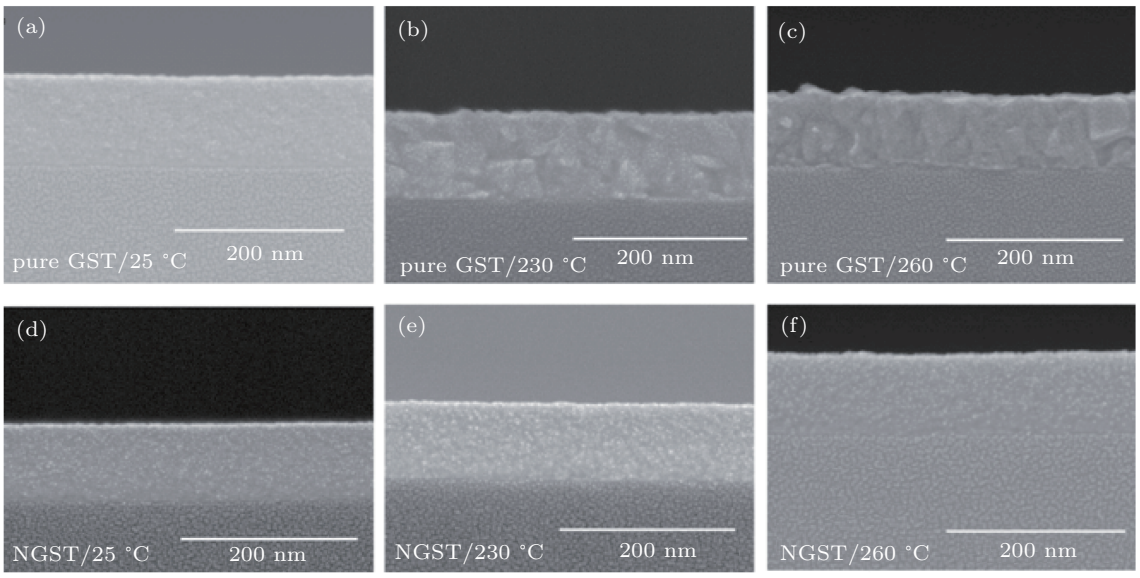


Fig. 4. Cross sections of as-deposited phase change films (GST and NGST) at various temperatures: (a) 25 °C for pure GST, (b) 230 °C for pure GST, (c) 260 °C for pure GST, (d) 25 °C for NGST, (e) 230 °C for NGST, and (f) 260 °C for NGST.

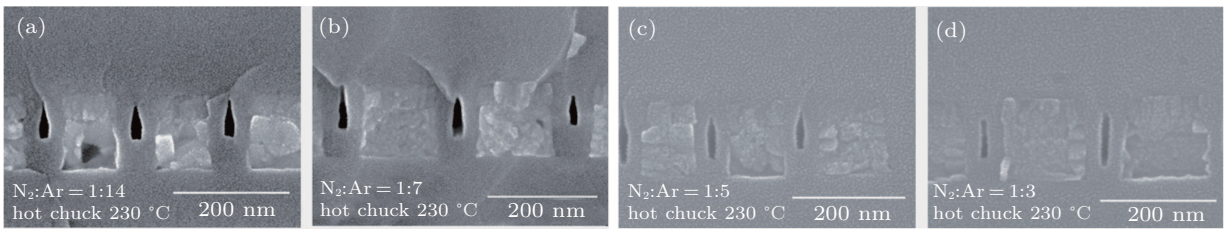


Fig. 5. SEMs of cross sections of fabricated line-GST PRAM cell with various N_2/Ar ratios of (a) 1:14, (b) 1:7, (c) 1:5, and (d) 1:3.

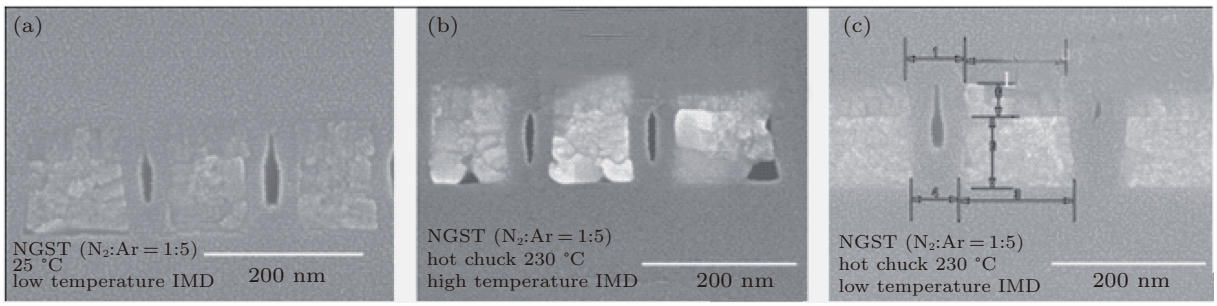


Fig. 6. SEM images of cross sections of fabricated line-GST PRAM cell with different GST deposition and IMD deposition processes: (a) NGST (N_2/Ar = 1:5), 25 °C, low temperature IMD process; (b) NGST (N_2/Ar = 1:5), hot chuck 230 °C, high temperature IMD process; (c) NGST (N_2/Ar = 1:5), hot chuck 230 °C, low temperature IMD process.

(Fig. 6(b)) and low (Fig. 6(c)) temperatures are compared. PRAM cells processed with high temperature IMD process suffer serious defects which mainly concentrate at the corner and lower surface of NGST line. The defect location is determined by temperature distribution and thermal stress distribution as mentioned above. Because of lower thermal budget in the process integration, PRAM cells with lower temperature IMD deposition process show better performance. It is acceptable to state that both hot chuck process and low temperature IMD deposition process are helpful to improve the PRAM cell quality.

4. Conclusions

In this article, cross sectional FIB-SEM analysis and EDS analysis confirm that initial open failure of line-GST PRAM cell is induced by the delamination at the interface between GST and the substrate, and the delamination is mainly driven by the decomposition of GST and out-diffusions of Ge and Sb, in the sequent thermal processes. In addition, we also investigate the impact of following thermal process on PRAM cell. Some ways such as hot-chuck process, N-dope process, and lower temperature IMD deposition process are proved to be effective to ease the thermal impact of GST film.

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