Forward and reverse electron transport properties across a CdS/Si multi-interface nanoheterojunction*

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The electron transport behavior across the interface plays an important role in determining the performance of optoelectronic devices based on heterojunctions. Here through growing CdS thin film on silicon nanoporous pillar array, an untraditional, nonplanar, and multi-interface CdS/Si nanoheterojunction is prepared. The current density versus voltage curve is measured and an obvious rectification effect is observed. Based on the fitting results and model analyses on the forward and reverse conduction characteristics, the electron transport mechanism under low forward bias, high forward bias, and reverse bias are attributed to the Ohmic regime, space-charge-limited current regime, and modified Poole–Frenkel regime respectively. The forward and reverse electrical behaviors are found to be highly related to the distribution of interfacial trap states and the existence of localized electric field respectively. These results might be helpful for optimizing the preparing procedures to realize high-performance silicon-based CdS optoelectronic devices.

Keywords: heterojunction, multi-interface nanoheterojunction, electron transport, silicon nanoporous pillar array (Si-NPA), CdS/Si-NPA

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1. Introduction

In the past decade, mainly aimed at the application of cadmium sulfide (CdS) thin films in fabricating solar cells,[1,2] light emitting diodes,[3] laser diodes,[4,5] and other optoelectronic devices,[6] the study of the electron transport properties across the interface formed between CdS thin film and the nether semiconductor has attracted considerable attention. Generally, the conduction behavior across a semiconductor heterojunction could heavily influence the device performances, such as efficiency and stability. So a clear understanding of the electron transport mechanism would be very important for the optimization of device producing process. Technically, the conduction mechanism of a typical semiconductor heterojunction could be clarified by measuring and analyzing its current density–voltage (J–V) curves.[7] Nevertheless, if the CdS thin film is grown on a nanostructured semiconductor surface, an untraditional, nonplanar, and multi-interface nanoheterojunction would be formed. In the case, the clarification of the electron transport mechanism would be a much more complicated and difficult work.

In the previous study, we reported the preparation and characterization of a CdS/Si nanoheterojunction based on a micron-nanometer hierarchical silicon substrate,[8,9] the silicon nanoporous pillar array (Si-NPA).[10] Through constructing an ITO/CdS/Si-NPA/Si/Ag structure, a prototype solar cell was prepared and an obvious photovoltaic effect was observed.[9] In the device, a relatively big open circuit voltage was obtained, which indicated the realization of high separation efficiency for photo-generated carriers. Although the big series resistance of the nanosystem leads to a small short circuit current and therefore low energy conversion efficiency, the obtaining of a CdS/Si-based solar cell with higher conversion efficiency is still hopeful. This might be realized through improving the CdS–Si interface status by optimizing the preparation processes. Considering the roles played by the conducting behavior in promoting the device performances, a deep and systemic study of the electron transport mechanism across the complex interface of CdS/Si-NPA is both important and necessary.

In this paper, we report that utilizing Si-NPA as a functional substrate, an n-CdS/p-Si multi-interface nanoheterojunction is prepared by a chemical bath deposition (CBD) method. The J–V curve is measured and the electron transport mechanisms under both forward and reverse biases are analyzed. An analysis based on the fitting results discloses that the electron transports under low forward bias, high forward bias, and reverse bias obey the Ohmic, space-charge-limited current (SCLC), and modified Poole–Frenkel (PF) models re-

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spectively. The forward and reverse electrical behaviors are found to be highly related to the distribution of interfacial trap states and the existence of localized electric field respectively. These results might be helpful for promoting the performances of silicon-based CdS optoelectronic devices through optimizing the preparation conditions.

2. Experiments

The Si-NPA samples were prepared by hydrothermally etching p-type, (111)-oriented single crystal silicon (sc-Si) wafers in the aqueous solution of hydrofluoric acid containing ferric nitrate. The resistivity of the initial sc-Si wafers was 0.007 $\Omega\cdot$cm $\sim$ 0.008 $\Omega\cdot$cm, with a boron doping concentration of $\sim 1\times10^{19}$ cm^{-3}. The details about the preparing conditions and processes have been reported previously.[10] The CdS thin film was grown on Si-NPA by a CBD method. Firstly, 0.003-mol cadmium chloride ($CdCl_2\cdot\frac{5}{2}H_2O$) was dissolved in the mixture solution of 15-ml 25%–28% ammonia ($NH_3\cdot H_2O$) and 65-ml de-ionized water. Then the solution was poured into a bath and stirred with a magnetic agitation. The bath was kept at 80 °C for 60 min. Next, 5-ml 0.1-mol/l ammonium chloride (NH_4Cl) and 5-ml 2-mol/l thiourea (H_2NCSNH_2) were slowly added into the bath sequentially. Five minutes later, Si-NPA was placed vertically into the solution to deposit CdS. The process lasted 40 min and then the sample was taken out, washed with deionized water, and dried in nitrogen atmosphere in sequence. At this stage, a layer of yellowish thin film was homogeneously grown on Si-NPA, which could be felt by naked eyes. To obtain properly crystallized and stabilized CdS, an annealing treatment was performed at 500 °C in high-purity argon atmosphere for 60 min. To carry out the subsequent electrical measurements, a transparent indium tin oxide (ITO) layer and an aluminum (Al) layer were grown as electrodes on the front side and the back side of CdS/Si-NPA by a magnetron sputtering and a vacuum evaporation method respectively. The device was annealed at 300 °C in Ar atmosphere for 60 min to realize a good Ohmic contact between the electrode and semiconductor.[11]

The morphological and structural characteristics of CdS/Si-NPA were studied by a field emission scanning electron microscopy (FESEM, JSM 6700F), a high-resolution transmission electron microscopy (HRTEM, JEM-2100), and a powder X-ray diffractometer (XRD, Panalytical X'Pert Pro) using Cu $k\alpha$ as the X-ray source ($\lambda = 1.5406$ Å). The dark J–V characteristics were measured with a Keithley SOURCEMETER-2400 and the measurements were carried out at room temperature.

3. Results and discussion

The XRD patterns of as-prepared CdS/Si-NPA and Si-NPA substrate are shown in Fig. 1. In the pattern for CdS/Si-NPA (pattern *a* in Fig. 1), five diffraction peaks located at 24.94°, 26.44°, 28.24°, 43.89°, and 52.11° were observed, which were indexed to the diffractions from the (100), (002), (101), (110), and (112) reflection planes of hexagonal CdS, respectively. According to Scherrer's formula[12] and based on the data corresponding to (002) peak, the average size of the grown CdS nanocrystallites (nc-CdS) is calculated to be $\sim$ 17.7 nm. For comparison, the XRD pattern for Si-NPA substrate is shown as pattern *b* in Fig. 1. Here only one diffraction peak corresponding to the diffraction from the (111) reflection plane of Si is observed. Compared with that for single crystal Si, the diffraction peak of Si-NPA is obviously broadened, which implies the existence of very fine Si nanocrystallites (nc-Si) in Si-NPA. Furthermore, the diffraction peak of Si is not observed in CdS/Si-NPA. This is attributed to the fact that the overall surface is covered by CdS film, which is evaluated to be several hundred nanometers in thickness and obstructs the penetration of X ray into the Si-NPA substrate.

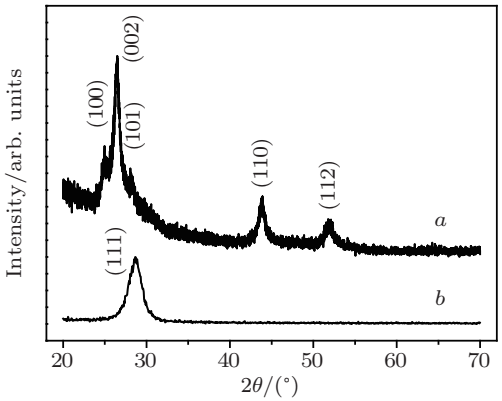


Fig. 1. XRD patterns of as-prepared CdS/Si-NPA (pattern *a*) and Si-NPA substrate (pattern *b*).

As has been reported previously,[10] Si-NPA has a unique silicon hierarchical structure consisting of vertically aligned nanoporous silicon pillars with the pore walls being the densely dispersed nc-Si encapsulated by silicon oxide. After CBD, the surface morphology of CdS/Si-NPA obtained by FE-SEM is shown in Fig. 2(a). Like the morphological characteristic of Si-NPA, a regular pillar array is also clearly observed on CdS/Si-NPA. The difference is that a continuous CdS film is formed on Si-NPA, which covers uniformly both the pillars and the valleys around the pillars. It should be noticed that above the uniform CdS film, some CdS particles with big sizes (over 200 nm) can be observed. Considering the fact that the average grain size evaluated by Scherrer's formula is only $\sim$ 17.7 nm, these big particles should be the agglomerates of

nc-CdS located above the continuous CdS film, which would not have a big influence on the electron transport across the interface. For further characterizing the interface microstructure formed between Si-NPA and the CdS film, which would have an effect on the transport characteristic across the CdS–Si interface, a piece of CdS thin film is cleaved from the sample and its bottom layer is observed by HRTEM. As shown in Fig. 2(b), where a lot of zones with distinct lattice fringes are clearly observed, with the sizes ranging from ~ 5 nm to 20 nm. Through measuring the fringe distances, these zones are determined to be randomly and alternately dispersed nc-Si or nc-CdS with different lattice orientations. Such an interfacial configuration may originate from the growing of nc-CdS into the nanopores of Si-NPA. This result indicates that the high-density nanoheterojunctions constructed by nc-Si or nc-CdS form in the interface region. Therefore in this sense, a non-planar and multi-interface CdS/Si heterojunction is prepared. Based on the above analysis, the overall structure of CdS/Si-NPA can be concluded as follows. The upper layer is a continuous thin film composing of nc-CdS or their agglomerates, the intermediate layer is the interface region constructed by randomly and alternately dispersed nc-CdS and nc-Si, and the bottom layer is the unfilled silicon nanoporous layer grown on sc-Si substrate. The clarification of the interface microstructure will be helpful to explain the electron transport properties obtained in the following experiments.

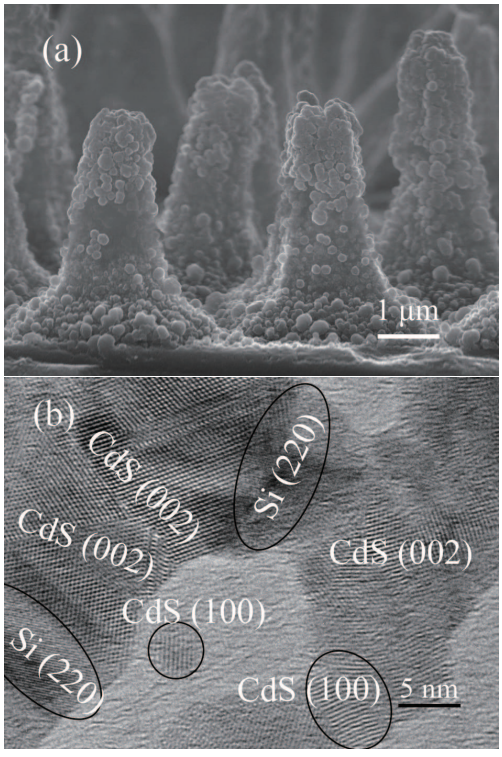


Fig. 2. Surface morphology of CdS/Si-NPA obtained by FESEM (a), and the interface microstructure of CdS/Si-NPA characterized by HRTEM (b).

To study the electrical properties of CdS/Si-NPA, a prototype device with a structure of ITO/CdS/Si-NPA/sc-Si/Al is constructed as schematically shown in the inset of Fig. 3. The experimental dark J–V curve measured at room temperature is given in Fig. 3. Here an obvious rectification behavior is observed, with an onset voltage of ~ 1.7 V at a current density of ~ 1.0 mA $\cdot$ cm^{-2}, a forward current density of ~ 194.70 mA $\cdot$ cm^{-2} at 3.6 V, a leakage current density of ~ 0.86 mA $\cdot$ cm^{-2} at a reverse bias of 3.6 V, and a breakdown voltage bigger than 6 V. The forward-to-reverse current ratio is calculated to be 226.4 at ± 3.6 V. All the parameters satisfy or approximately satisfy the technical requirements of practical applications. Because the contacts between Si-NPA and sc-Si, sc-Si and Al, and ITO and CdS were all proved to be Ohmic,[8,9,11] the rectification behavior can be due only to the nonplanar multi-interface nanoheterojunction formed between CdS and Si-NPA.

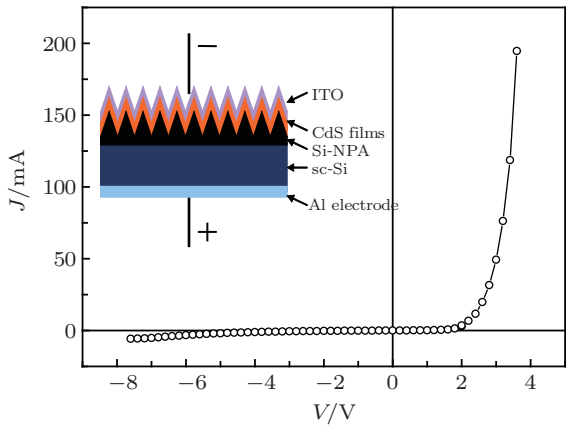


Fig. 3. (color online) Dark current–voltage characteristics of CdS/Si-NPA measured at room temperature. Inset: the schematic diagram of the CdS/Si-NPA device structure for measuring the electrical property.

From the J–V curve given in Fig. 3 it follows that the current density J increases very slowly with forward voltage increasing at a bias below 1.7 V, and then it increases steeply after that. This should result from the mode switch of the carrier injection at the interface with forward bias increasing. According to the basic theory about heterojunctions,[13,14] the J–V characteristic of a semiconductor heterojunction can be described as

$$J \propto V^m. \tag{1}$$

Here according to $m < 2$ or $m \geq 2$, the conduction behavior is usually classified as Ohmic regime or SCLC regime.[15,16] A pure SCLC mode follows the Child's law: $J \propto V^2$, which corresponds to the case of a material without or with a single discrete trap level.[13] To determine the value of m in the present experiment, the J–V curve (Fig. 3) under forward bias is transformed into a double logarithmic plot as depicted in Fig. 4, where there can be seen two distinct linear regions:

A and B. The two linear regions are separated at a transition bias $V_t = 1.38$ V. A simple calculation indicates that the slopes of the two fitting lines in regions A and B are ~ 1.33 and ~ 6.64 respectively. On the basis of the criterion for judging the conduction mode of a heterojunction,[17] the result indicates that below the V_t (region A), the carrier concentration is mainly contributed by thermally generated electrons, and the conduction mechanism is of Ohmic regime. With the bias increasing beyond the V_t (region B), the carrier concentration is mainly contributed by the external electron injection. Obviously, the value of the slope in region B (~ 6.64) deviates heavily from 2, the value that is for a pure SCLC regime. This indicates the presence of high-density trap states within the bandgap. Considering the fact that the device operating voltage is usually bigger than the onset bias (~ 1.7 V for CdS/Si-NPA, > 1.38 V), the overall conduction behavior for CdS/Si-NPA device should be dominated by the SCLC mechanism, in which the interfacial trap states can play an important role.

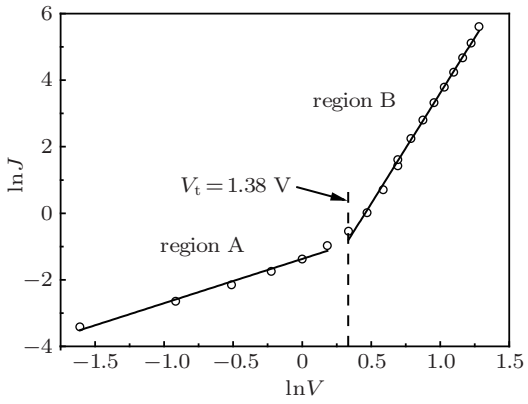


Fig. 4. The log–log plot of J–V characteristics of CdS/Si-NPA at forward bias, with J and V being in unit mA and in voltage respectively.

From the above judgement it follows that the status and distribution of the interfacial trap states near the Fermi level can make much contribution to the conduction behavior of CdS/Si-NPA nanoheterojunction. Under the frame of SCLC model, the distribution of partially-occupied trap states is controlled by an exponential function[18,19] beyond the transition voltage, and the corresponding J–V characteristics could be given as[20,21]

$$J/V = \left(\frac{q\mu n_0}{d_0}\right)\exp(SV), \tag{2}$$

in which d_0 represents the electrode spacing (~ 0.50 mm in the experiment), n_0 the density of thermally generated carriers, μ the electron mobility, q the electronic charge, and S a parameter defined as

$$S = \frac{2\varepsilon_0\varepsilon}{qN(E_F)kTd_0^2}, \tag{3}$$

with $N(E_F)$ being the density of localized trap states near the Fermi level, ε_0 the permittivity of free space, ε the constant of dielectric (CdS in the experiment), k the Boltzmann constant, and T the absolute temperature. The plot of logarithmic J/V versus V under forward bias is given in Fig. 5. Clearly, the ln(J/V)–V curve exhibits different characteristics in the voltage ranges of $V < 2.0$ V and $V \geq 2.0$ V. Combining with the relationship built up between S and $N(E_F)$ (Eq. (3)) indicates a continuously varying density ($V < 2.0$ V) and a constant density ($V \geq 2.0$ V) of the occupied trap states respectively. A simple calculation shows that the value of S, which is determined from the slope of the fitted line and keeps constant with $V \geq 2.0$ V, is ~ 2.15. This reflects that the density of the occupied trap states near the Fermi level does not change when the applied forward bias is bigger than 2.0 V, i.e., a saturation status is achieved. Correspondingly, the density of the wholly activated trap states is calculated to be $N(E_F) = 6.655 \times 10^{14}$ eV$^{-1}\cdot$cm^{-3}. Obviously, there exists a very high trap concentration in the interfacial zone of CdS/Si-NPA nanoheterojunction. These traps may originate from the formation of large quantities of sulfur vacancies or Cd interstitial atoms in CdS film,[9] or the lattice defects introduced in the growth process of CdS thin film because of the lattice mismatch between Si and CdS.[19] As can be seen from Fig. 4, SCLC is the dominant mechanism when $V > 1.38$ V. Therefore, one can assume that the trap states in a bias range of 1.38 V–2.0 V are partially occupied, while those at $V \geq 2.0$ V are completely occupied.

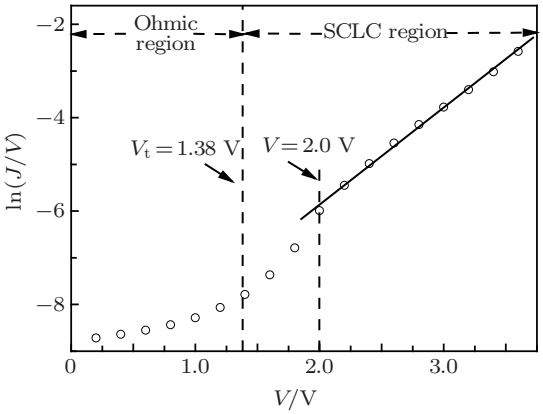


Fig. 5. The plot of semi-logarithmic J/V versus V characteristics of CdS/Si-NPA at forward bias, with J and V being in unit mA and in voltage respectively.

The reverse electron transport properties are also important factors in determining the integral performance of a heterojunction device. Among the technical parameters, the leakage current density and the reverse breakdown voltage are the two most concerned ones. Usually, in a heterojunction with trap, various Coulombic potential barriers are formed between the trap levels and the conduction or valence bandedges.[19]

These barriers make the carriers confined in the trap states and do not contribute to the conductivity. Nevertheless, the trapped carriers can simultaneously introduce localized electric field and cause the potential barriers to lower by the PF effect.[17,22,23] According to the theory, the J–V characteristic for a heterojunction under reverse bias can be described as[20,22,24]

$$J = A^* \exp\left(\frac{\phi_s}{kT}\right) \exp\left(\frac{\beta_{\rm PF}}{kT}\sqrt{\frac{V}{d}}\right), \tag{4}$$

with T being the absolute temperature, k the Boltzmann constant, d the thickness of the heterojunction, A^* the theoretical Richardson constant, ϕ_s the zero-bias barrier height, and $\beta_{\rm PF}$ the PF coefficient defined by

$$\beta_{\rm PF} = \left(\frac{q^3}{\pi\varepsilon}\right). \tag{5}$$

In the present nanosystem, the doping concentration of the initial sc-Si is much higher ($\sim 1\times10^{19}$ cm^{-3}) than that of as-grown CdS thin film ($< 10^{15}$ cm^{-3}), the space charge zone should be mainly located in the CdS film. Therefore A^* should be chosen to be the same as that for CdS, which is ~ 24 A$\cdot$cm$^{-2}\cdot$K^{-2} in value.[25] Then the theoretical PF coefficient $\beta_{\rm PF}$ is calculated to be $\sim 2.228\times10^{-5}$ eV$\cdot$m$^{1/2}\cdot$V$^{-1/2}$. To obtain the actual value of the PF coefficient of CdS/Si-NPA, the semilogarithmic plot of the experimental reverse current density J versus $V^{1/2}$ is presented in Fig. 6. A simple fitting result reveals that the $J\sim V^{1/2}$ curve can be characterized by two linear segments, with the slopes in regions I (with low reverse bias) and II (with high reverse bias) being ~ 3.4 and ~ 2.2, respectively. Based on the slope values in the two linear regions, the corresponding PF coefficients are determined to be $\beta_{\rm I} = 4.524\times10^{-5}$ eV$\cdot$m$^{1/2}\cdot$V$^{-1/2}$ and $\beta_{\rm II} = 3.157\times10^{-5}$ eV$\cdot$m$^{1/2}\cdot$V$^{-1/2}$ respectively. Obviously, there is a big difference between the experimental and theoretical PF coefficients: the values of $\beta_{\rm I}$ and $\beta_{\rm II}$ are ~ 2.03 and ~ 1.41 times bigger than the theoretical value $\beta_{\rm PF}$ respectively. To explain the difference theoretically, Gould and Bowler put forward the modified PF model.[26] In this model, the enhancement of $\beta_{\rm PF}$ is due to the existence of localized electric fields in the vicinity of the traps, such as donor or acceptor centers.[22] This may be just the case occurring in CdS/Si-NPA. Considering the preparation process of CdS/Si-NPA, the introducing of high-density trap states seems to be unavoidable, such as the structural defects caused by the interfacial stress and lattice mismatch, and the sulfur vacancies or Cd interstitial atoms introduced by the non-stoichiometric growth of CdS thin film. Clearly, the incorporation of these traps into the interfacial zone of CdS/Si-NPA can cause the potential barriers to lower with a field assistance, and thereby lead to the raising of the leakage current density and the reduction of the breakdown voltage. Such a consequence is almost surely harmful to the performance of the device based on CdS/Si-NPA. Fortunately, these effects may be practically reduced through controlling the preparation conditions or performing post-treatments. A positive example has demonstrated that through preparing CdS thin films in a sulfur-enrichment atmosphere, the trap states introduced by sulfur vacancies or Cd interstitial atoms could be greatly reduced.[27,28]

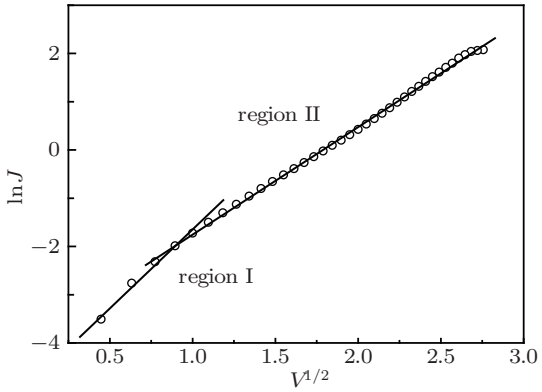


Fig. 6. The plot of semi-logarithmic current density J versus $V^{1/2}$ characteristic of CdS/Si-NPA at reverse bias, with J and V being in unit mA and in voltage respectively.

4. Conclusion

In this paper, an untraditional, nonplanar, and multi-interface CdS/Si nanoheterojunction is prepared by growing nc-CdS thin film on Si-NPA through using a CBD method. Through measuring the J–V curve of the nanosystem, an obvious rectifying effect is observed. Based on the results of model analysis about the forward and reverse conduction behaviors, the electron transport mechanisms are attributed to being the Ohmic regime (under low forward bias), SCLC regime (under high forward bias), and a modified PF regime respectively. The high-density trap states formed in the interfacial zone are determined to be the destructive factors in determining the integral device performances, but the resulting damage may be compensated or controlled under a reasonable level through optimizing the preparing process or adopting suitable post-treatments. Our results can provide some reference directions for optimizing the preparing conditions of untraditional, nonplanar, and multi-interface nanoheterojunctions with unique physical properties.

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