Experimental verification of the parasitic bipolar amplification effect in PMOS single event transients*

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The contribution of parasitic bipolar amplification to SETs is experimentally verified using two P-hit target chains in the normal layout and in the special layout. For PMOSs in the normal layout, the single-event charge collection is composed of diffusion, drift, and the parasitic bipolar effect, while for PMOSs in the special layout, the parasitic bipolar junction transistor cannot turn on. Heavy ion experimental results show that PMOSs without parasitic bipolar amplification have a 21.4% decrease in the average SET pulse width and roughly a 40.2% reduction in the SET cross-section.

Keywords: single event effect, single event transient, parasitic bipolar amplification, heavy ion experiments

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1. Introduction

Single event transients (SETs) are the main source of soft errors for integrated circuits (ICs) in the space environment, as they may propagate along the combinational logic and corrupt the downstream sequential logic once they are latched. SET-induced soft errors are becoming common due to the lower operating voltage, higher operating frequencies, and smaller nodal capacitance with technology scaling.[1,2] Therefore, it is critical to understand the generation of SETs and develop design guidelines and hardening methods.

One of the key factors that determines the probability of SETs being latched is the pulse width, which is directly related to the charge collection. Charge collection is usually the sum of drift, diffusion and parasitic bipolar amplification components.[3–5] Previous research has shown that the SETs generated in PMOSs dominate the overall SETs,[6–8] thus the heavy-ion response mechanisms for PMOSs demand more studies and analysis. To understand the single-event charge collection and distinguish the bipolar effect from the other two components (drift and diffusion), simulations were conducted using devices with and without the source implant (i.e., with and without the emitter junction of the parasitic bipolar transistor).[9–11] Another method was proposed to analyze the contribution of the bipolar effect to charge collection by comparing the SETs generated in a two-transistor inverter and a three-transistor inverter.[12,13] Though simulation characterization of the parasitic bipolar amplification component has been accomplished with these techniques, little experimental work has been done. Heavy ion experiments using a single device show that bipolar amplification can result in increased charge collection.[14] However, this component of charge collection in a single device is different from that in the circuit due to the different drain voltage changes.[10] Thus it is necessary to experimentally evaluate the contribution of parasitic bipolar amplification to circuit SETs.

In this paper, we proposed a P-hit target chain in a special layout design, in which the parasitic bipolar amplification could be suppressed. Experimental data show that heavy-ion striking on PMOSs with charge collection composed of only drift and diffusion results in a significantly reduced SET pulse width and cross-section.

2. Experimental setup and result

To verify the impact of parasitic bipolar amplification on PMOS SET performance, a test chip was fabricated in a commercial 180-nm bulk complementary metal oxide semiconductor (CMOS) process. The test structure was constructed by two P-hit target circuits and a pulse capture circuit, as shown in Fig. 1. The pulse capture circuit, which had a measurement range of 3 ns and a resolution of 60 ps, was based on the self-triggered SET pulse width measurement technique first described in Ref. [15]. In both target circuits, to provide a large sensitive area while mitigating the effect of propagation induced pulse broadening (PIPB),[16] four chains of 300 P-hit blocks were ORed together, composed of a total of 1200 target blocks.

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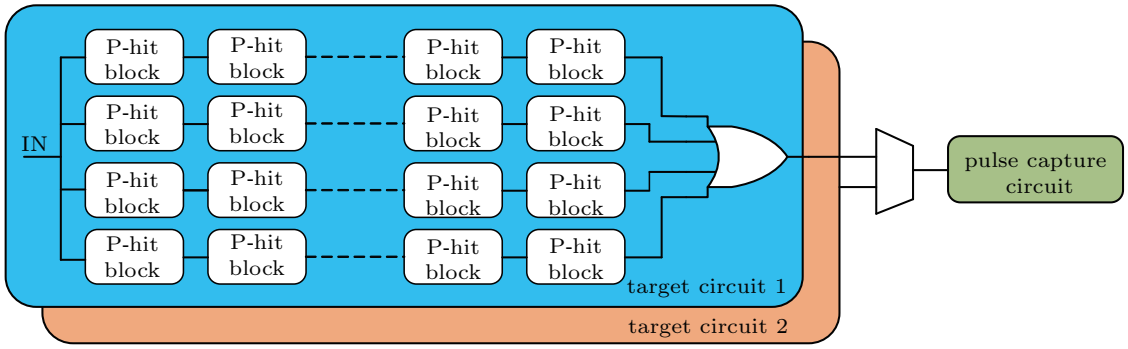


Fig. 1. (color online) Block diagram of the test structure consisting of two target circuits and a pulse capture circuit.

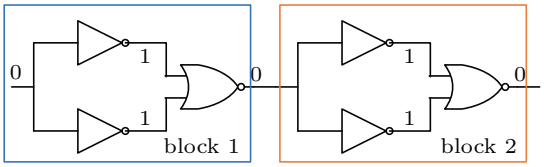


Fig. 2. (color online) Schematic of two of the blocks of P-hit.

The P-hit target block shown in Fig. 2 was first proposed in Ref. [7]. In this circuit, the input is held logic LOW. An SET generated by an individual ion strike on any one of the inverters cannot propagate through the NOR gate, because the other input of the NOR gate is maintained at logic HIGH. Therefore, only the SETs in the PMOS connected to the output of the NOR cell can propagate through the target chain and be measured by the capture circuit. The inverters and NOR gate in P-hit blocks were carefully designed to have equal gate loads.

The difference between the two P-hit target chains was the layout of the P-hit block. For the first chain, which is referred to as the normal layout (NL) chain, the two PMOSs (PA and PB) in the NOR gate are placed in the same N-well, as shown in Fig. 3(a). Figure 3(b) shows the layout of the P-hit block in the second chain, which is referred to as the special layout (SL) chain. The SL chain was identical to the NL chain in schematic, except that the two PMOSs in the NOR gate were placed in different N-wells. The PB connected to the output of the NOR gate is in the same place as that in the NL chain, and the PA connected to the VDD has been moved to another N-well. In short, for the NL chain, PA and PB lie adjacent to each other, while for the SL chain, they are spatially isolated.

Heavy ion testing was performed at the HI-13 tandem accelerator in China's Institute of Atomic Energy using the 9.5-MeV/amu beam on the two target circuits described above. Both the number and pulse width of SETs were collected at normal incidence.

A comparison of SET pulse widths for NL and SL chains is shown in Fig. 4. The data were collected using Titanium with the linear energy transfer (LET) of 20.9 MeV·cm^2·mg^{-1}. In this figure, the cross-section is defined as the number of SETs captured divided by a fluence of 1×10^7 ions/cm^2. As can be seen from this figure, the peak of the distribution for NL chain occurs at a larger pulse width (420 ps) compared to the peak of the distribution for the SL chain (360 ps). Meanwhile, a little more SETs were captured in the NL chain than in the SL one.

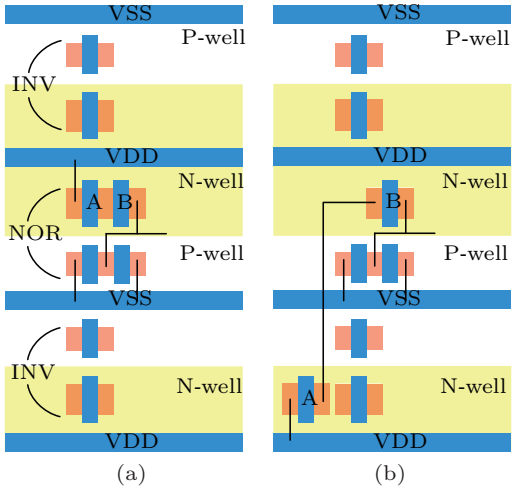


Fig. 3. (color online) Top-down view of the P-hit block in (a) normal layout and (b) special layout.

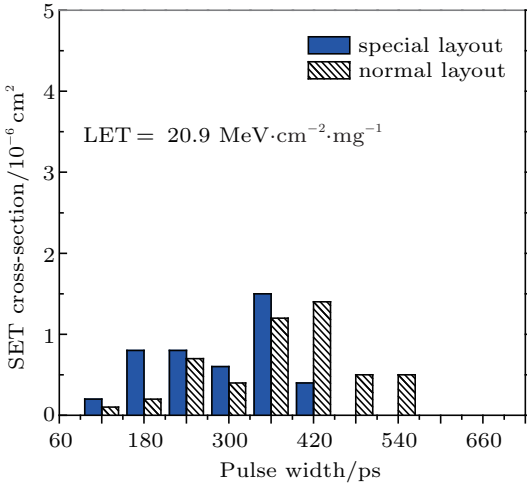


Fig. 4. (color online) Distribution of SET pulse widths generated in P-hit target chains by Titanium at normal incidence.

In Fig. 5, SET pulse width data collected using Bromine with LET of 41.2 MeV·cm^2·mg^{-1} is shown. A similar but

much more distinct trend can be observed in the histograms due to the increased LET and consequently increased SET numbers. The SET pulse width distribution for the NL chain shows a clear shift toward a longer SET width compared with the SL one. The average pulse widths for NL and SL chains were 601.77 ps and 472.26 ps, respectively. Meanwhile, the number of SET pulses captured in the SL chain was significantly less than that in the NL chain, with a roughly 40.2% reduction in the SET cross-section.

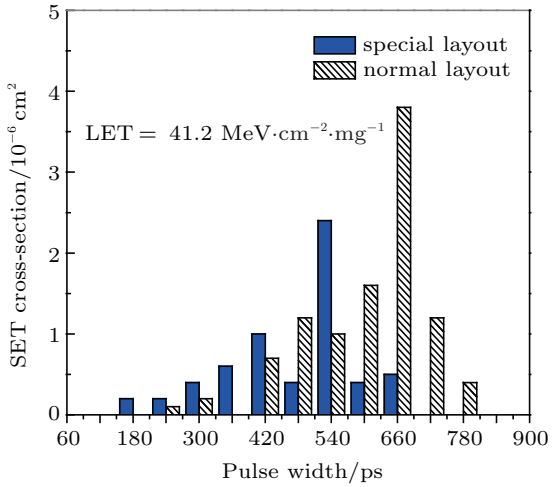


Fig. 5. (color online) Distribution of SET pulse widths generated in P-hit target chains by Bromine at normal incidence.

The experimental data indicate that the layout of the P-hit block has a remarkable effect on the circuit's SETs performance, although both target chains have the same sensitive area (the drain region of the PB). Because the two target chains are identical to each other, there could be little difference during the SET propagation. Thus the main reason for this behavior may lie in the SET generation. Using TCAD simulation, the mechanism responsible for this phenomenon is studied.

3. Discussion

Due to the good look-inside capability, three-dimensional mixed-mode technology computer aided design (TCAD) simulation has been proven to be a useful tool to investigate the mechanism of a single event effect in devices.[17–19] To examine the single event charge collection and pulse width in different layouts, Sentaurus SPICE/3D TCAD mixed-mode simulations were carried out in a 7-stage chain, as shown in Fig. 6. Both the PMOSs (PA and PB) at the 2nd stage were simulated in 3D device models, which were calibrated to the 180-nm PDK (process design kit) of the commercial dual-well CMOS process, while the remainder of the simulation setup was implemented in SPICE models. The 3D PMOSs structure for the simulation is shown in Fig. 7. For the normal layout simulation, PA and PB are placed in the same N-well, while for the special layout simulation they are placed in N-well-A and N-well-B respectively. The input for the chain was held LOW so that both PA and PB were OFF. The strike location was at the center of the drain in PB. The simulations were performed with heavy ion LET value ranging from 5 MeV·cm^2·mg^{-1} to 50 MeV·cm^2·mg^{-1}. The SET pulse width created by the ion strike was measured at the output of the 7-stage chain.

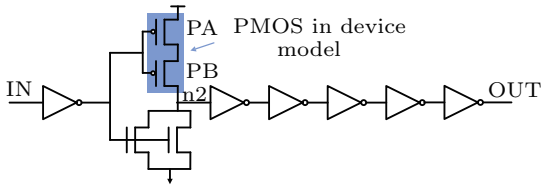


Fig. 6. (color online) SPICE/3D TCAD mixed-mode simulation setup.

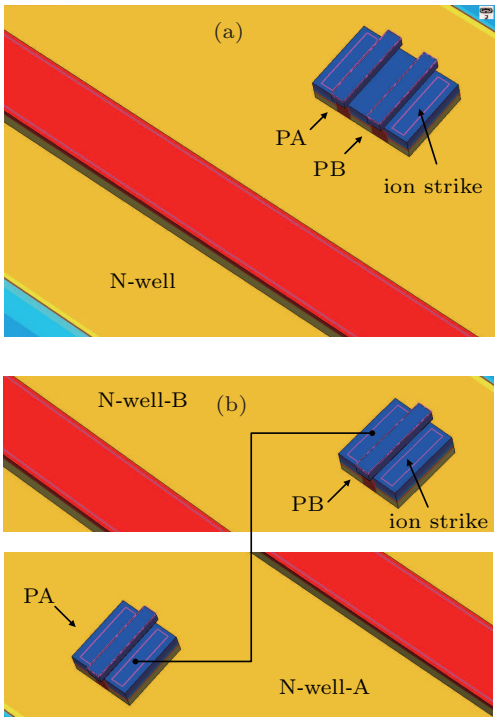


Fig. 7. (color online) Two PMOS device models (a) in the same N-well, (b) in different N-wells.

The following physical models were used in the simulations: Fermi–Dirac statistics, band-gap narrowing effect, doping dependent SRH and Auger recombination, and the Carrier–Carrier scattering mobility model. The incident heavy ions were modeled using a Gaussian radial profile with a characteristic 1/*e* radius of 50 nm and Gaussian temporal profile with a characteristic decay time of 0.25 ps. Simulations were carried out using the YINHE computing cluster in the National University of Defense Technology.

A comparison of PMOS pulse widths for the normal layout and special layout is shown in Fig. 8. As can be seen in the figure, the pulse width created in the special layout is

smaller than that in the normal layout. The difference in pulse width is insignificant when the LET is 5 MeV·cm^2·mg^{-1}, and becomes distinct at higher LETs. The pulse captured in the special layout is about 531 ps when the LET is 40 MeV·cm^2·mg^{-1}, showing a 37.7% reduction in the pulse width when compared with the pulse observed in the normal layout, which is about 852 ps. The mixed-mode simulation results are in agreement with the experiment result in that the SET pulse widths are shorter for the target chain in the special layout than the SETs generated in the normal layout one. In Fig. 8, it can be seen that the SET pulse width of the special layout reaches a peak of 531 ps when the LET is 40 MeV·cm^2·mg^{-1} and then decreases with LET. A similar phenomenon was also observed in a "three-transistor inverter chain" and the mechanism responsible for this behavior was the "pulse attenuation effect".[20] With LET increasing, the amplitude of the SET pulse in the special layout could decrease and consequently cannot completely propagate through the inverter chain, resulting in smaller SET pulses.

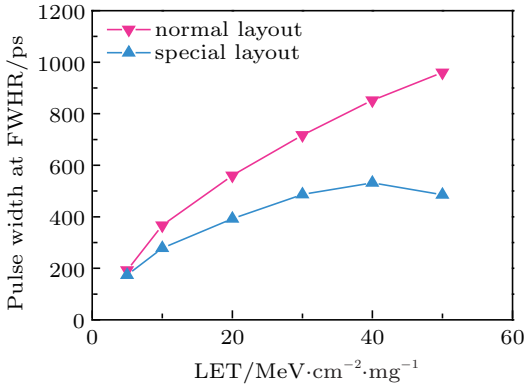


Fig. 8. (color online) SET pulse widths at the output of the 7-stage chain versus LET values for the normal layout and special layout.

This significant discrepancy in SET pulse width between the two target chains with different layouts can be attributable to the parasitic bipolar amplification. In a normal layout, a large number of surplus ionized electrons due to particle strike are confined to the N-well region, causing the N-well potential to fall. As a consequence, the P+ source of PA and the N-well potential barrier is lower, and the parasitic P$^+$–N–P$^+$ bipolar junction transistor (BJT) will turn on. The source of the PA (the emitter of the parasitic BJT) will inject holes into the channel (the base of the parasitic BJT). These holes can be collected by the drain of the PB (the collector of the parasitic BJT) and added to the initial charge collection. This component is referred to as the parasitic bipolar amplification.[3]

The parasitic bipolar amplification is directly related to the distance between the source of the PA and drain of the PB. Additional simulations were performed with the device structure shown in Fig. 9. In this structure (referred to as the separated layout), the serial PMOSs are placed in the same N-well, but they are separated by the shallow trench isolation (STI) with the drain-center-to-drain-center distance varying from 0.84 μm to 1.48 μm. Figure 10 depicts the hole current of the PA source in this design, along with those in the normal layout and special layout designs. As can be seen from this figure, the source of the PA in the normal layout has the largest hole current due to the minimum distance between the source of the PA and the drain of the PB, and the hole current decreases with the increased distance. With a distance of 1.48 μm, the source of the PA injects a few holes into the channel, which means that the heavy-ion induced potential perturbation of the N-well almost reaches its spatial limitation. In the special layout, which can be considered as an extreme situation, the PA and PB are placed in different N-wells. The PA source and N-well-A potential barrier cannot be influenced by the potential perturbation of N-well-B and consequently the parasitic bipolar transistor cannot turn on. Thus the bipolar amplification is eliminated and the hole injection from the PA source does not occur.

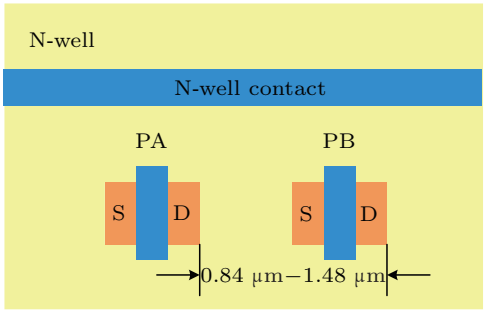


Fig. 9. (color online) Two PMOSs in the same N-well with drain-center-to-drain-center distance varying from 0.84 μm to 1.48 μm.

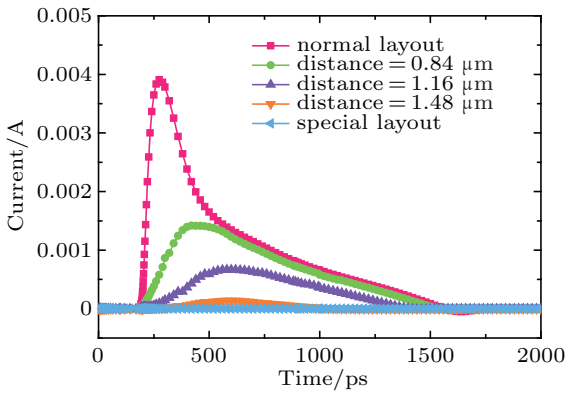


Fig. 10. (color online) Hole current of the PA source for the normal layout, separated layout, and special layout with a strike of LET 40 MeV·cm^2·mg^{-1}.

SET pulse width is dependent on the charge collection at the drain. According to the discussion above, the charge collection in the normal layout is composed of the drift, diffusion, and bipolar amplification effect. In the special layout, the drain

of the PB collects less charge due to the mitigation of bipolar amplification. Therefore, the SETs are much shorter than in the normal layout. In particular, some short SETs may attenuate during the propagation, resulting in a reduced SET cross section compared to the circuit in the normal layout. The experiment and simulation results demonstrate that the parasitic bipolar amplification has a great impact on the PMOS SETs performance.

4. Conclusion

In this paper, the contribution of parasitic bipolar amplification to PMOS single event transients is experimentally verified using two P-hit target chains in normal and special layout design. SET pulse width data collected indicated that target chain without parasitic bipolar amplification has a 21.4% decrease in the average SET pulse width and a roughly 40.2% reduction in the SET cross-section. Experimental and simulation results demonstrate that the parasitic bipolar amplification has a great impact on the PMOS SETs performance, which indicates that reducing the contribution of this component to charge collection could be an efficient method to mitigate SETs.

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