Hybrid phase-locked loop with fast locking time and low spur in a 0.18-μm CMOS process*

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We propose a novel hybrid phase-locked loop (PLL) architecture for overcoming the trade-off between fast locking time and low spur. To reduce the settling time and meanwhile suppress the reference spurs, we employ a wide-band single-path PLL and a narrow-band dual-path PLL in a transient state and a steady state, respectively, by changing the loop bandwidth according to the gain of voltage controlled oscillator (VCO) and the resister of the loop filter. The hybrid PLL is implemented in a 0.18-μm complementary metal oxide semiconductor (CMOS) process with a total die area of 1.4×0.46 mm^2. The measured results exhibit a reference spur level of lower than -73 dB with a reference frequency of 10 MHz and a settling time of 20 μs with 40 MHz frequency jump at 2 GHz. The total power consumption of the hybrid PLL is less than 27 mW with a supply voltage of 1.8 V.

Keywords: phase-locked loop (PLL), fast locking time, low spur, complementary metal oxide semiconductor (CMOS)

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1. Introduction

Phase-locked loops (PLLs) have been widely applied to recover and synthesize the frequency and phase in versatile wireless devices and systems, including frequency synthesizers, clock generators, high-speed data communication, and power generation systems.[1–5] Low spur signal and fast locking time are two key requirements in nearly all applications of PLLs. The most straightforward way to suppress the reference spurs of a PLL is to reduce its loop bandwidth. Unfortunately, the settling time of a PLL is inversely proportional to the loop bandwidth; that is, a narrow loop bandwidth of PLL leads to a slow switching speed.[1] Single-path PLLs can be easily designed with wide loop bandwidths for providing a fast locking time, but they suffer from high reference spurs.[1] PLLs with separate fine and coarse tuning paths, termed dual-path PLL, have been proposed to implement low reference spurs owning to the low VCO gain.[6–8] However, one difficulty of the dual-path PLLs is to achieve a fast locking settling time since the loop bandwidth of coarse path should be much smaller than that of a fine path to ensure stability.[6–8]

To overcome the conflict between the fast locking time and the low spur in conventional PLLs, an adaptive loop bandwidth control method for PLLs has been studied extensively.[9–15] The PLL loop bandwidth can be expressed as $I_{\rm CP}K_{\rm VCO}R/(2\pi N)$, where $I_{\rm CP}$ is the charge pump (CP) current, $K_{\rm VCO}$ is the gain of the VCO, R is the resistor loop filter (LF), and N is the frequency division radio. One can alter the loop bandwidth readily by changing the LF resister R, the CP current $I_{\rm CP}$, as well as the frequency division ratio N. So far, the adaptive loop bandwidth control method has only been studied in single-path PLLs[9–13] or dual-path PLLs,[14,15] where the high reference spurs of single-path PLLs and the slow locking settling time of dual-path PLLs cannot be completely overcome. Therefore, we propose and demonstrate a new architecture with a wide-band single-path PLL and a narrow-band dual-path PLL in a transient state and a steady state, respectively. Such type of hybrid PLL can be used for combining the advantages of both the single-path PLL and the dual-path PLL, which would result in a faster locking time and a lower spur than the adaptive loop bandwidth single-path PLLs or dual-path PLLs. In addition, the CMOS process has been widely used to implement microwave devices, circuits, and systems, showing advantages such as high integration capability, low cost, low power consumption, and ease of mass production.

In this paper, we propose a 0.18-μm CMOS hybrid PLL architecture that combines a wide-band single-path PLL and a

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narrow-band dual-path PLL in the transient and steady states, respectively. It shows better performance than the conventional single-path and dual-path PLLs. The advantages of this architecture are that the VCO gain and the LF resistor can be well controlled to obtain fast locking time in the transient state and lower reference spur suppression in the steady state, which makes it easy to combine the advantages of single-path PLL and dual-path PLL, while eliminating their disadvantages.

2. Hybrid PLL architecture and layout

The hybrid PLL architecture, as shown in Fig. 1, can be realized by combining a wide-band single-path PLL and a narrow-band dual-path PLL in the transient and steady states, respectively. The proposed hybrid PLL is a closed loop system composed of a PFD, a CP, a lock detector (LD), switches (SW 1-5), an LF, a VCO, a rail-to-rail operational amplifier, and a divider (N), as shown in Fig. 1(a). The loop bandwidth of the PLL in the transient state is M times wider than that in the steady state.

Figure 1(b) shows the steady state when the LD provides a signal of logic 0, that is, switches 2, 3, and 5 (SW2, SW3, SW5) are open and switches 1 and 4 (SW1, SW4) are closed, and thereby the PLL becomes a dual-path PLL. The idea here is to use an effective low VCO gain ($K_{\rm VCO}/r$) and a high LF resistor (MR) to obtain a dual-path PLL with narrow bandwidth and consistent phase margin, where r is the ratio of the VCO gain of the coarse-tuning path over that of the fine-tuning path. If $M=\sqrt{r}$, the loop bandwidth can be decreased by a

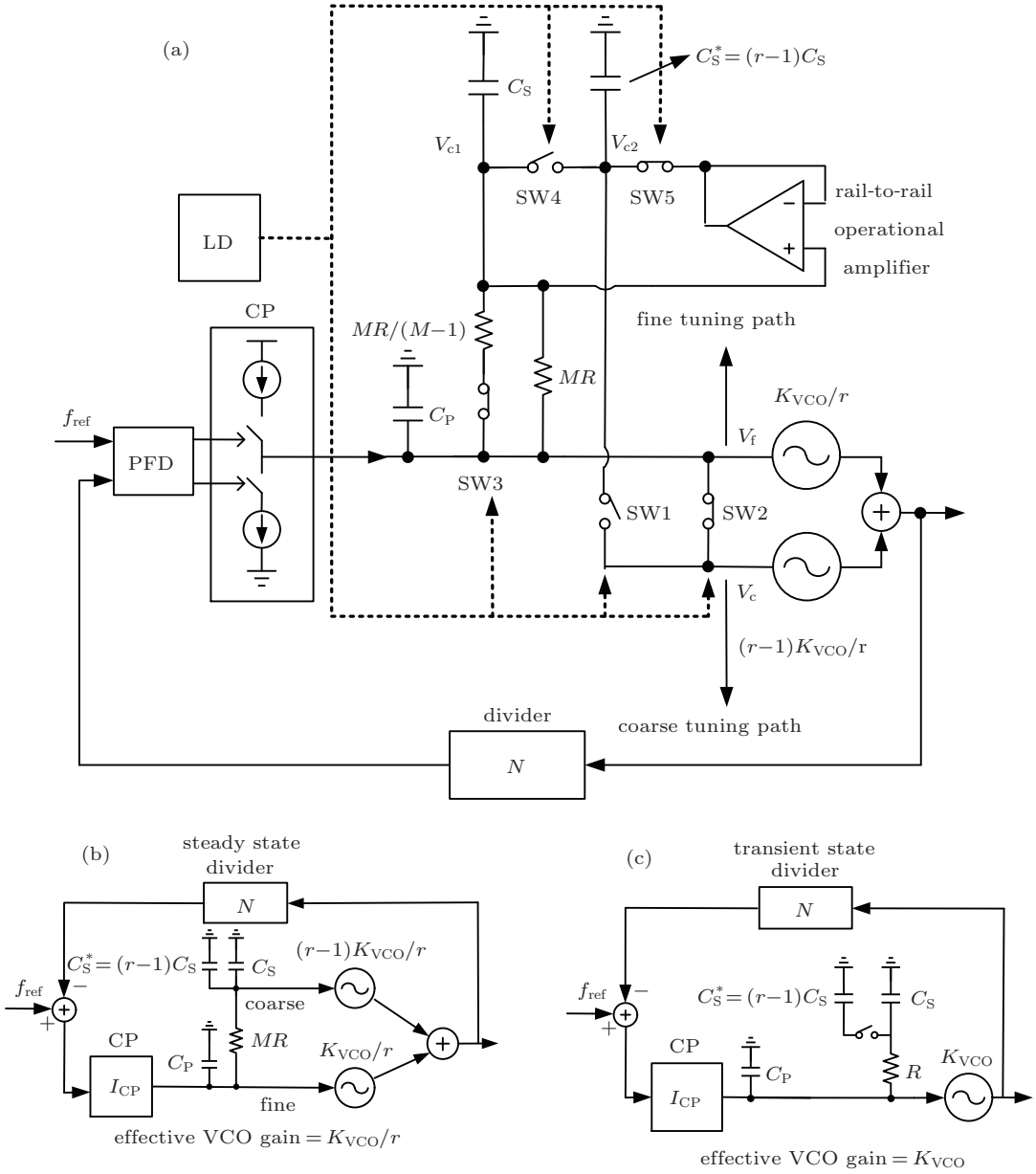


Fig. 1. (color online) (a) Schematic diagram of the hybrid PLL architecture. (b) Effective dual-path PLL in the steady state when the SW2, SW3, and SW5 are open, and the SW1 and SW4 are closed in (a). (c) Effective single-path PLL in the transient state when the SW1 and SW4 are open, and the SW2, SW3, and SW5 are closed in (a).

factor of M when we increase the resistor R of LF by M times and keep the CP current constant. It is crucial to keep a consistent phase margin for both the steady state and the transient state. The max phase margins of the single-path PLL $\phi_{\max_SP}$ and the dual-path PLL $\phi_{\max_DP}$ can be expressed as[15]

$$\phi_{\max_SP} = 2\tan^{-1}\sqrt{\frac{C_S}{C_P}} - 90^\circ, \quad (1)$$

$$\phi_{\max_DP} = 2\tan^{-1}\sqrt{\frac{C_S + C_S^*}{rC_P}} - 90^\circ, \quad (2)$$

where C_S and C_P are the series capacitor and parallel capacitor of the LF in the transient state, and $C_S + C_S^*$ is the series capacitor of the LF in the steady state. From Eqs. (1) and (2), we know that the phase margin can be kept constant while changing the series capacitor C_S of the LF to $C_S + C_S^*$ if C_S^* is equal to $(r-1)C_S$, as shown in Fig. 1.

Figure 1(c) shows the transient state when the LD provides a signal of logic 1, that is, SW1 and SW4 are open and SW2, SW3, and SW5 are closed, in which case the PLL becomes a single-path PLL. In the transient state, the fine and coarse tuning paths in Fig. 1(b) are shortened to each other. Thus, a wide loop bandwidth is obtained due to the effective high VCO gain (K_{VCO}). Note that the output frequency and switching time of the hybrid PLL can be strongly affected by the voltage difference between the series capacitor C_S^* and the series capacitor C_S. To solve this problem, a rail-to-rail operation amplifier is used for amplifying the voltage V_{c1} of the capacitor C_S to the voltage V_{c2} of the capacitor C_S^*, as shown in Fig. 1(a). This amplifier operates only in the transient state, which makes the power consumption of the hybrid PLL very low.

Unlike the previous adaptive loop bandwidth PLL designs,[9–15] we use a hybrid PLL with a wide-band single-path PLL and a narrow-band dual-path PLL in the transient and steady states, respectively. Such a hybrid PLL has advantages of both the fast locking time of the single-path PLL and the low spur of the dual-path PLL, while eliminating their disadvantages. It can both reduce the settling time and suppress the reference spurs, by changing the loop bandwidth according to the gain of the VCO and the resistor of the LF.

Figure 2 shows the chip photo of the hybrid PLL, which is fabricated in a 0.18-μm CMOS process, with a total die size of 1.4×0.46 mm^2. The circuit of VCO used here is the same as that described in Ref. [15], which is integrated with a full on-chip voltage regulator and a bandgap reference circuit to get a better phase noise than an ordinary VCO.[16] The rail-to-rail operation amplifier is used to replicate the voltage V_{c1} of the capacitor C_S to the voltage V_{c2} of the capacitor C_S^* with the structure in Ref. [17].

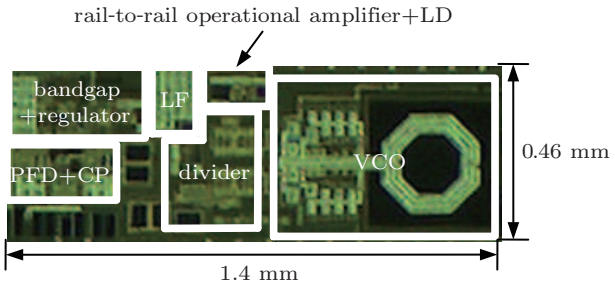


Fig. 2. (color online) Chip photo of the hybrid PLL.

3. Simulation and experimental results

The proposed PLL is designed by circuit simulation (Cadence Virtuoso Spectre), implemented in a 0.18-μm CMOS process, and measured by the MXA Signal Analyzer N9020A, MXG Vector Signal Generator N5182B, and Agilent Mixer Signal Oscilloscope MSO-X 2012A. Figure 3 shows the simulated locking process of the hybrid PLL. The black-dashed curve represents the output of LD. When the output of LD provides a signal of logic 0 or 1, the hybrid PLL is in a steady state or a transient state. The blue solid line shows the control voltage V_c of the coarse-tuning path. In the transient state, the coarse-tuning path V_c and fine-tuning path V_f are both shortened, which leads to a fast locking time. The V_{c1} of the capacitor C_S and the V_{c2} of the capacitor C_S^* are exactly the same, which is consistent with our prediction based on the application of the rail-to-rail operational amplifier, as shown in Fig. 3.

For comparison, we show the simulated results of the locking process of the hybrid PLL and the dual-path PLL in Fig. 4. When SW2, SW3, and SW5 are open and SW1 and SW4 are closed, the proposed PLL becomes a dual-path PLL. It is seen that the proposed hybrid PLL has shorter locked time as compared to the dual-path PLL. In particular, the proposed hybrid PLL has a settling time of 20 μs, while the settling time of the dull-path PLL is around 100 μs.

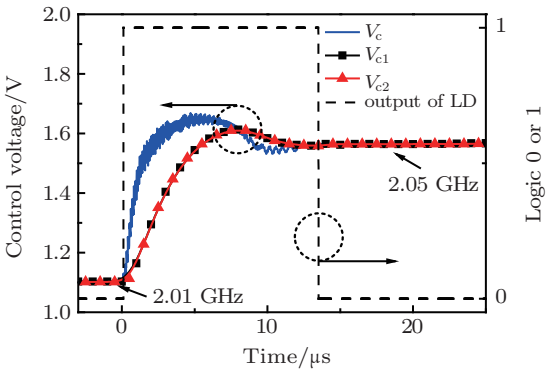


Fig. 3. (color online) Simulated locking process of the proposed hybrid PLL.

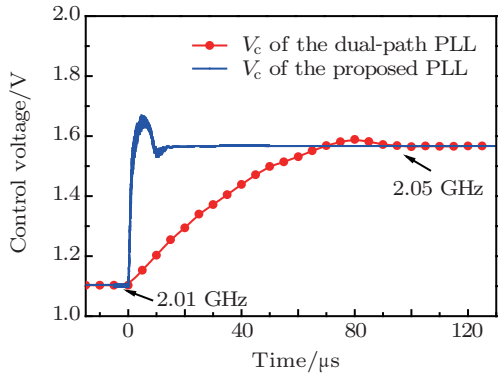


Fig. 4. (color online) Simulated locking times for the dual-path PLL and the proposed hybrid PLL.

A reference frequency of 10 MHz and a tuning range from 1.957 GHz to 2.089 GHz of the VCO are used in the measurements. The total power consumption of the hybrid PLL is less than 27 mW from a 1.8-V supply. The measured locking times for the dual-path PLL and the proposed hybrid PLL are shown in Fig. 5. At a given frequency jump at 40 MHz during the test, the settling times for the dual-path PLL and the hybrid PLL are 100 μs and 20 μs, respectively, which agrees well with the simulation results.

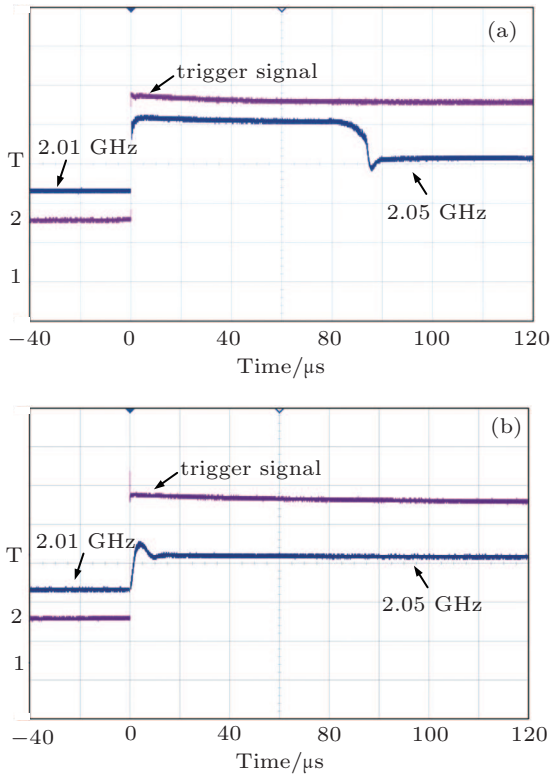


Fig. 5. (color online) Measured locking times for (a) the dual-path PLL and (b) the hybrid PLL.

To evaluate the performance of the VCO, the VCO free running power spectrum and the tuning curves in the transient and the steady states are measured and shown in Figs. 6(a) and 6(b). The output power of the VCO is 0.81 dBm at 2.01 GHz, as indicated in Fig. 6(a). In our measurement, the control voltage ($V_c = V_f$) of the VCO is tuned from 0 to 1.8 V in the transient state, while $V_c = 0.9$ V and V_f is tuned from 0 to 1.8 V in the steady state. The tuning range of the VCO is from 1.957 GHz to 2.089 GHz in the transient state, while it is from 2.002 GHz to 2.021 GHz in the steady state, as shown in Fig. 6(b). In the transient state, the VCO gain is about 87 MHz/V and the loop bandwidth is 200 KHz. However, the VCO gain and loop bandwidth are replaced by 11 MHz/V and 70 KHz, respectively, in the steady state.

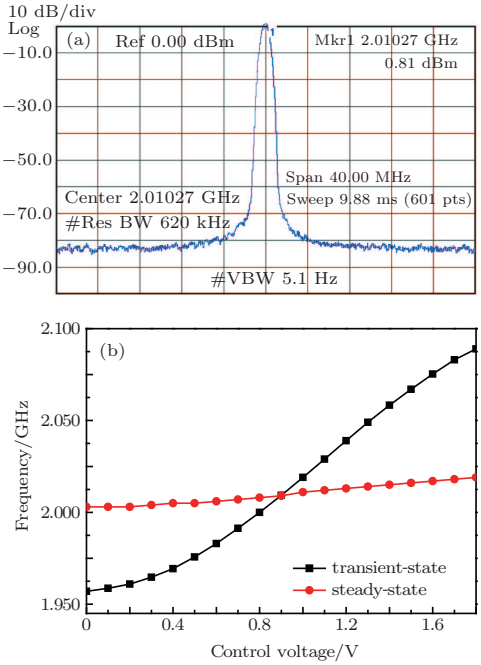


Fig. 6. (color online) (a) Measured VCO free running power spectrum; (b) measured VCO tuning curves in the transient and steady states.

Figure 7 shows the measured reference spurs for the single-path PLL and the hybrid PLL. When SW1 and SW4 are open and SW2, SW3, and SW5 are closed, the proposed PLL becomes a single-path PLL. The measured reference spur for the single-path PLL is about −60 dB as shown in Fig. 7(a), while it is below −73 dB for the hybrid PLL shown in Fig. 7(b). There is significant reduction of the reference spur in the hybrid PLL.

The measured phase noise performances of the VCO and the proposed hybrid PLL at 2.01 GHz are also shown in Fig. 8. It is seen that the VCO free running phase noise is −125.7 dBc/Hz at a 1 MHz offset. For 10 KHz and 1 MHz frequency offsets, the proposed PLL achieves −82.04 dBc/Hz and −121.06 dBc/Hz phase noises, respectively. These results are good enough for practical applications.

Finally, the performance comparison with some recent work is shown in Table 1. Compared with the single-path

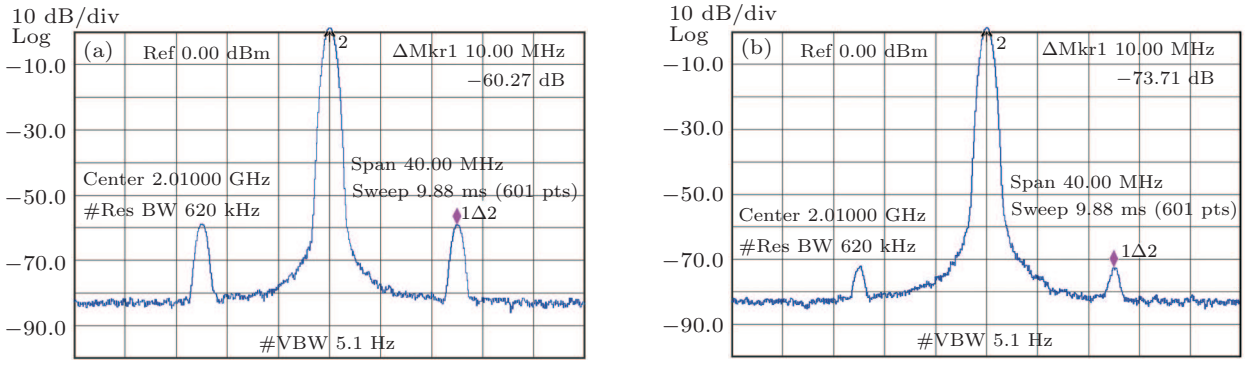


Fig. 7. (color online) Measured reference spurs for (a) the single-path PLL and (b) the proposed hybrid PLL.

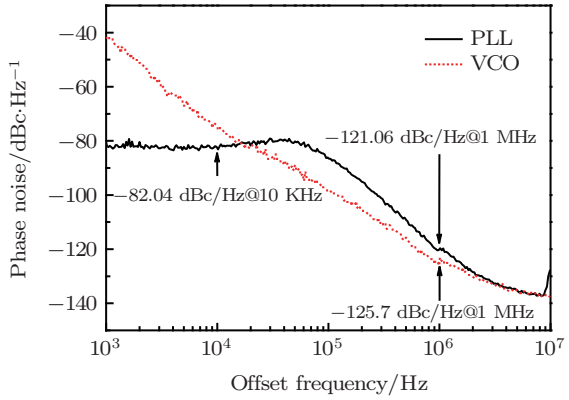


Fig. 8. (color online) Measured phase noise of the VCO and the proposed hybrid PLL at 2.01 GHz.

PLLs in Refs. [2] and [3], the proposed hybrid PLL achieves lower reference spur level. The sub-sampling technology is employed in Ref. [5] to achieve low spur, which may affect the stability of the PLL due to the variable loop gain. The proposed hybrid PLL can possess a faster locking settling time than the dual-path PLL in Ref. [6]. Although the adaptive loop bandwidth control method in single-path PLLs[12,13] or dual-path PLLs[14,15] can improve the performance to some extent, the high reference spurs in single PLLs and the slow locking settling time in dual-path PLLs cannot be completely overcome. The proposed hybrid PLL combines the advantages of both the single-path PLL and the dual-path PLL, which results in a faster locking time and a lower spur than the adaptive loop bandwidth single-path PLLs or dual-path PLLs.

Table 1. Performance comparison with some recent work.

Ref.	Ref. spur /dBc	Settling time/μs	F_{ref} /MHz	BW /KHz	Loop filter	Phase noise /dBc·Hz^{-1}	Process	Freq /GHz	Supply /V	Power /mW	Area /mm^2
[2]	∼ −46	*N*/*A*	38	*N*/*A*	3nd	–114.1@1MHz	0.18-μm CMOS	5	1.8	56	1.06
[3]	∼ −46	< 10	10	200	3nd	–110.2@1 MHz	0.18-μm CMOS	5	1.8	32	0.53
[5]	< −76	*N*/*A*	55.25	2700	3nd	–121@200 KHz	0.18-μm CMOS	2	1.8	3.8	0.2
[6]	*N*/*A*	800	19.8	1	2nd	–76@10 KHz –112@1 MHz	0.35-μm CMOS	2	3	60	5
[12]	–74	*N*/*A*	25	40	2nd	–102@40 KHz –114@1 MHz	90-nm CMOS	2	1.2	12	0.49
[13]	*N*/*A*	35	1	50	3nd	119.3@1 MHz	0.18-μm CMOS	2	1.8	17.3	0.588
[14]	–68	67	13	60	2nd	114.5@1 MHz	90-nm CMOS	4	1.2	25	1.37
[15]	–74	76	20	60	2nd	–79@10 KHz –113@1 MHz	0.18-μm CMOS	5	1.8	36	0.8
This work	–73.7	20	10	70	2nd	–82@10 KHz –121@1 MHz	0.18-μm CMOS	2	1.8	27	0.64

4. Conclusion

In this paper, we have proposed and demonstrated a novel hybrid PLL architecture to overcome the trade-off between the low spur signal and the fast locking time. By using a wide-band single-path PLL and a narrow-band dual-path PLL in the transient and steady state respectively, the hybrid PLL is simulated, implemented, and measured at 2 GHz. The measured results show that the hybrid PLL exhibits a lower reference spur than that in the single-path PLL by 13 dB, and the switching time can be reduced by about 80% as compared to the dual-path PLL. In addition, the proposed CMOS hybrid PLL offers advantages, such as small size, low-power consumption, low cost, and ease of mass production, which are of interest for application in wireless communications and power generation systems.

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