High dV/dt immunity MOS controlled thyristor using a double variable lateral doping technique for capacitor discharge applications*

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An analysis model of the dV/dt capability for a metal–oxide–semiconductor (MOS) controlled thyristor (MCT) is developed. It is shown that, in addition to the P-well resistance reported previously, the existence of the OFF-FET channel resistance in the MCT may degrade the dV/dt capability. Lower P-well and N-well dosages in the MCT are useful in getting a lower threshold voltage of OFF-FET and then a higher dV/dt immunity. However, both dosages are restricted by the requirements for the blocking property and the forward conduction capability. Thus, a double variable lateral doping (DVLD) technique is proposed to realize a high dV/dt immunity without any sacrifice in other properties. The accuracy of the developed model is verified by comparing the obtained results with those from simulations. In addition, this DVLD MCT features mask-saving compared with the conventional MCT fabrication process. The excellent device performance, coupled with the simple fabrication, makes the proposed DVLP MCT a promising candidate for capacitor discharge applications.

Keywords: MOS controlled thyristor, capacitor discharge

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1. Introduction

Pulsed power systems, featured high instantaneous power during short periods of time, mostly use capacitive energy storage (CES) as the power supply because of its stable energy storage, high power density, and transferring speed.[1–5] Since the pulse width is determined by the time constant of the circuit, the CES requires the load impedance to be low enough to generate a short pulse with a large current, thus realizing a high current rising rate di/dt.[6,7] Traditionally, it employs spark gaps as the switching units, which have the drawbacks of low repetition rate, short life time, and inefficiency.[8,9] Thanks to the development of power semiconductor devices, they have drawn special attention in pulse power applications due to their superior properties of compactness, light weight, low cost, and high efficiency.[9,10] Among the high-voltage power semiconductor devices, the metal–oxide–semiconductor (MOS) controlled thyristor (MCT) exhibits a strong conductivity modulation, and thus the low on-resistance makes it a proper candidate for capacitor discharge applications.

However, when switching from discharging to recharging, particularly under a fast operation for repetitive pulses, the MCT is often subjected to a high rate of rise of forward blocking voltage (dV/dt) during the operation.[11] This produces a capacitive displacement current, which can cause undesirable turn-on at voltages below the rated blocking voltage. Conventionally, the MCT is fabricated through a triple-well diffusion process in the DMOS technology.[12] The upper N/P-type wells are formed by implantation and diffusion, while the doping concentrations are restricted by the forward conduction and the blocking voltage. It lacks a specific doping profile optimization for the dV/dt immunity.

In this paper, an analysis model of dV/dt capability is developed. Based on this model, the existence of the OFF-FET channel resistance in the MCT may cause dV/dt triggering. So a double variable lateral doping (DVLD) technique is proposed to realize high dV/dt immunity without any sacrifice in the forward conduction and the blocking capability. In addition, this DVLD technique features mask saving compared with the conventional MCT fabrication process.

2. The dV/dt analysis model

The dV/dt effect in the MCT, as shown in Fig. 1, is due to the rapidly varying anode–cathode voltage, which gives rise to a displacement current across the capacitance of the P-well/N-drift junction. This displacement current flows through the P-well region and OFF-FET to the P^+ contact, thus giving a voltage drop (V_Z at red point Z) across the emitter junction of the parasitic NPN. If the forward bias, V_Z exceeds the built-in potential of the PN junction (V_{bi}), the NPN transistor is turned on, which will lead to a false turn-on of the MCT. An effective method to improve the MCT dV/dt rating is to get the P well shorted with the cathode via the inversion layer of OFF-FET.

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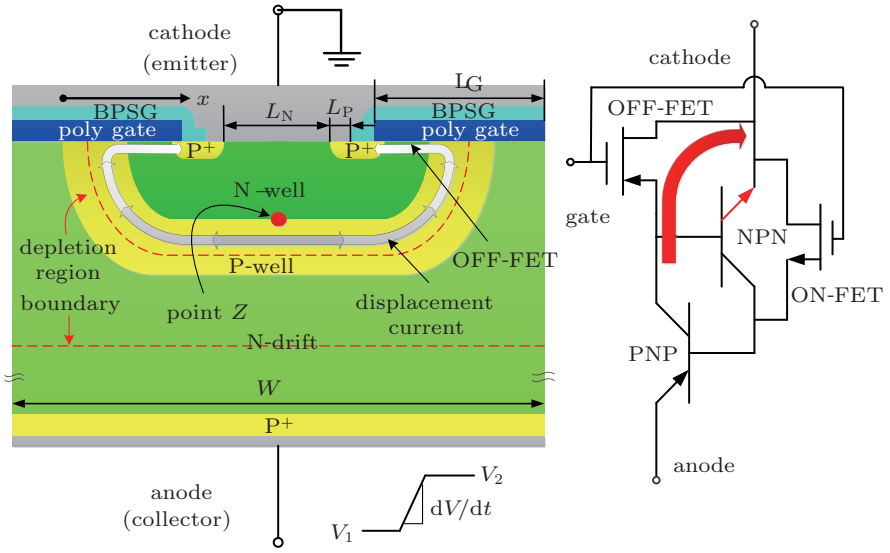


Fig. 1. (color online) (a) A diagram of $\mathrm{d}V/\mathrm{d}t$ triggering in MCT, and (b) equivalent circuit of the MCT.

Obviously, the $\mathrm{d}V/\mathrm{d}t$ immunity is influenced in principle by the intensity of the inversion layer of the OFF-FET channel. The $\mathrm{d}V/\mathrm{d}t$ capability can be analyzed in capacitor discharge by the following analysis.

The V_Z is the voltage drop of the displacement current along the total specific resistance R_{total} of the P well and the OFF-FET channel and is given by

$$V_Z = J_C R_{\mathrm{total}}. \tag{1}$$

The displacement current density J_C is amplified by a factor of $(1-\alpha_{\mathrm{PNP}})^{-1}$as the base current for the parasitic PNP transistor and is given by

$$J_C = \frac{C_D}{(1-\alpha_{\mathrm{PNP}})}\frac{\mathrm{d}V}{\mathrm{d}t}, \tag{2}$$

where C_D is the depletion capacitance of the P-well/N-well junction. The total specific resistance consists of the P-well resistance and the OFF-FET channel resistance, and is given by

$$R_{\mathrm{total}} = \int \rho x \mathrm{d}x = \int_0^{L_{\mathrm{P-well}}} \rho x \mathrm{d}x + R_{\mathrm{ch}}, \tag{3}$$

where $L_{\mathrm{P-well}}$, ρ, and R_{ch} are the half P-well length, the square resistance of the P well, and the specific resistance of the OFF-FET channel, respectively. Thus, V_Z is expressed as

$$\begin{aligned} V_Z &= \int_0^{L_{\mathrm{P-well}}} J_C \rho x \mathrm{d}x + J_C R_{\mathrm{ch}} \\ &= \frac{C_D \rho L_{\mathrm{P-well}}^2}{2(1-\alpha_{\mathrm{PNP}})}\frac{\mathrm{d}V}{\mathrm{d}t} + \frac{C_D R_{\mathrm{ch}}}{1-\alpha_{\mathrm{PNP}}}\frac{\mathrm{d}V}{\mathrm{d}t}, \end{aligned} \tag{4}$$

$$R_{\mathrm{ch}} = \frac{L t_{\mathrm{ox}}}{Z\mu_p \varepsilon_{\mathrm{ox}} |V_G - V_{\mathrm{TH}}|}, \tag{5}$$

where Z, L, μ_p, t_{ox}, $\varepsilon_{\mathrm{ox}}$ are the OFF-FET channel width, the OFF-FET channel length, the hole mobility in the inversion layer, the gate oxide thickness, and the dielectric constant, respectively. From Eq. (5), it can be seen that the difference between the gate bias (V_G) and the threshold voltage of OFF-FET (V_{TH}) strongly determines R_{ch}. On the other hand, V_{TH} is influenced by the N-well concentration N_D at the OFF-FET region, which is realized by the compensation between P-well and N-well dosages. Their relationship is given by

$$V_{\mathrm{TH}} = \psi_{\mathrm{MS}} - \frac{t_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}} Q_{\mathrm{ox}} - 2\frac{t_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}}\left(-q\varepsilon_s N_D \psi_{\mathrm{Fn}}\right)^{\frac{1}{2}} + 2\psi_{\mathrm{Fn}}, \tag{6}$$

where ψ_{MS} is the difference of the work function between the gate material and silicon, ψ_{Fn} is the flat band voltage of the n-type silicon, Q_{ox} is the fixed charge in the gate oxide layer, and ε_s is the dielectric constant of silicon. The $\mathrm{d}V/\mathrm{d}t$ triggering occurs when V_Z exceeds V_{bi}. Thus, the $\mathrm{d}V/\mathrm{d}t$ capability is given as

$$\frac{\mathrm{d}V}{\mathrm{d}t} = \frac{2V_{\mathrm{bi}}}{\rho L_{\mathrm{P-well}}^2 + 2R_{\mathrm{ch}}}\sqrt{\frac{2V_A}{qN_D\varepsilon_s}}\left(1-\alpha_{\mathrm{PNP}}\right), \tag{7}$$

where V_A is the applied anode voltage. From Eq. (7), $\rho L_{\mathrm{P-well}}^2$ and R_{ch} are two key physical device parameters that affect $\mathrm{d}V/\mathrm{d}t$. Obviously, $\rho L_{\mathrm{P-well}}^2$ relies on the P-well impurity dosage Q_P and the profile; R_{ch} is mainly determined by the N-well impurity dosage Q_N and V_G. The typical P-well and N-well concentrations are 5×10^{16} cm^{-3} and 2×10^{18} cm^{-3}, respectively, leading to $\rho L_{\mathrm{P-well}}^2 = 7.7$ μΩ·cm^2 and $R_{\mathrm{ch}}=\frac{63.3\ \mu\Omega\cdot\mathrm{V}\cdot\mathrm{cm}^2}{|V_G-V_{\mathrm{TH}}|}$. The term R_{ch} varies as $|V_G - V_{\mathrm{TH}}|$ changes. If the relationship $2R_{\mathrm{ch}} \ll \rho L_{\mathrm{P-well}}^2$ is satisfied, then the term of R_{ch} can be omitted. The $\mathrm{d}V/\mathrm{d}t$ capability will rely on the P-well width and the doping profile, which is represented as $\rho L_{\mathrm{P-well}}^2$. This situation has been discussed clearly before[11] and will not be discussed here. In this paper, we

concentrate on the situation of $\rho L_{\mathrm{P-well}}^2 \ll 2R_{\mathrm{ch}}$, which is usually caused by undesirable high $|V_{\mathrm{TH}}|$. Substituting Eqs. (5) and (6) into Eq. (7) provides a simplified expression

$$\left|\frac{\mathrm{d}V}{\mathrm{d}t}\right| = K_{\mathrm{G}} \frac{\varepsilon_{\mathrm{ox}} Z \mu_{\mathrm{ni}} V_{\mathrm{bi}} \left(A - B N_{\mathrm{D}}^{\frac{1}{2}}\right)}{t_{\mathrm{ox}} L_{\mathrm{ch}}} \sqrt{\frac{2V_{\mathrm{A}}}{qN_{\mathrm{D}}\varepsilon}} (1 - \alpha_{\mathrm{PNP}}), \quad (8)$$

where

$$A = \psi_{\mathrm{MS}} - \frac{t_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}} Q_{\mathrm{ox}} + 2\psi_{\mathrm{Fn}}, \quad (9)$$

$$B = \frac{2t_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}} \left(-q\varepsilon_{\mathrm{s}}\psi_{\mathrm{Fn}}\right)^{\frac{1}{2}}. \quad (10)$$

In the above expression, a coefficient K_{G} has been introduced to account for the influence of the N-well impurity dosage Q_{N} on ψ_{Fn} and α_{PNP}. A typical value for this coefficient is 1.3 in simulation.

Normally, higher $\mathrm{d}V/\mathrm{d}t$ immunity can be achieved by simply lowering Q_{N} to obtain a lower $|V_{\mathrm{TH}}|$ at OFF-FET. However, it is essential to have a high concentration gradient at the N-well/P-well junctions for a high injection rate and $\mathrm{d}i/\mathrm{d}t$ capability. This means a high $Q_{\mathrm{N}}/Q_{\mathrm{P}}$ rate.[13] Considering the blocking property, Q_{P} is high and then Q_{N} is even higher. Simply lowering Q_{N} definitely brings about a great sacrifice in the forward conduction property such as $\mathrm{d}i/\mathrm{d}t$ capability. Therefore, we introduce the DVLD technique. Using DVLD to form the P well and the N well can realize a high concentration gradient at the main current path and a low N_{D} at the channel region, thus realizing high $\mathrm{d}V/\mathrm{d}t$ immunity without compromising other properties.

3. Double variable lateral doping technique

MCTs are usually fabricated by triple diffusions in the DMOS process, as shown in Fig. 2(a). It is evident that the dosage requirement for forward conduction and blocking property conflicts with that for the OFF-FET threshold voltage and the $\mathrm{d}V/\mathrm{d}t$ capability. It is essential to realize a high concentration gradient at the desired position of the main current path and a low concentration at the channel region. Therefore, we introduce the variable lateral doping (VLD) technique, which is often used to improve the breakdown voltage in power semiconductor devices,[14,15] to form both the N well and the P well. A summary of the process flow outlining the original and the new steps is shown in Fig. 2(b). The DVLD is featured in the VLD formation for both N well and P well as shown in Fig. 2(c). Masks above the OFF-FET channel region shield approximately 45% and a field-limit-ring (FLR) mask is utilized to form the VLD P well and the junction terminal region at one time. The compensation between the DVLD layers at the OFF-FET channel can make N_{D} properly adjusted. The P-well width is proportionally enlarged to maintain a sufficient dosage in the P well for blocking. Thus, the DVLD technique can realize a desired doping profile for the enhancement in the $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}V/\mathrm{d}t$ capability simultaneously. It is economically better because of the less high temperature process and one mask being saved.

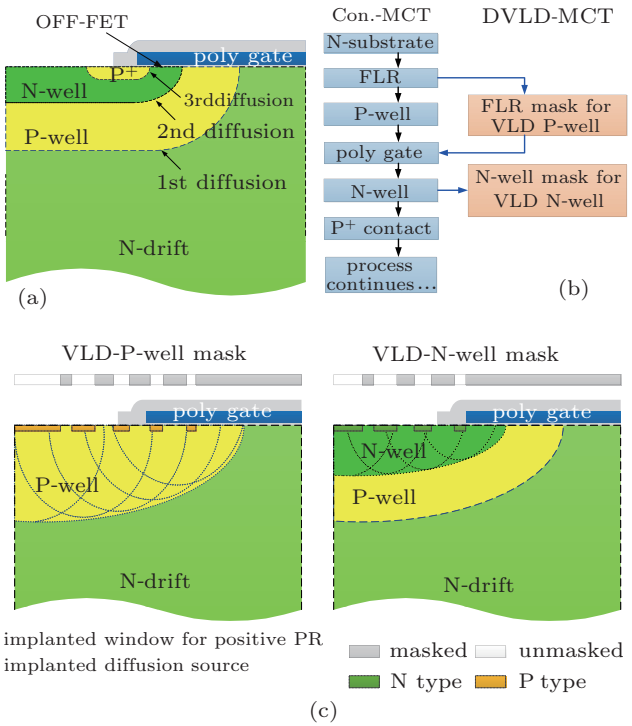


Fig. 2. (color online) (a) Conventional MCT with triple diffusions; (b) summary of process flow; (c) DVLD implantation pattern.

Table 1. Device parameters.

Parameter	Symbol	Value
Cell pitch/μm	W	30
MOS gate length/μm	L_{G}	7.5
N^+-cathode length/μm	L_{N}	4.5
P^+-cathode shorts length/μm	L_{P}	1
P-well impurity dose/cm^{-2}	Q_{P}	4×10^{13}
N-well impurity dose/cm^{-2}	Q_{N}	1.8×10^{14}
		1.9×10^{14}
		2×10^{14}
		2.1×10^{14}
		2.2×10^{14}
N-drift doping/cm^{-3}	N_{D}	5×10^{13}
N^+-cathode junction depth	/	0.5
N^+-cathode peakdoping/cm^{-3}	/	1×10^{19}
P^+-anode doping/cm^{-3}	/	1×10^{19}
P^+-anode depth/μm	/	4
P^+-cathode shorts junction depth/μm	/	0.5
P^+-cathode shorts doping/cm^{-3}	/	1×10^{19}
Carriers lifetime/μs	τ_{n}, τ_{p}	400/100

In order to verify the merits of the DVLD MCT, we study the DVLD MCT and the conventional MCT (Con. MCT) in Synopsys TCAD with the device parameters listed in Table 1. Figure 3 shows the MCT surface doping profiles. It can be seen that the DVLD MCT has an identical concentration in the

N well at the P–N–P–N portion while a lower one at the OFF-FET channel attributing to the VLD technique implemented in both P well and N well. Consequently, a lower concentration at the OFF-FET channel will contribute to a lower $|V_{TH}|$. Figure 4 shows the V_{TH} against N-well dosage N_D for both conventional MCT and DVLD MCT devices. Compared to the conventional triple diffusion process, the DVLD can realize 75% lower N_D and maintain a V_{TH} shift over 7 V. The analysis results obtained with Eq. (6) show good accordance with the simulation results.

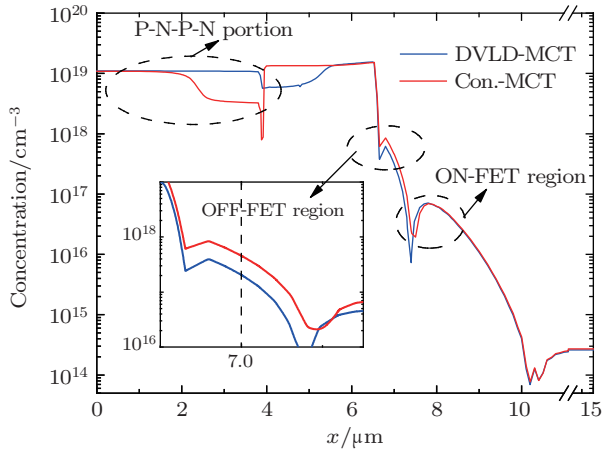


Fig. 3. (color online) Lateral concentration profile along the surface in MCTs with an N-well dosage of 2×10^{14} cm^{-2}. The insert shows the close view at the OFF-FET region.

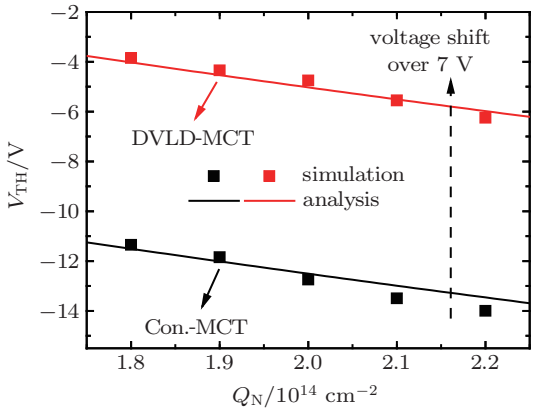


Fig. 4. (color online) The OFF-FET threshold voltage V_{TH} against N-well impurity dosage Q_N for DVLD MCT and conventional MCT.

The dV/dt capability is analyzed with the capacitive charging circuit shown in Fig. 5. Here V_{cc} produces 0–1000 V pulse waves with a maximum dV/dt of 1000 kV/μs. The waves are converted to exponentially rising and falling waveforms on capacitor C through the RC circuit. The voltage between the anode and the cathode of the MCT is supplied by the capacitor with a series resistor R_L to limit the maximum current. The dV/dt is varied by changing R, and the dV/dt capability is the maximum value at which the device still maintains its blocking state.

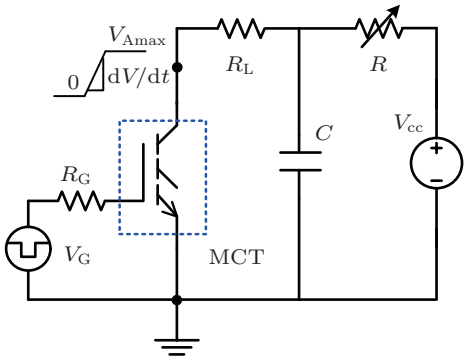


Fig. 5. (color online) The dV/dt immunity analysis circuit. The supply voltage V_{cc} is 1000 V; the storage capacitor C and current-limiting resistor R_L are 5 μF and 1 Ω, respectively; the gate resistance R_G is 4.7 Ω.

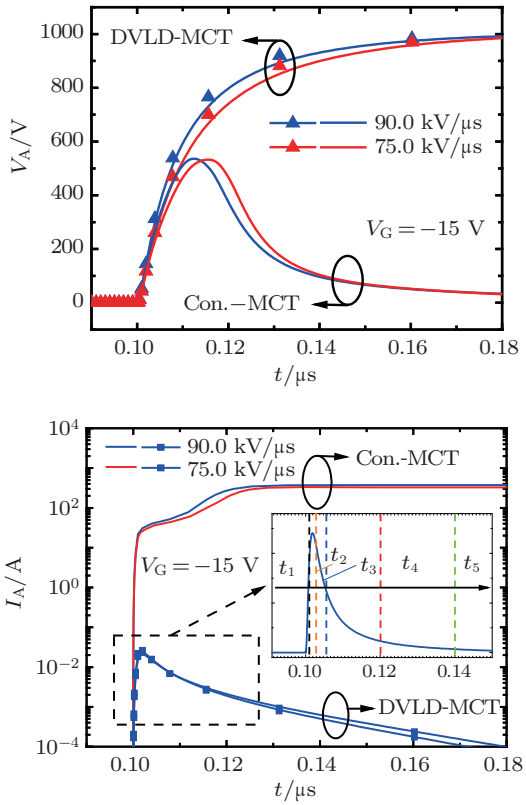


Fig. 6. (color online) The waveforms under dV/dt of 75 kV/μs and 90 kV/μs: (a) anode voltage versus time; (b) anode current versus time. The inserted graph in Fig. 6(b) shows the time definition for the following carrier distribution analysis, where $t_1 = 0.101$ μs; $t_2 = 0.103$ μs; $t_3 = 0.106$ μs; $t_4 = 0.12$ μs; $t_5 = 0.14$ μs.

The simulated results at $V_G = -15$ V are shown in Fig. 6. The voltage curves in Fig. 6(a) indicate that the DVLD MCT can reach a blocking voltage of 1000 V in around 0.06 μs at dV/dt of 90 kV/μs. On the contrary, it is found that the anode voltage of the Con. MCT quickly declines after having reached a specific peak value. It indicates that the Con. MCT is turned on and its dV/dt effect is triggered under this condition. A larger dV/dt causes breakdown in the Con. MCT at an earlier time. For current curves in Fig. 6(b), the Con. MCT eventually stays on and fixes at a high current of ∼ 300 A, while the DVLD MCT exhibits a peak current less

than 50 mA. The results confirm that the DVLD MCT can withstand a higher dV/dt.

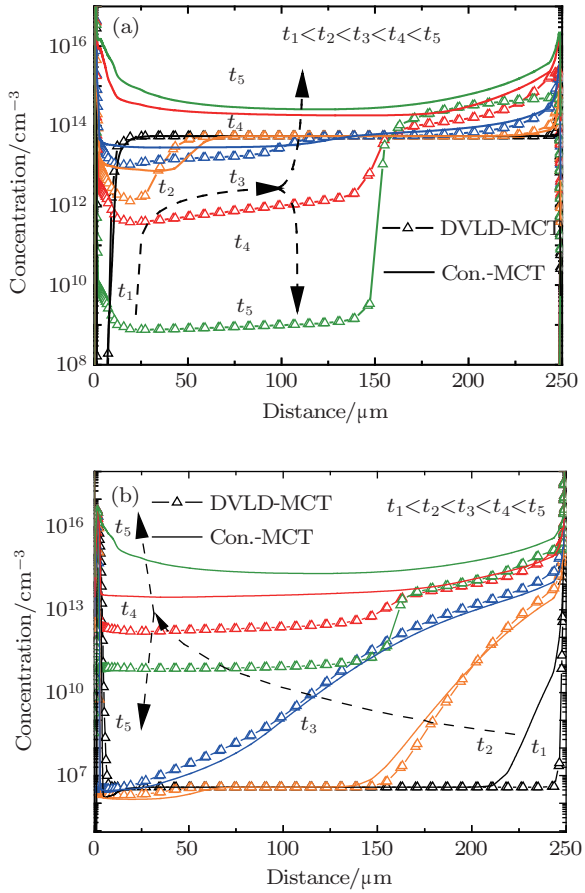


Fig. 7. (color online) (a) Electrons and (b) holes concentration profiles under dV/dt of 90 kV/μs.

Figure 7 shows the electron- and hole-carrier distributions under dV/dt of 90 kV/μs for both Con. MCT and DVLD MCT devices. It is noticed that the DVLD MCT maintains the blocking state under the condition of 90 kV/μs, while the Con. MCT dV/dt capability is about 20 kV/μs. As can be seen from Fig. 7, the electron-carrier concentration decreases from t_1 to t_3 for both devices, and the hole-carrier concentration is increased in this period. However, there are differences in the carrier distributions for DVLD MCT and Con. MCT from t_4 to t_5. The electron-carrier density of the DVLD MCT declines and the depletion layer expands further with the increase in time. It indicates that the device is entering the blocking state and the electrons are being depleted out in this period. As a result, the hole-carrier density of the DVLD MCT also declines from t_4 to t_5, as shown in Fig. 7(b). While, for the Con. MCT device, both the electron- and hole-carrier densities sharply increase from t_4 to t_5 and finally exceed the background doping (5×10^{13} cm^{-3}). It indicates that the Con. MCT is turned on and its dV/dt effect is triggered under this condition. Consequently, the DVLD MCT shows a faster establishment of the depletion region under the maximum dV/dt and a higher dV/dt immunity. This can be verified by the comparison of the dV/dt capability at different applied gate voltages V_G for both DVLD MCT and Con. MCT structures, as shown in Fig. 8. From this figure, it is evident that the proposed DVLD MCT suffers from dV/dt triggering when V_G is larger than -5 V, while the dV/dt triggering for the Con. MCT is larger than -13 V. It demonstrates that the dV/dt triggering voltage of the proposed DVLD MCT is improved by ~ 8 V compared with that of the Con. MCT. The analytical results are also shown in this figure. It is shown that the analysis results calculated by Eq. (8) are in good agreement with the simulation results.

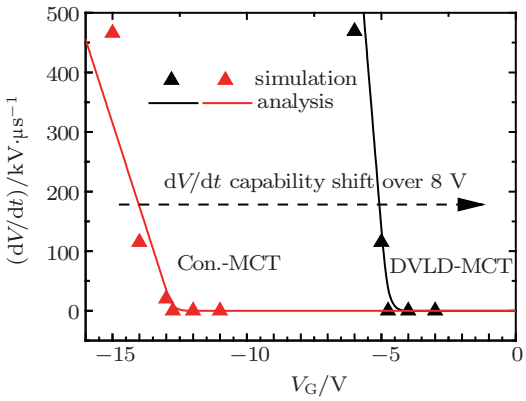


Fig. 8. (color online) The dV/dt versus applied gate voltage V_G.

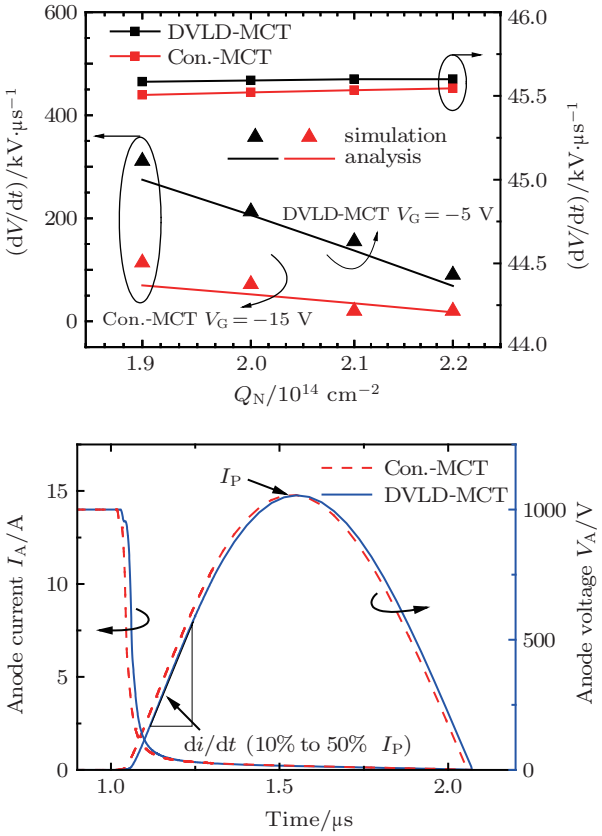


Fig. 9. (color online) (a) The dV/dt and di/dt versus the N-well dosage, (b) the simulated pulse discharge waveforms with $L = 20$ nH and $C = 5$ μF.

The dV/dt capability is also investigated by varying N-well dosage Q_N as shown in Fig. 9(a). It is noteworthy that in order to adequately reflect the effect of the N-well dosage on dV/dt, V_G of -5 V and -15 V are applied to the DVLD MCT and the Con. MCT, respectively. The dV/dt immunity increases with the declining N-well dosage for both devices, while the DVLD MCT shows a better improvement. In fact, according to Fig. 8, the dV/dt immunity of the DVLD MCT can be further improved by applying a smaller V_G. The analysis results correlate well with the simulation results. Meanwhile, the DVLD MCT shows the same di/dt capability as the Con. MCT around 45 kA/μs. Figure 9(b) shows the simulated pulse discharge waveforms for both devices with $L = 20$ nH and $C = 5$ μF, and the di/dt definition is given in this figure. Thus, it demonstrates that the proposed DVLD MCT features a higher dV/dt immunity without any sacrifice in the di/dt capability.

4. Conclusion

An analysis model for the MCT dV/dt capability is developed in this paper. It is shown that the existence of the OFF-FET channel resistance in the MCT may lead to the dV/dt effect triggering, which is determined by the threshold voltage of OFF-FET. However, the dosage requirements for the forward conduction capability and the blocking property conflict with the threshold voltage of OFF-FET and the dV/dt capability. Therefore, a double variable lateral doping technique is introduced to form the P well and N well with a high concentration gradient at the main current path and a low concentration at the channel region. It demonstrates that the OFF-FET threshold voltage of the proposed DVLD MCT shifts over 7 V compared with that of the conventional MCT, thus resulting in high dV/dt immunity without any sacrifice in other properties. The analysis results show excellent agreement with the simulation results. In addition, this DVLD technique features mask-saving compared with the conventional MCT fabrication process. The excellent device performance, coupled with the simple fabrication, makes the proposed DVLP MCT a promising candidate for capacitor discharge applications.

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