A low specific on-resistance SOI LDMOS with a novel junction field plate*

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A low specific on-resistance SOI LDMOS with a novel junction field plate (JFP) is proposed and investigated theoretically. The most significant feature of the JFP LDMOS is a PP–N junction field plate instead of a metal field plate. The unique structure not only yields charge compensation between the JFP and the drift region, but also modulates the surface electric field. In addition, a trench gate extends to the buried oxide layer (BOX) and thus widens the vertical conduction area. As a result, the breakdown voltage (BV) is improved and the specific on-resistance ($R_{on,sp}$) is decreased significantly. It is demonstrated that the BV of 306 V and the $R_{on,sp}$ of 7.43 mΩ·cm^2 are obtained for the JFP LDMOS. Compared with those of the conventional LDMOS with the same dimensional parameters, the BV is improved by 34.8%, and the $R_{on,sp}$ is decreased by 56.6% simultaneously. The proposed JFP LDMOS exhibits significant superiority in terms of the trade-off between BV and $R_{on,sp}$. The novel JFP technique offers an alternative technique to achieve high blocking voltage and large current capacity for power devices.

Keywords: LDMOS, RESURF, field plate, breakdown voltage, specific on-resistance

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1. Introduction

A lateral double-diffused metal-oxide-semiconductor field-effect transistor (LDMOSFET) is considered as a preferred power device in smart power integrated circuits (PICs) owing to ease of integration and drive. However, it will lead to an increase in power dissipation, since the specific on-resistance ($R_{on,sp}$) increases with breakdown voltage (BV) as $R_{on,sp} \propto BV^{2.5}$ in conventional power LDMOS.[1] The reduced surface field (RESURF), field plate (FP), and lateral varied doping (LVD) have been widely used to decrease $R_{on,sp}$ and improve BV.[1–6] The conventional metal field plate (MFP) technique has an advantage of its simple process, but the peak electric field occurs at the end of the MFP and limits the increase in BV.[6,7] The LVD is a good choice to achieve a high BV; however, a considerable resistance emerges in the lower doping region and leads to a "hotspot" when a high current flows.[8] In the previous work, lots of new device structures are equipped with trench gates to reduce $R_{on,sp}$ due to high current density and elimination of the junction field effect transistor (JFET) effect.[9,10] Furthermore, the trench gate has an extra merit of the isolation for silicon-on-insulator (SOI) LDMOS when the trench gate is extended to the buried oxide layer (BOX).[11]

In this paper, a new SOI LDMOS with a novel junction field plate (JFP) and an extended trench gate is presented, which not only breaks through the silicon limit, but also overcomes the drawbacks of the MFP mentioned above. The basic idea of the JFP technique is that a PP–N junction is utilized to form field plate. The proposed JFP LDMOS forms double-RESURF effect in the drift region, resulting in a higher n-drift doping and a uniform electric field because of the linear doping technology used in the thin JFP layer.[12,13] In addition, the trench gate is employed to widen the conduction area. Therefore, the BV is enhanced and the $R_{on,sp}$ is reduced significantly. The MEDICI simulation is used to study the mechanism of the JFP structure and design the device. It is shown that the JFP technique has a good function to the static performance of an LDMOS.

2. Device structure and mechanism

The schematic cross section of the proposed JFP LDMOS is shown in Fig. 1(a). The novel device is equipped with a JFP structure at the surface and has a trench gate extended to the BOX. Moreover, we utilize a linear doping in the p- region of the JFP, and the doping profile is shown in Fig. 1(b). Therein, N_d is the doping concentration of the n-drift region, N_p and G are the background doping concentration and the concentration gradient of the p- region of the JFP, respectively, and T_f is the thickness of the field oxide layer.

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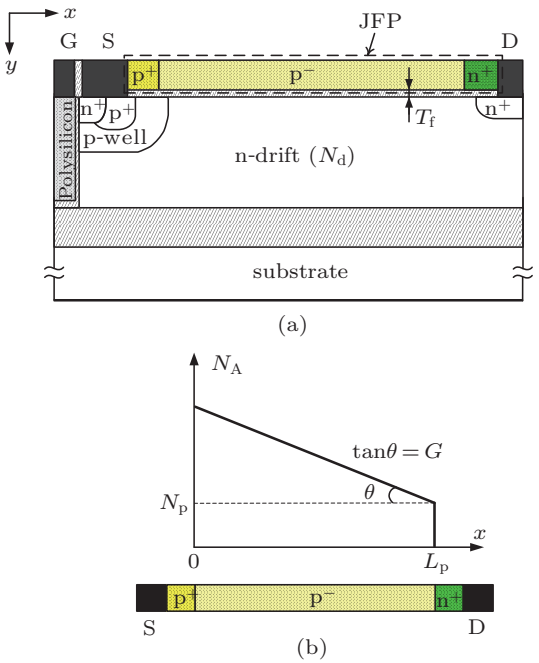


Fig. 1. (color online) (a) Schematic cross section of the JFP LDMOS; (b) linear doping profile in the p- region of the JFP.

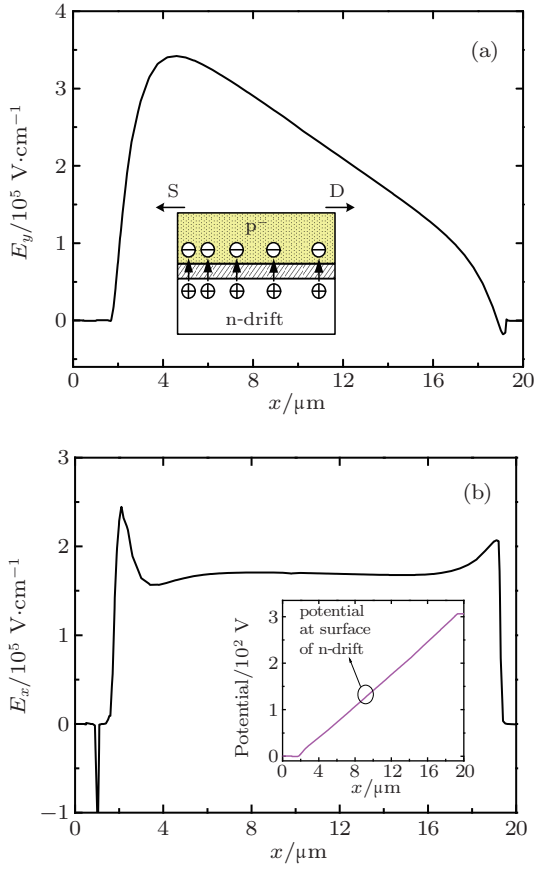


Fig. 2. (color online) Electric field distribution of (a) the y component (E_y) and (b) the x component (E_x) at the surface of the n-drift region. The positive directions of the electric fields are opposite to the directions of the coordinate axis shown in Fig. 1(a).

In the off state, the p- region of the JFP is depleted to achieve charge compensation with the n-drift region. The unique device thereby yields an effect in the drift region just like double RESURF, allowing a higher n-drift doping. Both the RESURF effect and the linear doping technique lead to a nearly linear potential distribution in the thin JFP film. As a result, the electric field of the x component (E_x) at the surface of the drift region is modulated to be uniform and an enhanced BV is acquired. This is just like the effect of resistive field plate. In brief, the JFP on an LDMOS causes charge compensation in the y direction and modulates the surface electric field of the n-drift region in the x direction, which not only reduces $R_{on,sp}$, but also improves BV. In Fig. 2(a), the effect of charge compensation in the y direction is verified by the large electric field of the y component (E_y). Meanwhile, the effect of charge compensation is increasingly strong from the drain to the source as a result of the linear doping in the JFP. Therefore, $R_{on,sp}$ is decreased. At the same time, figure 2(b) shows that the surface potential distribution of the n-drift region is nearly linear and the E_x is almost rectangular distribution.

Moreover, the JFP technique does not occupy the conduction area of the n-drift region, which is superior to the conventional double-RESURF structure. In addition, the long electron accumulation layer is formed near the extended gate in the n drift to further reduce $R_{on,sp}$.

3. Results and discussion

The device structures are designed by the MEDICI simulation. The deposited Si film on the field oxide is mostly polycrystalline, and it can be recrystallized to obtain microcrystalline by different annealing techniques to improve the carrier mobility and decrease diffusion coefficient.[14,15] Meanwhile, the JFP film is preferable not to be too thick (e.g., 0.6 μm in this paper), since the linear doping technology is suitable for a thin film. In our simulation, the following is the same device dimensional parameters for several structures: the thicknesses of SOI ($T_s = 2.5$ μm) and BOX ($T_{ox} = 2$ μm), the cell pitch of device ($W_d = 20$ μm), and the length of the drift region ($L_d = 17$ μm).

Figure 3 shows the current flowline contours for the JFP LDMOS, trench gate LDMOS with p-top layer (P-top LDMOS), trench gate LDMOS with metal field plate (MFP), and conventional (Con.) LDMOS with their own high figure of merits (FOM, $\mathrm{FOM} = \mathrm{BV}^2/R_{on,sp}$) at $V_{GS} = 15$ V and $V_{DS} = 0.5$ V. The charge compensation effect causes an increased n-drift doping and a reduced $R_{on,sp}$. Comparing Fig. 3(a) with Figs. 3(b)–3(d), $R_{on,sp}$ of the JFP LDMOS is the lowest, demonstrating the remarkable function of the JFP technique. The optimized N_d is as high as 1.4×10^{16} cm^{-3} and $R_{on,sp}$ is 7.43 mΩ·cm^2 for the JFP LDMOS. For the P-top LDMOS, although the double RESURF also increases the optimized N_d to 1.2×10^{16} cm^{-3} compared with Figs. 3(c) and 3(d), the P-top layer narrows the effective conduction area and introduces a depleted region in the n-drift compared with Fig. 3(a). Eventually, the $R_{on,sp}$ of 10.55 mΩ·cm^2 is obtained. For the Con. LDMOS, the $R_{on,sp}$ of 17.12 mΩ·cm^2 is the highest as a result of the lowest N_d of 5.0×10^{15} cm^{-3}.

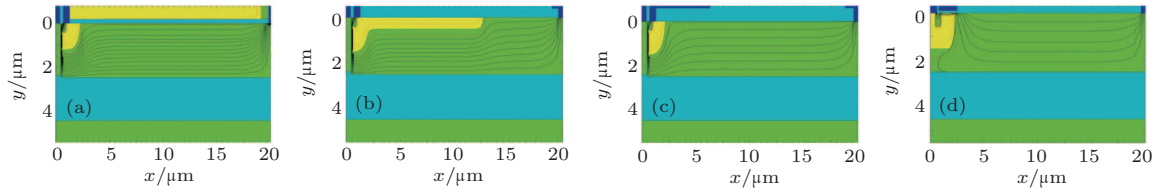


Fig. 3. (color online) Current flowline contours in the on state for (a) JFP (7.43 mΩ·cm^2), (b) P-top (10.55 mΩ·cm^2), (c) MFP (14.14 mΩ·cm^2), and (d) Con. (17.12 mΩ·cm^2) LDMOSFETs. (1×10^{-6} A·μm^{-1}/contour, $V_{GS} = 15$ V, with the optimal N_d).

Figure 4 shows the current density in the y direction for the four device structures in the middle of the cell (at $x = 10$ μm). Owing to the higher doping concentration than those of the MFP and Con. LDMOSFETs as well as the broader conduction area than that of the P-top LDMOS, the current density of the JFP LDMOS is the highest. The $R_{on,sp}$ of the JFP LDMOS is thus far lower than those of any other structures. The output characteristics of the four devices are studied and shown in Fig. 5. Owing to the contribution of the high n-drift doping, the JFP LDMOS exhibits the largest drain current.

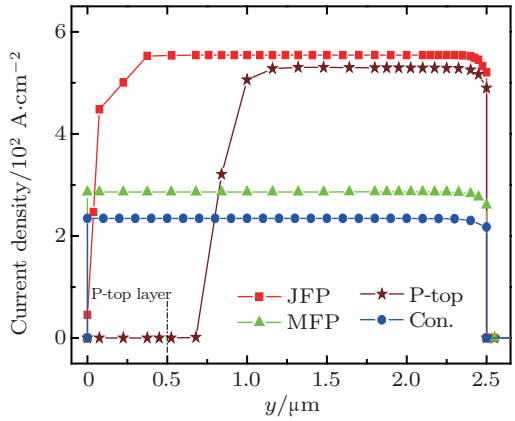


Fig. 4. (color online) Current density in the y direction at $x = 10$ μm ($V_{GS} = 15$ V).

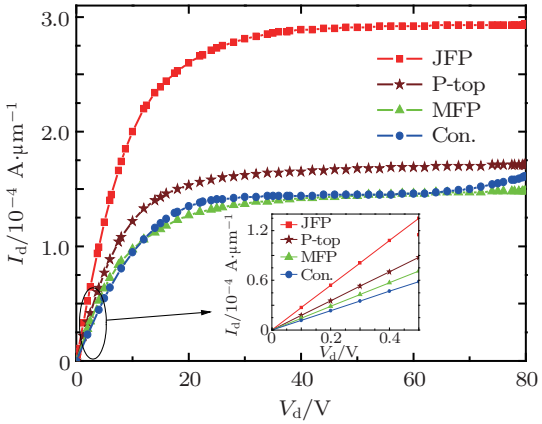


Fig. 5. (color online) Output I–V characteristics at $V_{GS} = 15$ V.

Figure 6 shows the equi-potential contours of the four devices at breakdown. Figure 6(a) shows that the equi-potential contours of the JFP LDMOS are dense and uniform, just as proved in Fig. 2(b). The BV of the JFP LDMOS is the highest and reaches 306 V. In comparison, the MFP LDMOS exhibits an inferior blocking characteristic. At the field plate end, intensive equi-potential contours appear in the dashed ellipse of Fig. 6(c), leading to electric field crowding and premature breakdown. For the Con. LDMOS, the electric field depression is present in the middle of the drift region, as shown in the dashed rectangle of Fig. 6(d), and the BV is thus the lowest.

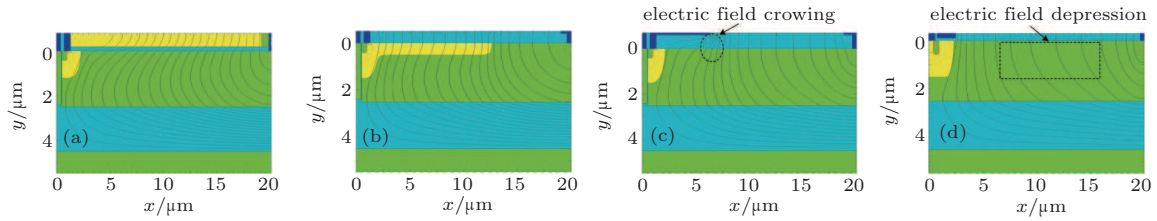


Fig. 6. (color online) Equi-potential contours at their breakdown for (a) JFP (306 V), (b) P-top (298 V), (c) MFP (267 V), and (d) Con. (227 V) LDMOSFETs (15 V/contour).

Figure 7 shows the dependences of the BV and $R_{on,sp}$ on N_d for the JFP, P-top, and MFP LDMOSFETs. The BV of the JFP LDMOS are a little higher than those of the P-top LDMOS. Furthermore, both the higher optimized N_d and the wider current path contribute to a much smaller $R_{on,sp}$ for the JFP LDMOS. For the MFP LDMOS, the single RESURF instead of the double RESURF is formed. As a result, the optimal N_d is almost half of those of the JFP and P-top LDMOSFETs. Owing to the contribution of the charge compensation by the JFP structure, the JFP LDMOS also exhibits an insensitivity of BV to N_d in comparison to the MFP LDMOS when $N_d \leq 1.4\times10^{16}$ cm^{-3}.

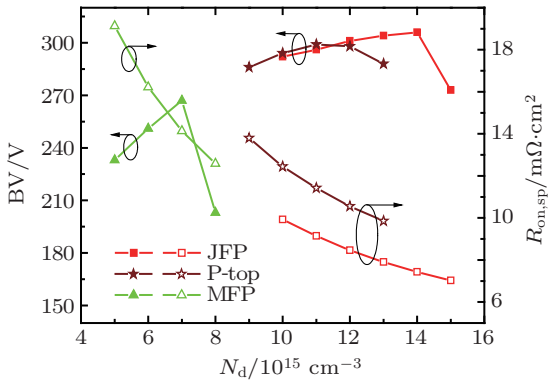


Fig. 7. (color online) Dependences of BV and $R_{on,sp}$ on N_d (the other parameters are optimized).

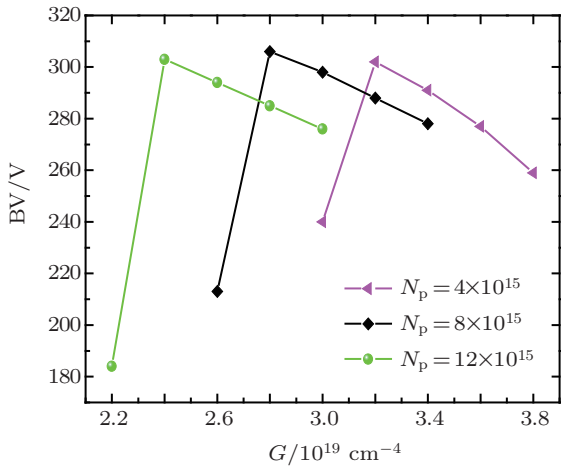


Fig. 8. (color online) Influence of the doping of the JFP structure on BV for the JFP LDMOS.

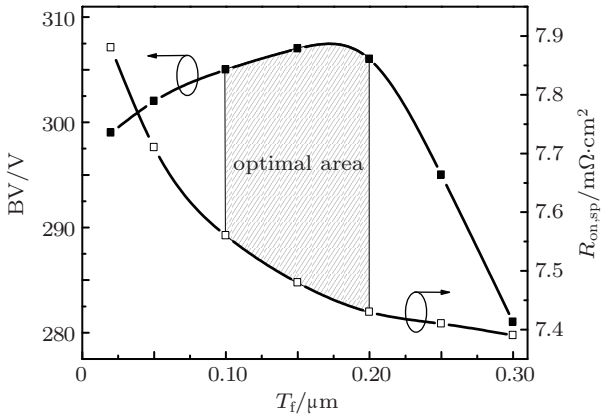


Fig. 9. (color online) Dependences of BV and $R_{on,sp}$ on the thickness of field oxide layer T_f.

Figure 8 shows the influence of the doping of the JFP on the BV. The doping of the JFP is measured by N_p and G. If N_p is too high, the device is prone to breakdown close to the drain of the JFP. If G is too high, the charge compensation effect at the drift surface near the source is harsh, where E_y is too large, and leads to premature breakdown. Moreover, it is advisable to adopt a little higher doping dose in the JFP structure, since the n-drift is difficult to be depleted and the BV decreases dramatically if the doping dose of the JFP structure is lower. Figure 9 shows the influence of T_f on BV and $R_{on,sp}$. When T_f is thick enough, the function of the JFP structure is degenerated. However, when T_f is too thin, the effect of charge compensation is enhanced and leads to an increased E_y at the surface of the n-drift, which results in premature breakdown. Moreover, $R_{on,sp}$ increases with the decrease in T_f because of the presence of a narrow depletion region at the surface of the drift caused by the JFP structure. Consequently, the optimal range of T_f is 0.15 μm $\leq T_f \leq$ 0.2 μm.

Table 1 lists the values of optimized N_d, BV, $R_{on,sp}$, and FOM for the JFP, P-top, MFP, and Con. LDMOSFETs, respectively. Owing to the contribution of the JFP technique, the JFP LDMOS possesses an excellent static characteristic. The FOM of JFP LDMOS is far higher than those of the other structures. Figure 10 shows the relationship between $R_{on,sp}$ and BV of the proposed JFP LDMOS and different state-of-the-art RESURF structures.[1] The proposed JFP SOI LDMOS reduces $R_{on,sp}$ by 80.4%, 66.4%, and 58.7% compared with the single-, double-, and triple-RESURF LDMOSFETs with planar gate in Ref. [1] at the same BV class. It is demonstrated that the JFP LDMOS exhibits significant superiority and breaks through the silicon limits for different RESURF LDMOS devices.

Table 1. Optimized parameters N_d, BV, $R_{on,sp}$, and FOM for the 4-type devices. $R_{on,sp}$ is the specific on-resistance at V_{GS}=15 V and a half-cell pitch of 20 μm.

LDMOS type	Optimized $N_d/10^{15}$cm^{-3}	$R_{on,sp}$ /mΩ·cm^2	BV/V	FOM /MW·cm^{-2}
JFP	14.0	7.43	306	12.60
P-top	12.0	10.55	298	8.42
MFP	7.0	14.14	267	5.04
Con.	5.0	17.12	227	3.01

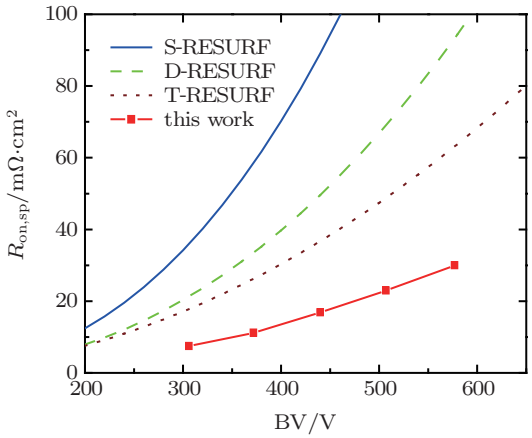


Fig. 10. (color online) $R_{on,sp}$ versus BV for the JFP LDMOS and different types of RESURF structures with planar gate.

Figure 11 shows the key fabrication steps for the JFP LDMOS: (a) to form the p well; (b) to form the JFP film with linear doping, including thermal oxidation to form the field

oxide layer, deposition the polysilicon film, recrystallization and implantation to form linear doping profile; (c) and (d) impurity implantation and annealing, including p+ contact, p+ anode region, n+ source, n+ drain, n+ cathode region; (e) to form the trench gate; and (f) to form the electrodes. The linear doping can be achieved with only one mask by controlling the size and space of the mask windows, which is utilized in the p- region of the JFP as shown in Fig. 1(b).[13,16]

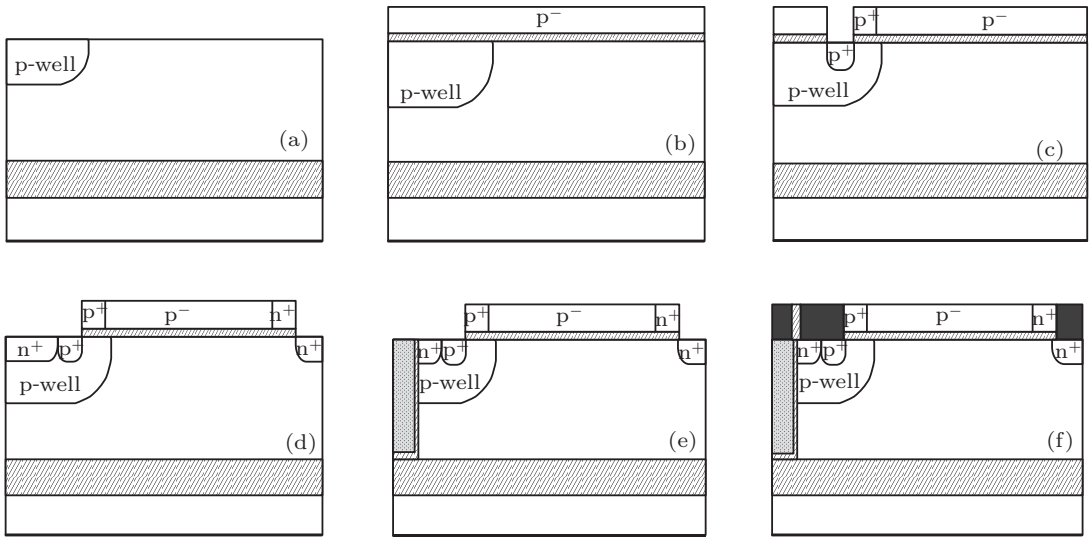


Fig. 11. Key process steps of the JFP LDMOS to: (a) form the p-well; (b) form JFP film with linear doping; (c), (d) impurity implantation and annealing; (e) form the trench gate; (f) form the electrodes.

4. Conclusion

The SOI LDMOS with a novel JFP technique is proposed and investigated by simulation. The JFP structure yields a charge compensation effect in the y direction and modulates the surface electric field of the n-drift region in the x direction, resulting in an enhanced n-drift doping and uniform surface electric field distribution. It is demonstrated by the MEDICI simulation that the BV of 306 V and the $R_{on,sp}$ of 7.43 mΩ·cm^2 are obtained for the proposed JFP LDMOS at 20-μm half-cell pitch. Compared with the conventional LDMOS, the BV is improved by 34.8% and the $R_{on,sp}$ is decreased by 56.6% simultaneously. The novel JFP technique is available to achieve power devices with the capacity of high voltage and low power dissipation.

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