Non-recessed-gate quasi-E-mode double heterojunction AlGaN/GaN high electron mobility transistor with high breakdown voltage*

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A non-recessed-gate quasi-E-mode double heterojunction AlGaN/GaN high electron mobility transistor (quasi-E-DHEMT) with a thin barrier, high breakdown voltage and good performance of drain induced barrier lowering (DIBL) was presented. Due to the metal organic chemical vapor deposition (MOCVD) grown 9-nm undoped AlGaN barrier, the effect that the gate metal depleted the two-dimensiomal electron gas (2DEG) was greatly impressed. Therefore, the density of carriers in the channel was nearly zero. Hence, the threshold voltage was above 0 V. Quasi-E-DHEMT with 4.1-μm source-to-drain distance, 2.6-μm gate-to-drain distance, and 0.5-μm gate length showed a drain current of 260 mA/mm. The threshold voltage of this device was 0.165 V when the drain voltage was 10 V and the DIBL was 5.26 mV/V. The quasi-E-DHEMT drain leakage current at a drain voltage of 146 V and a gate voltage of −6 V was below 1 mA/mm. This indicated that the hard breakdown voltage was more than 146 V.

Keywords: GaN-based HEMTs, enhancement-mode, high breakdown voltage

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1. Introduction

Recently, the research on AlGaN/GaN DHEMTs has attracted much attention because of its great potential in microwave and millimeter wave power devices. It is estimated that the performance of the AlGaN/GaN high electron mobility transistor (HEMT) could be improved by inserting an AlGaN layer with an Al composition of 15%, which acted as a back-barrier between the GaN channel layer and the GaN buffer layer, because of the following advantages: firstly, the use of a back-barrier could raise the back side of the conduction band energy (E_c) of the channel layer thus suppressing the hot electrons running into the buffer layer, consequently it could improve the reliability of the device; secondly, by using a back-barrier layer, the confinement of two-dimensiomal electron gas (2DEG) has been greatly improved. Thus, the buffer leakage current and subthreshold leakage current are eliminated.[1–7] Therefore, the breakdown voltage and subthreshold characteristics can be enhanced.

So far, most of the works on DHEMTs have focused on the depletion-mode (D-DHEMT) device. However, from the application point of view, the E-DHEMT is essential and has many advantages. For the applications such as high frequency power amplifiers (PAs) and low noise amplifiers (LNAs), E-mode devices can simplify the circuit configuration and improve the circuit reliability by eliminating the negative power supply,[8] because there is no need to use a negative bias voltage to pinch-off the device. Although E-mode devices provide a smaller drain current and a lower power density compared with D-DHEMTs, they can still offer enough power density for high power applications. Compared with the D-DHEMTs, GaN based E-DHEMTs are difficult to realize because of the existence of high density 2DEG at the AlGaN/GaN heterointerface, which results in a non-pinched-off conduction channel at zero gate bias. Nowadays, several techniques to achieve E-HEMTs have been reported, such as etching the barrier layer of the gate-foot,[9] using a p-type gate structure[10,11] or exposing the device to a fluoride-based plasma treatment.[12] These methods are neither reliable nor stable. For gate recess technology, reproducibility is an issue as it is very hard to control the etch depth and hence the threshold voltage of the devices varies across a sample. For ion implantation, the implanted fluorine ions make the devices very unstable and also degrade the drain breakdown voltage of the device. The ultimate goal of these methods is to decrease the 2DEG in the gate region meanwhile keeping sufficient density in the access region. Therefore, a very thin barrier layer incorporated with the back-barrier layer, which provides reversed polarization charge, is favorable to realize high performance enhancement mode HEMTs. In theory, the threshold voltage of Schottky-gate AlGaN/GaN HEMT is defined as

$$V_{\rm th} = \phi_{\rm B}/e - d\sigma/\varepsilon - \Delta E_{\rm c}/e + E_{\rm f0}/e - \frac{e}{\varepsilon}\int_0^d {\rm d}x \int_0^x N_{\rm si}(x)\,{\rm d}x - edN_{\rm st}/\varepsilon$$

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$$-eN_b/C_b, \quad (1)$$

where ϕ_B is the barrier height, which is partly determined by Al composition, d is barrier layer thickness, σ is the polarization charge at the interface between the AlGaN/GaN, ε is the dielectric constant of the barrier layer, ΔE_c is the conduction band offset at the AlGaN/GaN heterojunction, E_{f0} is the distance between the Fermi level and the conduction band edge, $N_{si}(x)$ is the Si-doping concentration in the barrier layer, N_{st} is the charged surface, N_b are bulk traps, and C_b is the buffer to channel capacitance. According to this theory, after optimization of the AlGaN barrier thickness, Al composition, and back-barrier thickness, the threshold voltage can be shifted above zero volts.

In this paper, we propose a method of a non-recessed-gate to achieve quasi-E-DHEMTs. By using this technique, the Schottky gate can be formed on a damage-free surface, which does not suffer from etching induced defects. In addition, a thin barrier layer is used to achieve the enhancement-mode operation. Moreover, the fabrication process of a non-recessed-gate is relatively simple. Quasi-enhancement-mode operation has been obtained in a large V_{DS} range up to 20 V.

2. Device structure and fabrication

The quasi-E-DHEMT used in this paper was grown on a sapphire substrate by MOCVD. The schematic cross section of the non-recessed-gate quasi-E-DHEMT is shown in Fig. 1. The DHEMT consisted of a low-temperature AlN nucleation layer, a 700-nm unintentionally doped GaN buffer layer and a 700-nm AlGaN back barrier with the Al mole fraction of 15%. Then a 14-nm GaN layer was deposited as a 2DEG channel. Finally, a 9-nm top AlGaN barrier layer with the Al mole fraction of 65% and 1.5-nm GaN cap layer were deposited. Room-temperature Hall measurements showed an electron sheet concentration of 9.84×10^{12} cm^{-2} and a mobility of 1188 cm^2·V^{-1}·s, resulting in a sheet resistance of 752 Ω/□.

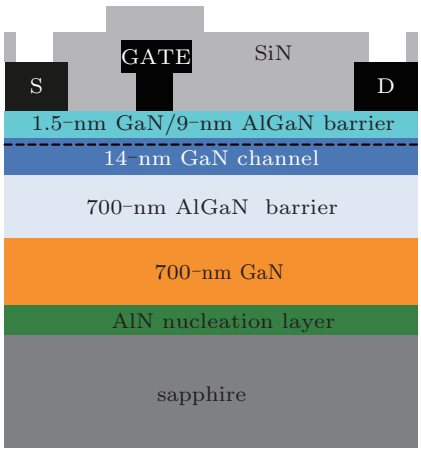


Fig. 1. (color online) Schematic cross section of non-recessed-gate quasi-E-DHEMT.

The device fabrication started with the source/drain contact formation with Ti/Al/Ni/Au (22 nm/140 nm/55 nm/45 nm) by electron beam evaporation and annealed at 850 °C for 30 s. Then, a 140-nm mesa etched by Cl_2-based reactive ion etching (RIE) was used as the device region. The buffer leakage current was as low as 0.4 mA/mm between two isolated mesas at a distance of 5 μm and the voltage across the two isolated mesas was 200 V. Using an on-wafer transfer length method (TLM), the ohmic contact resistance was measured to be 3 Ω·mm due to the unoptimized ohmic metal stacks and annealing on the novel high-Al-composition AlGaN material. Otherwise, the maximum drain current and extrinsic transconductance would be higher. After 60-nm SiN deposition on the surface of the device by PECVD to reduce frequency dispersion, the gate window with a 0.5-μm footprint length was opened by contact photolithography, and then etched by CF_4 plasma in a RIE system at the RF power of 50 W to remove the SiN of the gate region. Finally, a Ni/Ti/Ni (70 nm/80 nm/30 nm) gate electrode was deposited by electron beam evaporation on the device. All the devices in this paper had a gate width of 50 μm, a gate-source spacing of 1 μm, and a gate-drain spacing of 2.6 μm.

3. Results and discussion

The output characteristics of the non-recessed-gate quasi-E-DHEMT are shown in Fig. 2(a). The maximum drain current I_d is 260 mA/mm at $V_{GS} = 2.5$ V and $V_{DS} = 10$ V. The knee voltage is 1.8 V and the turn-on resistance of the E-DHEMT is 10 Ω·mm extracted from the linear region of the output curves at $V_{GS} = 2.5$ V. We define V_{th} as the gate bias intercept of the linear extrapolation of drain current at the point of peak transconductance (g_m). Figure 2(b) shows the V_{th} is 0.165 V when the drain voltage is 10 V. The maximum extrinsic transconductance of 128 mS/mm is obtained because of the large ohmic contact resistance. The Schottky diode characteristics are shown in Fig. 3(a). Under a negative gate bias $V_{GS} = -20$ V and $V_{GS} = -10$ V, the gate current is 4×10^{-3} mA/mm and 6.8×10^{-4} mA/mm respectively, which is larger than the ordinary structure HEMT. This is due to the thin barrier thickness that makes the electrons tunnel through the AlGaN barrier layer more easily.[13] The breakdown voltage V_{br} is measured at a deep closed-gate condition when the $V_{GS} = -6$ V is less than V_{th}. The V_{br} is defined as the voltage at which the drain leakage current I_d reaches 1 mA/mm. Figure 3(b) shows the DC breakdown characteristics. The off-state breakdown voltage is 146 V with the gate-drain distance of 2.6 μm higher than the previous report.[14] It can be obviously seen that the gate leakage current and the drain leakage current dramatically increase at the same time when the drain voltage V_{DS} exceeds 100 V. In the vicinity of the breakdown voltage, the gate leakage current is about 0.5 mA/mm equal to

the buffer leakage current. This means that if the gate leakage current is suppressed by using a thicker barrier layer, higher Al composition, gate dielectric or lowering the defect density under the gate metal, the off-state breakdown voltage can be continuously enhanced. Meanwhile, it is verified that the sub-threshold leakage current could be suppressed by the back barrier layer.

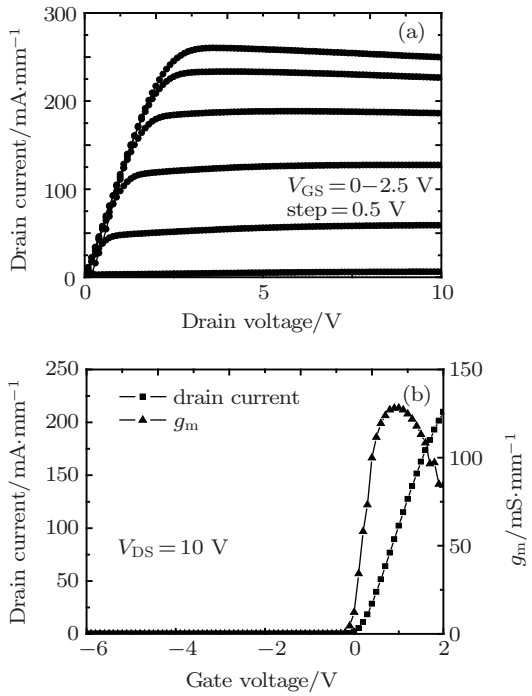


Fig. 2. The DC *I*–*V* (a) output characteristics and (b) transfer characteristics.

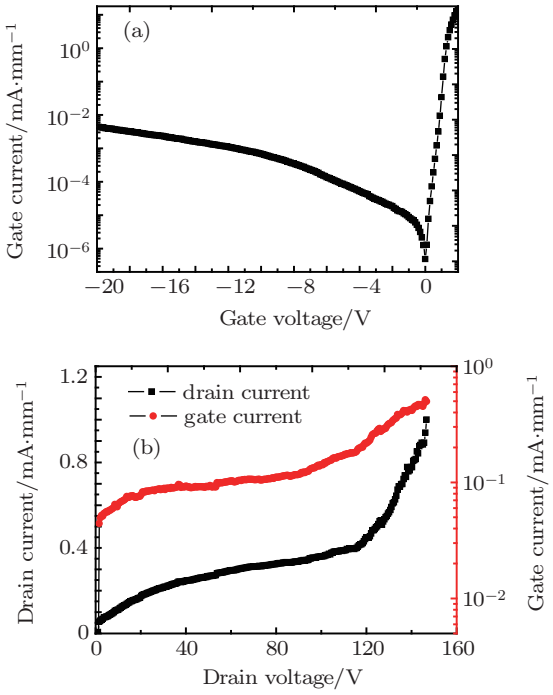


Fig. 3. (color online) (a) Schottky diode characteristics and (b) DC breakdown characteristics.

The transfer characteristics of quasi-E-DHEMT with different drain voltages are shown in Fig. 4. The threshold voltages V_{th} are 0.21 V, 0.2 V, 0.165 V, and 0.11 V when the drain voltages V_d are 1 V, 5 V, 10 V, and 20 V respectively. It can be seen that V_{th} is insensitive to the drain voltage. The DIBL over the drain voltage range of 1 V to 20 V is measured to be 5.26 mV/V. These experimental results show good suppression of DIBL, which indicates that the short channel effect is minimal for this device due to the thinner barrier and the inserted back barrier layer. Otherwise the off-state drain current will reach the ultralow level due to the large gate leakage current. Thus the value of DIBL will continue to decline.

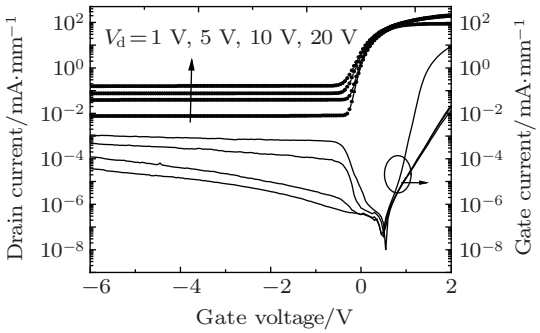


Fig. 4. Transfer characteristics for back-barrier HEMT. The drain voltage was varied with 1 V, 5 V, 10 V, and 20 V.

In Fig. 5, simulated conduction band diagrams of the back-barrier compared with the conventional AlGaN/GaN HEMT using a one-dimensional Poisson equation are shown. The simulation indicates that electron confinement is dramatically improved in the back-barrier structure, therefore, the electrons in the 2DEG channel are confined well on the buffer side, and they cannot spill over to the buffer, suppressing the buffer leakage current. Simultaneously, the back-barrier layer raises the bottom of the conduction band that is exceeding the Fermi level. That is to say, there is no 2DEG in the channel.

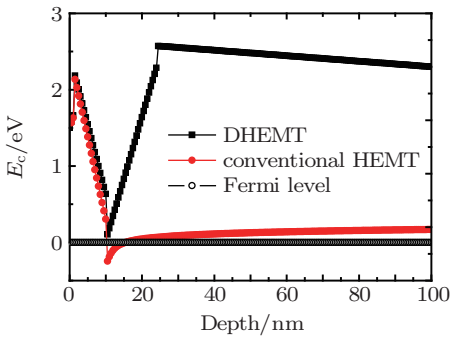


Fig. 5. (color online) Calculated conduction band diagram of DHEMTs and conventional HEMTs.

Pulsed measurements are taken on the non-recessed-gate quasi-E-DHEMT with a pulse width of 500 ns and a pulse period of 1 ms. The quiescent bias points are chosen at (V_{GSQ}, V_{DSQ}) = (0 V, 0 V) and (V_{GSQ}, V_{DSQ}) = (−8 V, 10 V) respectively. In the pulse measurement, the bias point (V_{GSQ},

$V_{DSQ}) = (0\ V, 0\ V)$ is chosen so as to avoid the self-heating effect. At the bias point $(V_{GSQ}, V_{DSQ}) = (-8\ V, 10\ V)$, there is potential difference between the gate and the drain, so the electrons in the gate electrode can be captured by the surface trap. Meanwhile, the large electric field along the 2DEG channel will lead the electrons in the channel to easily spill over to the buffer layer. So that the bias point $(V_{GSQ}, V_{DSQ}) = (-8\ V, 10\ V)$ is selected to evaluate the surface trap effect and buffer layer confinement. From Fig. 6, we can see only 6.87% drain current collapse between the bias point $(V_{GSQ}, V_{DSQ}) = (0\ V, 0\ V)$ with the bias point $(V_{GSQ}, V_{DSQ}) = (-8\ V, 10\ V)$, which reveals that the non-recessed-gate quasi-E-DHEMTs do not suffer from the surface-related defect and hot-carrier injection into the buffer layer. These results demonstrate that a non-recessed-gate could make the gate region free from etching damage and the back barrier layer could suppress the channel punch-through.

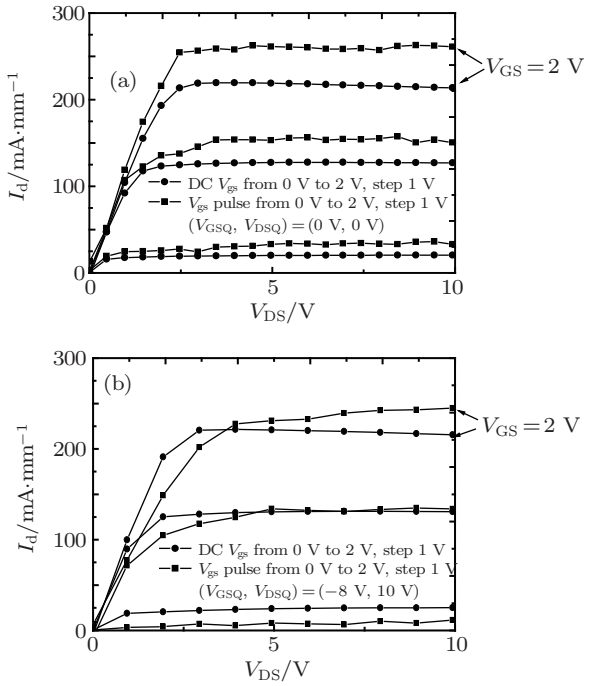


Fig. 6. Comparison of pulsed *I–V* characteristics (a) at point of $(V_{GSQ}, V_{DSQ}) = (0\ V, 0\ V)$ and (b) $(V_{GSQ}, V_{DSQ}) = (-8\ V, 10\ V)$.

4. Conclusion

We have studied a method of fabricating the non-recessed-gate quasi-E-DHEMT to achieve a high breakdown voltage. Owing to the thin barrier layer, the 2DEG can be easily depleted by the gate metal, and the back barrier layer can raise the conduction band under the 2DEG channel to suppress the punch-through so that the breakdown voltage has been increased. Meanwhile, the back barrier generating the reversed polarization charge can deplete the 2DEG channel, which contributes to the E-mode operation. Moreover, a non-recessed gate combined with a back barrier layer can suppress the current collapse, which demonstrates the great potential of this structure for microwave and millimeter power applications.

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