Design consideration and fabrication of 1.2-kV 4H-SiC trenched-and-implanted vertical junction field-effect transistors*

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We present the design consideration and fabrication of 4H-SiC trenched-and-implanted vertical junction field-effect transistors (TI-VJFETs). Different design factors, including channel width, channel doping, and mesa height, are considered and evaluated by numerical simulations. Based on the simulation result, normally-on and normally-off devices are fabricated. The fabricated device has a 12 μm thick drift layer with 8×10^{15} cm^{-3} N-type doping and 2.6 μm channel length. The normally-on device shows a 1.2 kV blocking capability with a minimum on-state resistance of 2.33 mΩ·cm^2, while the normally-off device shows an on-state resistance of 3.85 mΩ·cm^2. Both the on-state and the blocking performances of the device are close to the state-of-the-art values in this voltage range.

Keywords: silicon carbide, trenched-and-implanted vertical junction field-effect transistor, normally-on device, normally-off device

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1. Introduction

Due to its wide band gap, excellent thermal conductivity, and high critical field strength, silicon carbide (SiC) has now been widely recognized as an ideal base material for high-power, high-temperature, and high-frequency devices.[1,2] In particular, the high critical electric field of SiC (10 times greater to that of Si) permits high efficiency power electronic switching devices to be fabricated with high voltage ratings. Compared with other wide-bandgap semiconductors, such as GaN and diamond, SiC has the most mature fabrication technology. In recent years, numerous SiC high power switching devices such as Schottky barrier diodes (SBDs), metal–oxide–semiconductor field-effect transistors (MOSFETs), junction field-effect transistors (JFETs), bipolar junction transistors (BJTs), and insulated gate bipolar transistors (IGBTs) have been demonstrated[3–10] and some of them have already entered the commercial market.

For 4H-SiC based switching devices, the junction field effect transistor is by far the most mature technology and it is also the first commercial SiC transistor structure entering the market. Having no interface issues, SiC JFETs can fully benefit from the superior properties of SiC. With dedicated packages, the application of SiC JFETs has been pushed to an extremely high temperature of 550 °C and has also been demonstrated under cryogenic temperature down to −268 °C. In addition, a record low resistance of 2.8 mΩ·cm^2 with 1.9 kV blocking voltage and a high saturation current of 120 A have also been, respectively, reported in SiC JFETs in recent years.[11,12]

The trenched-and-implanted vertical JFET (TI-VJFET) structure is an excellent design to realize the SiC JFET.[13] With no requirement of epi-regrowth or stringent lithography alignment, the TI-VJFET structure is simple to fabricate and can achieve a high current density. In addition, by fine adjusting the channel width, the device can be readily made to be either normally on or normally off, showing a great convenience in device design and fabrication.

In this paper, the design factors of the SiC TI-VJFET structure, including channel width, channel doping, and mesa height, are considered and evaluated by numerical simulations. With extensive device simulations and delicate processing technologies, SiC TI-VJFETs with different channel widths are fabricated and measured. The measurement result shows a superior device performance. Along with the simulation and the fabrication results, a comparison between normally-on and normally-off devices is presented. The resistance distribution of the fabricated device is also discussed in this paper.

2. Device structure and simulation

The schematic cross section of SiC TI-VJFETs is shown in Fig. 1. The TI-VJFET structure typically consists of three epi-layers, including a drift layer, a channel layer, and a highly doped contact layer. The drift layer is used to withstand the desired high voltage. The channel layer is used to modulate the threshold voltage. The top highly doped layer is used to obtain a low ohmic resistance in the source contact. In the voltage range of 1–2 kV, the channel doping concentration is usually

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equal to that of the drift layer. The design factors are mainly the channel length (L_{ch} in Fig. 1) controlled by the mesa height and the channel width controlled by the mesa width (W_{ch} in Fig. 1).

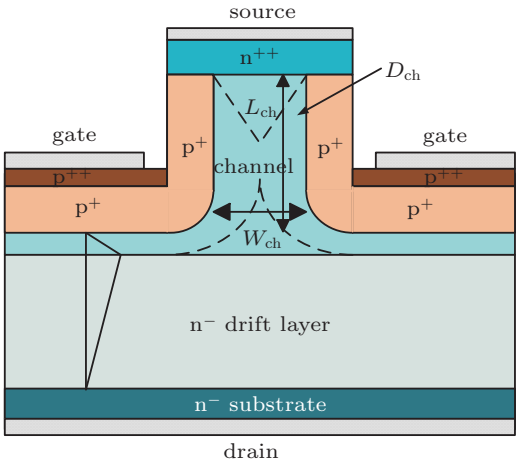


Fig. 1. (color online) Schemicatic cross-sectional view of the TI-VJFET unit cell.

To obtain a blocking capability of 1.2 kV, a drift layer with a thickness of 12 μm and a doping concentration of 8×10^{15} cm^{-3} is chosen. The width of the cell pitch is set to be 5 μm, and the channel doping concentration is 8×10^{15} cm^{-3}.

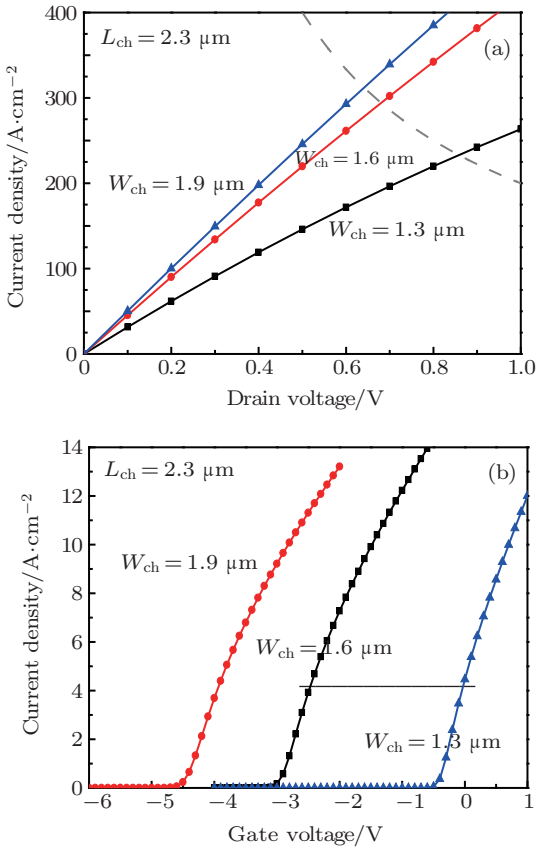


Fig. 2. (color online) Simulated (a) output characteristics and (b) transfer characteristics of TI-JFETs with different channel widths. The output curves are simulated with a gate bias of 1.6 V, and the transfer curves are simulated with a drain voltage of 0.05 V. The dash line indicates a power density of 200 W/cm^2.

In the device simulation, the channel is designed to have an opening from 1.3 μm to 1.9 μm, with a channel length of 2.3 μm. The simulated output and transfer curves are depicted in Fig. 2. The power density limit of 200 W/cm^2 is indicated as a dash line in the figure. In the output characteristics simulation, the gate voltage is 1.6 V, and in the transfer characteristics simulation, the drain voltage is 0.05 V. As shown in Fig. 2, the current conducting capability of the TI-JFET is very sensitive to its channel opening. By increasing the channel opening from 1.3 μm to 1.9 μm, the forward current density increases from 171 A/cm^2 to 292 A/cm^2 at the drain voltage of 0.6 V. However, a wider channel also leads to a lower threshold voltage and a higher pinch-off voltage of the channel. In actual device applications, a large negative gate bias is usually needed to maintain a good blocking performance.

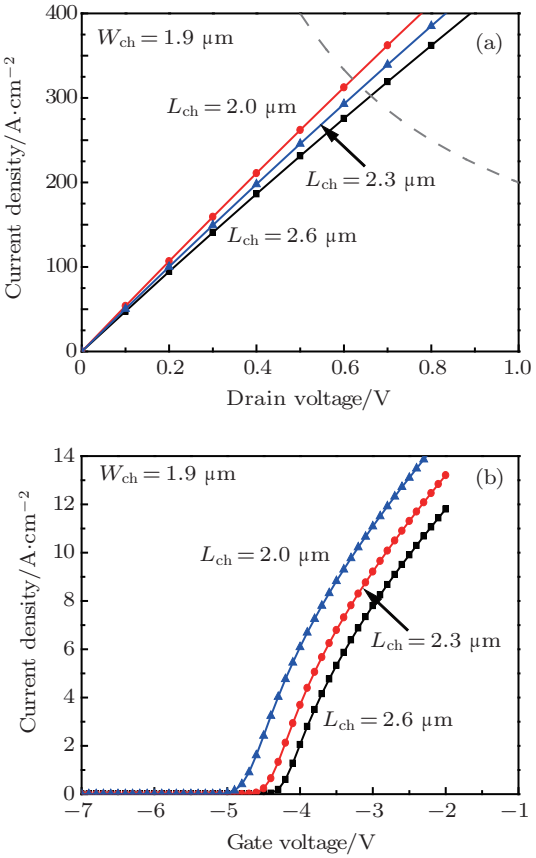


Fig. 3. (color online) Simulated (a) output characteristics and (b) transfer characteristics of TI-JFETs with different channel lengths. The output curves are simulated with a gate bias of 1.6 V, and the transfer curves are simulated with a drain voltage of 0.05 V. The dash line indicates a power density of 200 W/cm^2.

As for the channel length, the simulated output and transfer curves are depicted in Fig. 3, with a channel opening of 1.9 μm and a channel length changing from 2.0 μm to 2.6 μm. Compared with the channel width, the channel length does not largely affect the device characteristics. In practice, a larger channel length leads to a better blocking performance. However, a deep trench also brings more challenges in device manufacturing.

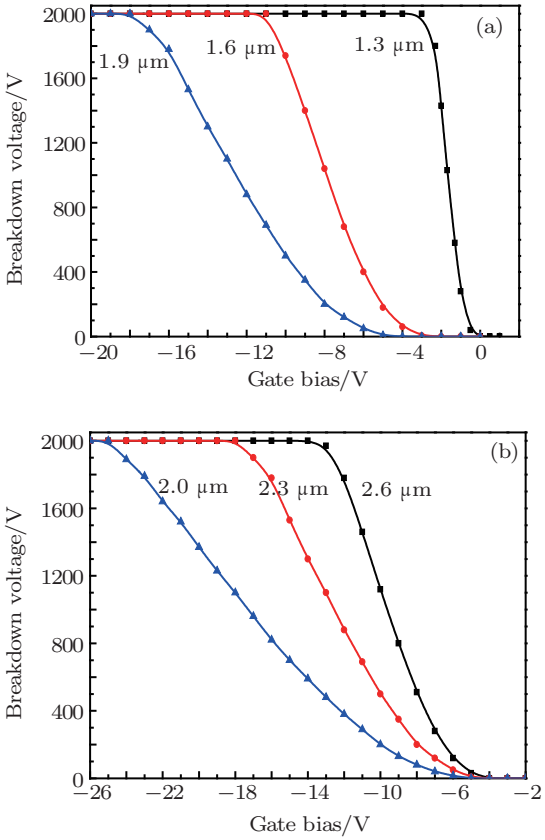


Fig. 4. (color online) Simulated relationship between gate bias and breakdown voltage. (a) The channel length is assumed to be 2.3 μm and the channel width changes from 1.3 μm to 1.9 μm. (b) The channel width is assumed to be 1.9 μm and channel length changes from 2.0 μm to 2.6 μm.

Another important issue is the influence of the channel width and the channel length to the device's blocking performance. In the forward blocking state, the channel of the TI-JFET has to be pinched off by the depletion of adjacent gate PN junctions. As the drain voltage increases, the drain potential penetrates into the channel and lowers the potential barrier. A long channel and an optimized length/width ratio are, hence, desired in order to obtain a good blocking performance. Figure 4 shows the relationship between gate bias and breakdown voltage of different device designs. In the device simulation, the breakdown voltage is obtained at leakage current exceeding 1 μA. In Fig. 4(a), the channel length is assumed to be 2.3 μm and the channel width changes from 1.3 μm to 1.9 μm. In Fig. 4(b), the channel width is assumed to be 1.9 μm and the channel length changes from 2.0 μm to 2.6 μm. As is shown, with a larger channel width or a smaller channel length, the curve of gate bias versus breakdown voltage becomes less steep, which means that a larger reverse gate bias is needed to pinch off the channel. In the device fabrication, a gate bias less than 5 V from on-state to off-state is desired.

3. Device fabrication

Based on the above simulation results, customer-ordered 4H-SiC wafers with three N-doped epi-layers were purchased. The device fabrication started with trench etching of the 4H-SiC wafer. A metal layer was first sputtered and defined to serve as the dry etching mask. Deep trench etching was conducted by SF_6 based dry etching in a reactive ion etching system. The etching depth was about 4 μm, and the mesa line widths were intentionally varied from 2.0 μm to 2.4 μm across the wafer. A cross-sectional view of the resulting mesa and trench structure is shown in Fig. 5.

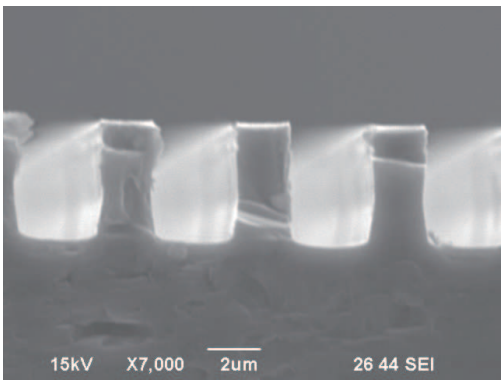


Fig. 5. Cross-sectional view of the mesa and trench structure.

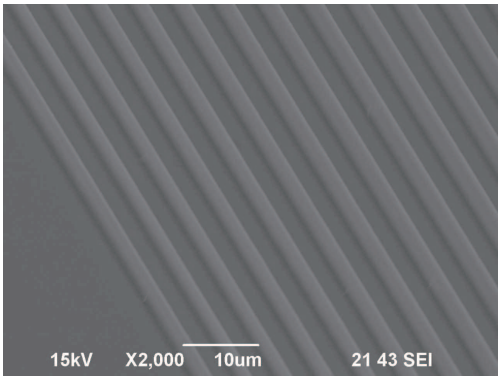


Fig. 6. SEM picture of SiO_2 implanted mask.

The P^+ region in the mesa sidewalls and trench bottoms were formed by multiple normal and tilted Al ion implantations. The energies and the doses of the four-time implantation were 360 keV and 2.7×10^{13} cm^{-2}, 280 keV and 3.7×10^{14} cm^{-2}, 160 keV and 1.9×10^{14} cm^{-2}, and 110 keV and 4.1×10^{13} cm^{-2}, respectively. A thick SiO_2 layer was firstly deposited and patterned by standard lithography to serve as the implantation mask. A field guard ring termination was adopted as the termination structure and the P^+ implanted rings were formed simultaneously with the active region in this ion-implantation. The area of the active region was 9×10^{-4} cm^2 in the small device, and the termination length was 90 μm. An SEM photograph of the implantation mask in the termination structure is shown in Fig. 6. After the ion implantation, the wafer was cleaned and annealed at 1550 °C in Ar ambient for 30 min to active the implanted Al atoms.

The surface passivation was accomplished by a 1.5 h wet oxidation at 1050 °C, followed by a 200 nm PECVD Si_3N_4 and SiO_2. After surface passivation layer opening, nickel was sputtered in the active area and annealed to form the source and gate ohmic contacts. A SEM picture of the mesa structure after gate and source contacts formation is shown in Fig. 7. Figure 8 shows the device with a passivation layer opening in the active area. The backside ohmic contact was formed by a tri-layer metallization of Ti/Ni/TiW. The TiW layer is necessary since it can prevent the Ni metal from oxidation during the annealing process. The sample was annealed at 950 °C to form a good ohmic contact in a high-purity N_2 atmosphere.

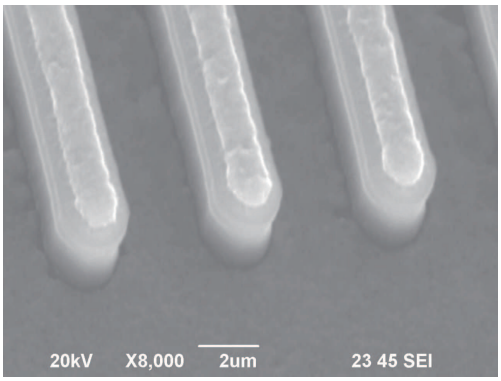


Fig. 7. SEM photograph of the mesa structure after gate and source contacts formation.

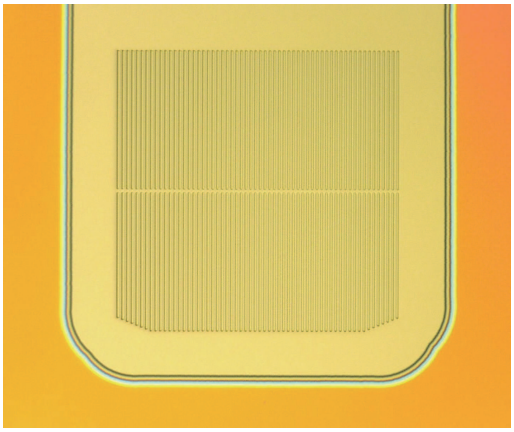


Fig. 8. (color online) Optical photograph of a small device with passivation layer opening.

Finally, a dielectric material like polyimide was spin-coated on the sample and etched back to fill the trenches and expose the mesa tops. A thick overlay metal consisting mainly of Al was then deposited and patterned by wet etching to form the source pad and the gate pad of the device.

4. Device characterization and results

4.1. Transfer and forward conduction characterization

The fabricated devices were characterized at the wafer level by using a HP 4155B semiconductor parameter analyzer and a probing station. During characterization, a dedicated measurement setup was built to minimize the background noise. The tested devices had an active area of 9×10^{-4} cm^2. In order to compare with the simulated values easily, all currents were converted into current densities in the following discussion.

Figure 9 shows the transfer characteristics and the threshold voltages of the fabricated devices with different channel widths. During the measurement, the drain voltage was kept as 0.05 V and the gate voltage was swept from −2.5 V to 2.5 V. As shown, the threshold voltage of the fabricated TI-VJFET changes from 1.3 V to −1.0 V as the channel width increases from 1.0 μm to 1.4 μm. Note that the fabrication of normally-on or normally-off devices can be achieved by manipulating the line width of the channel. This is in agreement with the above simulations.

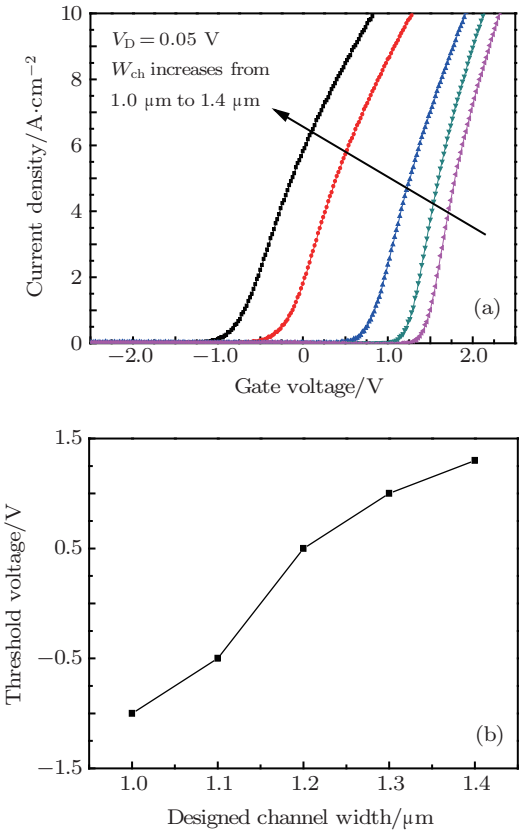


Fig. 9. (color online) (a) Transfer curves and (b) threshold voltages of the fabricated TI-VJFETs.

Figures 10(a)–10(c) show the output I–V curves of the fabricated devices with different channel widths. With the channel opening of 1.0 μm, the device performs like a normally-off device, while with the channel opening of 1.4 μm, the device performs like a normally-on device. In addition, with the channel width decreasing from 1.4 μm to 1.0 μm, the device's forward conduction capability also drops dramatically, from about 800 A/cm^{-2} to 220 A/cm^{-2} with a gate bias (V_{GS}) of 2.5 V and a drain voltage (V_{DS}) of 2 V. For

the specific device described in Fig. 10(c), with V_{GS} of 2.5 V and V_{DS} of 0.5 V, the forward current density is 215 A/cm^2, corresponding to a specific on-resistance of 2.33 mΩ·cm^2, which is close to the lowest reported value to date for 1.2-kV SiC JFETs.

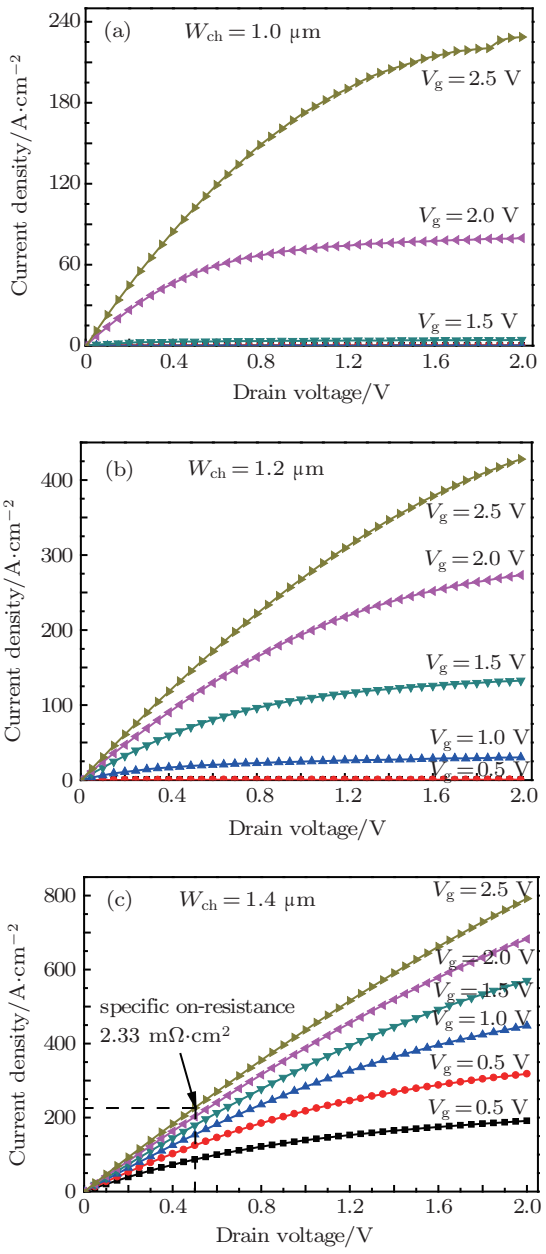


Fig. 10. (color online) Forward *I*–*V* curves of the TI-VJFETs with different channel widths: (a) 1.0 μm, (b) 1.2 μm, (c) 1.4 μm.

4.2. Gate-to-source junction characterization

The gate control of SiC-VJFET devices is accomplished by the space modulation of the gate to source PN junction. For normally-on devices, a negative gate bias is needed to pinch-off the channel and achieve the desired blocking voltage. So, a reliable gate to source junction is necessary for TI-VJFET devices. Figure 11 presents the gate to source blocking capability of the fabricated devices. As is shown, the leakage current is kept relatively small up to 40 V reverse bias, which is enough to pinch off the vertical channel. This indicates that the fabricated devices have robust gate junctions and a negative gate voltage can be applied to obtain a high blocking voltage.

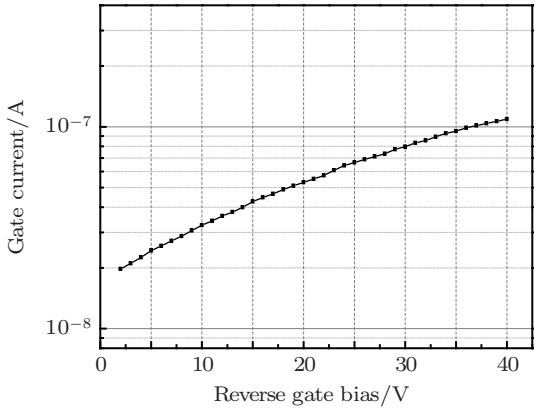


Fig. 11. Reverse characteristics of the gate to source junction.

4.3. Reverse blocking characterization

The reverse blocking test was performed with a high voltage power source and a 24-bit source meter. The samples were immersed in Fluorinert^{TM} dielectric liquid to prevent air breakdown. The devices in Fig. 10 with channel widths of 1.4 μm and 1.2 μm were tested with a gate bias of −15 V. The measured reverse *I*–*V* curves are depicted in Fig. 12, both linearly and logarithmically.

As shown in Fig. 12, the devices have a breakdown voltage of 1200 V. The leakage keeps relatively low until 800 V and remains less than 1 μA at 1200 V. This indicates a good pinch-off capability of the channel and the reliable termination structure of the device.

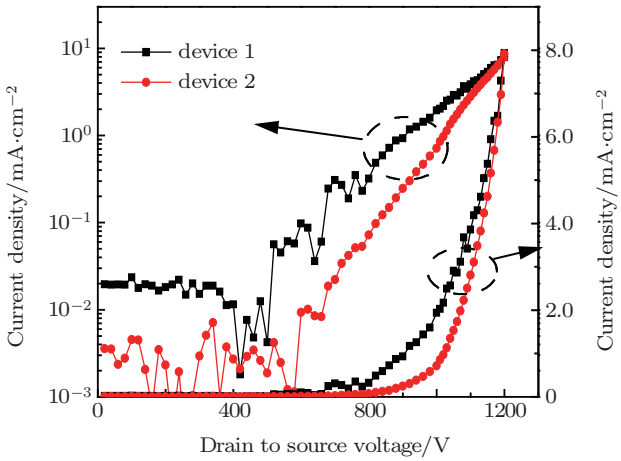


Fig. 12. (color online) Breakdown curves of the fabricated TI-VJFETs.

5. Discussion

Normally-on and normally-off TI-VJFETs have both merits and demerits. The normally-off device has the natural advantage in safe operation when a zero gate voltage is

applied, whereas the normally-on device has a 39.5% lower on-resistance and an about three-time higher saturation current, as is shown in this work. In addition, since the TI-VJFET is a PN junction controlled device, the gate bias should not exceed positive 2.5 V at the forward conduction mode, thus leaving only a small room ($\sim$ 1.5 V) for the gate control circuit. A compromised design is to set the gate threshold voltage to be around -1 V. On one hand, the relatively large channel opening guarantees a high current conduction capability and a lower on-resistance. On the other hand, with the threshold voltage of -1 V, the device channel can be completely pinched off with a negative gate bias of 15 V. This can be achieved easily by low voltage silicon MOSFETs in a cascade configuration.

Another interesting issue is the specific on-resistance of the fabricated devices. For the device in Fig. 10(c), the specific on-resistance of 2.33 mΩ·cm^2 has three main contributions, which are: the wafer intrinsic resistance, the device channel resistance, and the process induced resistance. The wafer substrate has a thickness of 300 μm and resistivity of 0.18 Ω·cm, leading to a specific resistance of 0.54 mΩ·cm^2. The 12-μm drift layer with an N-type doping concentration of 8×10^{15}cm^{-3} has a specific resistance of 0.84 mΩ·cm^2, assuming an electron mobility of 750 cm^2/Vs. In addition, the channel resistance is 0.57 mΩ·cm^2, calculated by using a channel doping concentration of 8×10^{15} cm^{-3}, a channel length of 2.3 μm, and a channel width/cell pitch ratio of 1.4 μm/5 μm. Thus, the additional resistance caused by the process is 0.38 mΩ·cm^2. This low additional resistance indicates the successful fabrication process of the present device.

6. Conclusion

This paper presents the design consideration and fabrication of 1.2-kV 4H-SiC TI-VJFETs. Devices with different mesa heights and channel openings were simulated and both normally-off and normally-on devices were fabricated. With the channel opening of 1.4 μm, the fabricated devices had a minimum specific on-resistance of 2.33 mΩ·cm^2, which is close to the lowest value at this voltage.[14] In the reverse blocking test, the fabricated devices reached a blocking voltage of 1200 V with a negative gate bias of 15 V.

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