Mutator for transferring a memristor emulator into meminductive and memcapacitive circuits*

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In this paper, a concise but effective interface circuit for transforming a memristor into meminductive and memcapacitive systems is designed. This newly proposed interface circuit, constructed by only two current conveyors, is equipped with three available ports, which can provide six connecting combinations in terms of one resistor, one capacitor, and one memristor. For the sake of confirming the design effectiveness, theoretical and simulation discussions are hence introduced and all the experimental waveforms provide conclusive evidence to validate the correctness of these new mutators. The most attractive features of this new interface circuit are the floating terminals and convenient practical implementation.

Keywords: memristor, meminductive, memcapacitive, self-excited oscillator

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1. Introduction

The memristor was originally envisioned by Chua as the fourth non-linear passive two-terminal fundamental circuit element in 1971.[1] In 2009, by taking an extra step, Chua *et al.* generalized the concept of memory devices to the capacitor and the inductor, and brought forward two other dynamic elements called the memcapacitor and the meminductor.[2] Together with the memristor, the memcapacitor and the meminductor constitute an important class of two terminal circuit mem-elements, which can retain memory of their past states. The memory features of these elements are related to the corresponding internal states and can also be influenced by the externally imposed control parameters. These elements, as functionally combined in integrated circuits, will certainly play important roles in future applications, in the area of non-volatile memory, low-power and remote sensing, oscillators, neuromorphic and biological systems, quantum computing, etc.[2–5]

Currently, since all these three mem-elements are not commercially available, a lot of emulating methods have been brought forward to analyze their equivalent dynamical characteristics beforehand. The memristor has attracted relatively more extensive research attention after the announcement of the successful fabrication of a solid memristive system by the HP Lab.[5–17]

Note that, in addition to information, memcapacitors and meminductors are capable of storing energy, and therefore, could explore new orientations in the technologically important area of energy storage and circuit operation.[18] As two newly emerged elements, only a few articles relating to the meminductor and the memcapacitor have been published. Via replacing a plate of a parallel-plate capacitor with a strained elastic membrane, a bistable non-volatile memcapacitor was realized in Ref. [19] and then the chaotic behavior existing in this memcapacitive circuit was discussed. Biolek and his team have established several behavioral models of meminductive and memcapacitive systems in accordance with the constitutive relations, and they also proposed mutators for simulating a meminductor and a memcapacitor by a grounded memristor.[20–24]

By making use of the microprocessor based memristive emulator proposed in Ref. [10], memcapacitive and meminductive systems inherently connected in a series with a resistor were proposed by Pershin and Di Ventra.[25] References [24] and [26] pointed out the limitation of the transforming mutators proposed in Ref. [25] and designed a more exact memcapacitive emulator without the parasitic resistor. A grounded memcapacitive emulator was experimentally introduced in Ref. [27], of which the memcapacitance can hardly be obtained with high precision in consideration of the nonlinear response of the light-dependent resistor. Mutators for transferring a memristor into floating memcapacitive and meminductive systems were conceptually proposed in Ref. [28]. Interestingly, by pointing out that most of the preceding memcapacitor emulators had an identical character of being designed necessarily based on the memristor, a new memristor-less memcapacitor emulator was contrived in Ref. [29]. Recently, based on the memristor proposed in Ref. [14], a novel meminductor emulator was designed and experimentally tested in Ref. [30]. These emulators have assisted researchers commendably in discovering the dynamic behaviors and potential applications

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of these memory elements in circuit design.

These memory elements are of very general interest in science and engineering and are potentially useful not just in information storage, but also apparently in other areas of research. However, since these elements are currently unavailable as commercial off-the-shelf components, this paper focuses on designing a concise interface circuit which can transfer the previously proposed memristive emulator into meminductive and memcapacitive circuits.

2. Floating memristor emulator

Inspired by Ref. [28], a practical memcapacitor emulator without the parasitic resistor and grounded restriction had been formulated and experimentally tested in Ref. [31], by making use of the relation between the terminal voltage and the current of a floating memristive circuit. Subsequently, a meminductive circuit inherently parasitized with dissipative elements, resistor and memristor, was put forward in Ref. [32], also with the assistance of a floating memristor emulator. Clearly, the floating memristive circuit is essential in these two designs. However, the memristive circuit earlier introduced in Ref. [31] has evident insufficiency that the emulator itself cannot guarantee the equality between the input and output currents of its two terminals. The memristor emulator used in Ref. [32] has upgraded the performance by the utilization of two current conveyors and hence can ensure the current equality. By referring to Ref. [32], the memristive circuit of Ref. [31] can be easily improved to achieve the current equality by two current conveyors as well, as shown in Fig. 1.

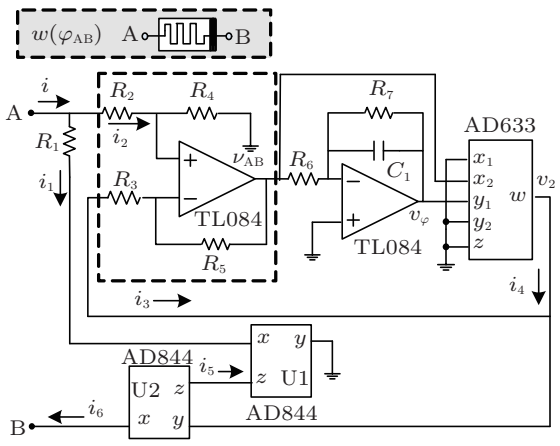


Fig. 1. The circuit diagram of memristor emualtor.

Therefore, a mathematical description of the flux-controlled memductance can be directly introduced by referring to Ref. [31]

$$W(\varphi_{\rm AB}) = \frac{1}{R_1}\left(1+\frac{1}{10R_6C_1}\varphi_{\rm AB}\right), \tag{1}$$

where $\varphi_{\rm AB}$ is defined as the integral of terminal voltage $v_{\rm AB}$. Equation (1) apparently shows that the control function of memductance is of linearity with respect to flux $\varphi_{\rm AB}$. This control function can be varied by adding a computing circuit to the input terminal y_1 of the multiplier chip. For example, by adding one more multiplier chip, equation (1) can be modified into a quadratic equation in terms of flux $\varphi_{\rm AB}$. In consideration of simplicity, only the linear flux-controlled memritor emulator is considered in this paper. By taking advantage of Ohm's law, equation (1) can be rewritten as

$$i = W(\varphi_{\rm AB})\frac{{\rm d}\varphi_{\rm AB}}{{\rm d}t}. \tag{2}$$

Hence, the current going through the memristor emulator can be computed by solving Eq. (2), which implies that the internal state of the memristor emulator is dynamically varying in accordance with the integral of the terminal voltage.

Assuming that a voltage $v_{\rm AB}(t)$ of a square wave with period T is imposed upon the memristor terminals A and B, namely

$$v_{\rm AB}(t) = \begin{cases} A_{\rm m}, & 0 \le t < \dfrac{1}{2f}, \\ -A_{\rm m}, & \dfrac{1}{2f} \le t < \dfrac{1}{f}, \end{cases} \tag{3}$$

where f is the frequency of the square wave. This square wave can be represented by means of a Fourier series

$$\begin{aligned} v_{\rm FAB}(t) &= \frac{4A_{\rm m}}{\pi}\left[\sin(2\pi ft)+\frac{1}{3}\sin(6\pi ft)+\cdots\right] \\ &= \frac{4A_{\rm m}}{\pi}\sum_{n=0}^{\infty}\frac{1}{2n+1}\sin[(4n+2)\pi ft]. \end{aligned} \tag{4}$$

Since flux $\varphi_{\rm AB}$ is actually the integral of $v_{\rm AB}(t)$, by carrying out an integral operation on both sides of Eq. (4), it hence can be calculated that

$$\begin{aligned} \varphi_{\rm AB}(t) &= -\frac{2A_{\rm m}}{\pi^2 f}\left[\cos(2\pi ft)+\frac{1}{9}\cos(6\pi ft)\right. \\ &\quad \left.+\frac{1}{25}\cos(10\pi ft)+\cdots\right] \\ &= -\frac{2A_{\rm m}}{\pi^2 f}\sum_{n=0}^{\infty}\frac{1}{(2n+1)^2}\cos[(4n+2)\pi ft]. \end{aligned} \tag{5}$$

It is worth noting that since the amplitude of the high frequency item is relative small, here, only the first two items are adopted to represent $\varphi_{\rm AB}$ approximately

$$\varphi_{\rm AB}(t) = -\frac{2A_{\rm m}}{\pi^2 f}\left[\cos(2\pi ft)+\frac{1}{9}\cos(6\pi ft)\right]. \tag{6}$$

The memductance hence can be calculated as

$$\begin{aligned} W(f,t) &= \frac{1}{R_1}\left\{1-\frac{A_{\rm m}}{5R_6C_1\pi^2 f}\right. \\ &\quad \left.\times\left[\cos(2\pi ft)+\frac{1}{9}\cos(6\pi ft)\right]\right\}. \end{aligned} \tag{7}$$

Note that, it can be calculated that possible values of the two cosine items enclosed by the inside bracket in Eq. (7) are located in an interval of $[-1.11, 1.11]$. Therefore, in order to guarantee positive memductance, the parameter configuration of the forced voltage is supposed to satisfy the following condition:

$$\frac{f}{A_{\rm m}} > \frac{0.22}{R_6 C_1 \pi^2}. \tag{8}$$

Based on Eqs. (7) and (8), all the possible values of memductance satisfy

$$0 < W < \frac{2}{R_1}. \tag{9}$$

The result of Eq. (9) is identical with that obtained in Ref. [31]. Actually, for other periodical forcing voltages with different waveforms, etc., triangular wave or sawtooth wave, as long as the amplitude of the DC component is equivalent to zero, values of memductance satisfy the boundary condition of Eq. (9).

For the sake of simplicity, a sinusoidal forcing voltage is a more appropriate candidate for approaching the characters of the memristor with the memductance of Eq. (1). On the basis of $v_{\rm AB} = A_{\rm m}\cos(2\pi f t)$, the time-points $t_{\max}$ and $t_{\min}$, corresponding to the maximal and minimal values of memductance, respectively, can be computed as

$$t_{\max} = \frac{4m+1}{4f}, \quad t_{\min} = \frac{4m+3}{4f}, \tag{10}$$

where, m is a natural number. Equation (10) also implies that the varying period of memductance is identical to the period of the forcing voltage. In accordance with Eq. (2), the current i can then be calculated by

$$\begin{aligned} i &= \frac{A_{\rm m}}{R_1}\cos(2\pi f t) + \frac{A_{\rm m}^2}{40\pi R_1 R_6 C_1 f}\sin(4\pi f t) \\ &= i_{1\rm f} + i_{2\rm f}, \end{aligned} \tag{11}$$

which apparently implies that current i includes two frequency components, $i_{1\rm f}$ and $i_{2\rm f}$. The $i_{1\rm f}$ is proportional to imposed voltage $v_{\rm AB}$ in terms of coefficient R_1, while $i_{2\rm f}$ possesses the frequency twice as big as $v_{\rm AB}$ and the variable amplitude of frequency-dependence. This frequency character of $i_{2\rm f}$ indicates that the curve of i versus $v_{\rm AB}$ is not a straight line but a Lissajous-like loop, which can be correspondingly shrunk as the frequency of the imposed voltage increases.

In the following section, by taking advantage of this improved memristor emulator, an interface circuit using two current conveyors for transferring a floating memristor into memcapacitive and meminductive circuits are discussed. The memcapacitive circuit proposed in this paper is different from that using four current conveyors as depicted in Ref. [31]. Although the meminductive circuit addressed in Ref. [32] also has three ports, reference [32] only pays attention to one connecting combination of meminductive character and more importantly, no experimental results as applied in practical circuits are presented in Ref. [32].

3. Design of meminductive and memcapacitive circuits

Since prospective designs of the solid-state meminductor and memcapacitor have not been started, it is of significant importance to design effective circuits currently to investigate their dynamic behaviors. It has been stressed in Ref. [26] that, from the view point of circuit response, memcapacitive and meminductive operation models can be realized by the appropriate utilization of a memristor emulator. As shown in Ref. [2], a canonical lossless flux-controlled meminductive and charge-controlled memcapacitive systems can be defined by the following equations, respectively

$$i_x(t) = L_{\rm m}^{-1}\left[\int_{-\infty}^{t}\varphi_x(\tau)\,{\rm d}\tau\right]\varphi_x(t), \tag{12a}$$

$$v_x(t) = C_{\rm m}^{-1}\left[\int_{-\infty}^{t}q_x(\tau)\,{\rm d}\tau\right]q_x(t), \tag{12b}$$

where $\varphi_x(t)$ is the flux of the inductor, $i_x(t)$ is the internal current, $L_{\rm m}$ represents the meminductance, $v_x(t)$ is the terminal voltage, $q_x(t)$ is the integration of current $i_x(t)$, and $C_{\rm m}$ represents the memcapacitance.

3.1. Design of meminductive circuit

To obtain a circuit with meminductive characteristics, there are various amplifier-*RC* methods, as summarized in Ref. [33]. In this subsection, a brief meminductive circuit consisting of one memristor, one capacitor, one resistor and two current conveyors, is newly designed and analyzed. The key part of this circuit is the utilization of the previously proposed floating memristor emulator to achieve nonlinear controllable meminductance, as shown in Fig. 2(a).

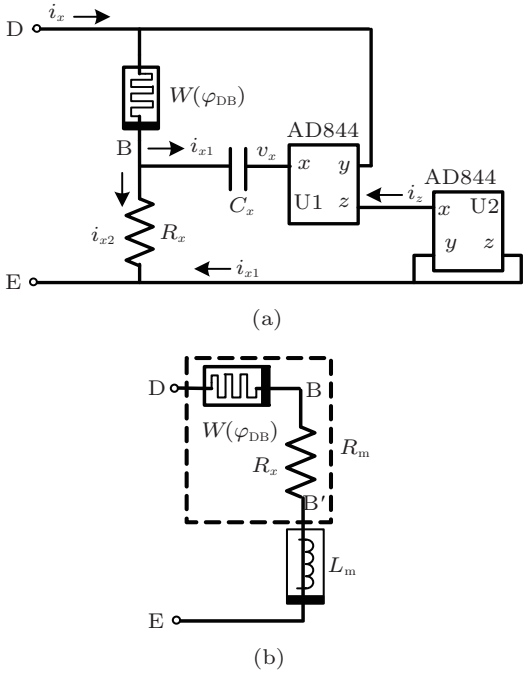


Fig. 2. Meminductive circuit (a) schematic diagram (b) equivalent circuit.

The two current conveyor chips, AD844, are labeled as U1 and U2, respectively. According to their inherent properties, we can obtain

$$v_x = v_{\rm D}, \quad i_{x1} = i_z, \tag{13}$$

where $v_{\rm D}$ is the voltage of terminal D. The U2 is used to change the flowing direction of current i_z, which can guarantee the relation of $i_{x1} = i_z$. Based on Ohm's Law, the following two equations hold:

$$i_x = v_{\rm DB} W(\varphi_{\rm DB}), \quad i_{x2} = \frac{(-v_{\rm DB} + v_{\rm DE})}{R_x}, \tag{14}$$

where, $v_{\rm DE}$ is the voltage source imposed on the two terminals of the meminductive circuit and $v_{\rm DB}$ is the voltage across the memristor emulator, and $v_{\rm B}$ and $v_{\rm E}$ are the voltages of node B and terminal E, respectively. For capacitor C_x, since $v_x = v_{\rm D}$, the current passing through its two terminals can be calculated by

$$i_{x1} = -C_x \frac{{\rm d}v_{\rm DB}}{{\rm d}t}. \tag{15}$$

According to Kirchhoff's current law, the current flowing into a meminductive circuit can be computed as

$$i_x = i_{x2} + i_{x1}. \tag{16}$$

By combining Eqs. (14)–(16), we can obtain

$$v_{\rm DE} = \frac{C_x R_x}{W(\varphi_{\rm DB})} \frac{{\rm d}i_x}{{\rm d}t} + i_x \left[R_x + \frac{1}{W(\varphi_{\rm DB})} \right]. \tag{17}$$

Equation (17) indicates that the circuit depicted in Fig. 2(a) can be simplified equivalently as one resistor, one memristor, and one meminductor connected in a series, as shown in Fig. 2(b), where the memristor connected in the series with the resistor is denoted by $R_{\rm m}$. According to Ohm's law, the equivalent memristance can be identified as

$$R_{\rm m} = \frac{1}{W(\varphi_{\rm DB})} + R_x. \tag{18}$$

Note that, inductance is defined as a parameter to present the constitutive relationship between the flux and the current, and since $W(\varphi_{\rm AB})$ is not constant but flux-dependent, it is improper to derive the equivalent meminductance directly from Eq. (17) in terms of the voltage and the derivative of the current.

By applying an integral operation to Eqs. (14)–(16), the following four equalities hold:

$$\begin{aligned} q_x &= \int v_{\rm DB} \left[\frac{1}{R_1} \left(1 + \frac{1}{10 R_6 C_1} \varphi_{\rm DB} \right) \right] {\rm d}t = \varphi_{\rm DB} W(0.5\varphi_{\rm DB}), \\ q_{x2} &= \frac{(-\varphi_{\rm DB} + \varphi_{\rm DE})}{R_x}, \end{aligned} \tag{19}$$

$$q_{x1} = -C_x v_{\rm DB} = -C_x \frac{i_x}{W(\varphi_{\rm DB})}, \tag{20}$$

$$q_x = q_{x2} + q_{x1}. \tag{21}$$

Combining Eqs. (19)–(21), we can get the following equation to describe this meminductive circuit:

$$\varphi_{\rm DE} = \frac{C_x R_x}{W(\varphi_{\rm DB})} i_x + q_x \left[R_x + \frac{1}{W(0.5\varphi_{\rm DB})} \right]. \tag{22}$$

On the basis of Eq. (22), the nonlinear controllable meminductance hence can be identified as

$$L_{\rm m} = \frac{C_x R_x}{W(\varphi_{\rm DB})}. \tag{23}$$

Apparently, comparing Eq. (22) with Eq. (17), the mathematical expression of the second item enclosed in the square bracket is different owing to the coefficient 0.5, which implies that it is incorrect to derive the equivalent memristance directly from Eq. (22). It can be seen from Eq. (23) that the meminductance is controlled by the terminal flux of the equivalent serial memristor, not by the meminductor itself. Here, the flux of the equivalent meminductor can be exhibited in terms of current i_x or the voltage across the memristor, namely

$$\varphi_{\rm L} = C_x R_x \frac{i_x}{W(\varphi_{\rm DB})} = C_x R_x v_{\rm DB}. \tag{24}$$

Since the circuit depicted in Fig. 2(a) includes only one energy-storage component C_x, equations (17) and (22) actually present a first-order system. Note that, as shown in Fig. 2(b), although the voltage of node B can be directly measured from Fig. 1(a), while the voltage of equivalent node B′ can only be indirectly gained by calculation.

3.2. Design of memcapacitive circuit

By exchanging capacitor C_x and memristor emulator W, a new circuit with the memcapacitive property can be obtained. As shown in Fig. 3(a), $\varphi_{\rm DB}$ is proportional to the integration of the charge going through capacitor C_x, by defining that σ_x is the integral of charge q_x, we can obtain

$$C_x \varphi_{\rm DB} = \int_{-\infty}^{t} q_x {\rm d}\tau = \sigma_x. \tag{25}$$

In this case, the flux-controlled memristor can be converted into the σ_x-controlled memristor emulator. The memductance hence can be rewritten as

$$W(\sigma_x) = \frac{1}{R_1} \left(1 + \frac{\sigma_x}{10 R_6 C_1 C_x} \right). \tag{26}$$

Referring to the state equations induced in the preceding analysis, we can get

$$i_x = C_x \frac{{\rm d}v_{\rm DB}}{{\rm d}t}, \tag{27}$$

$$i_{x1} = W(\sigma_x) v_{\rm BD}, \quad i_{x2} = \frac{v_{\rm BE}}{R_x}. \tag{28}$$

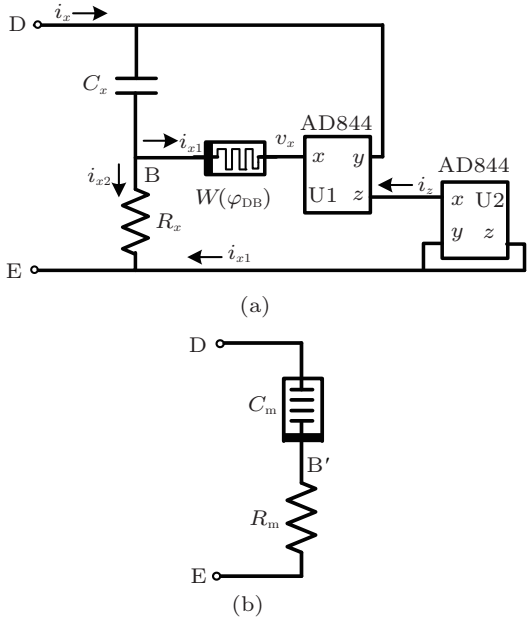


Fig. 3. Memcapacitive circuit (a) schematic diagram (b) equivalent circuit.

Combining Eqs. (27) and (28), the following set of state equations can be used to describe this memcapacitive circuit

$$v_{DE} = R_x \frac{dq_x}{dt} + \frac{q_x}{C_x}[R_x W(\sigma_x) + 1], \tag{29}$$

which demonstrates that the circuit presented in Fig. 3(a) is equivalent to a memcapacitor connected in serial with a linear resistor R_x, as redrawn in Fig. 3(b). The nonlinear controllable memcapacicitance and R_m hence can be identified as

$$C_m = \frac{C_x}{R_x W(\sigma_x) + 1}, \quad R_m = R_x. \tag{30}$$

It is worth noting that since there is no such node corresponding to the equivalent node B′ of Fig. 2(b), the terminal voltages of the equivalent memcapacitor and resistor R_m are also incapable of being measured directly.

3.3. Transferring interface circuit

Preceding analysis shows that different circuit properties can be interestingly obtained by changing the connecting position of memristor W and capacitor C_x. Here, referring to Figs. 2 and 3, a transferring circuit is designed as depicted in Fig. 4, of which three interface ports are defined by T_1 (1, 2), T_2 (3, 4), and T_3 (5, 6), respectively. Besides the two previously discussed meminductive and memcapacitive circuits, there are other four possible connection combinations of memristor W, capacitor C_x, and resistor R_x in terms of the three interface ports. The six possible combinations, and corresponding circuit properties are depicted in Table 1, of which two meminductive and four memcapacitive circuits can be obtained.

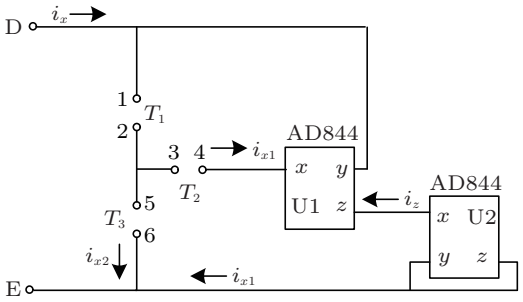


Fig. 4. Interface circuit.

Table 1. Circuit properties and equivalent parameters according to six combinations.

Connecting combinations			Circuit properties	Equivalent parameters	
T_1 (1,2)	T_2 (3,4)	T_3 (5,6)			
W	C_x	R_x	meminductive	$L_m = R_x C_x / W(\varphi_{DB})$,	$R_m = R_x + 1/W(\varphi_{DB})$
C_x	W	R_x	memcapacitive	$C_m = C_x/(R_x W(\varphi_{DB}) + 1)$,	$R_m = R_x$
W	R_x	C_x	memcapacitive	$C_m = R_x C_x/(R_x + 1/W(0.5\varphi_{DB}))$,	$R_m = 1/W(\varphi_{DB})$
R_x	W	C_x	memcapacitive	$C_m = C_x/(R_x W(0.5\varphi_{DB}) + 1)$,	$R_m = R_x$
C_x	R_x	W	memcapacitive	$C_m = R_x C_x/(R_x + 1/W(\varphi_{BE}))$,	$R_m = 1/W(\varphi_{BE})$
R_x	C_x	W	meminductive	$L_m = R_x C_x / W(0.5\varphi_{BE})$,	$R_m = R_x + 1/W(\varphi_{BE})$

4. Simulation analysis

SPICE is adopted in this section to verify the correctness and effectiveness of the newly designed memristive, meminductive, and memcapacitive circuit.

4.1. Improved memristor emulator

The memristor emulator is connected with an ac voltage source in parallel for the test. The circuit parameters are configured as: $R_1 = 33$ kΩ, $R_2 = R_3 = R_4 = R_5 = R_7 = 1000$ kΩ, $R_6 = 51$ kΩ, $C_1 = 100$ nF. First, the forcing voltage is configured to be a square waveform with amplitude $A_m = 2.8$ V and frequency $f = 40$ Hz. Since i is proportional to v_A with coefficient R_1, v_A can be used to characterize current i.[31] The Lissajous curve of v_{AB} versus v_A is drawn in Fig. 5(a) using a dashed line. This curve looks like fan blades and is similar to Fig. 8, as discussed in Ref. [13]. The most important character of a memristor is the frequency-dependence of the

pinched hysteresis loops.[34] As is also presented in Fig. 5(a), the pinched hysteresis loop of $f = 80$ Hz is obviously shrunk compared with the dashed curve of $f = 40$ Hz. This simulated result is evidently consistent with the preceding theoretical analysis of Eq. (7).

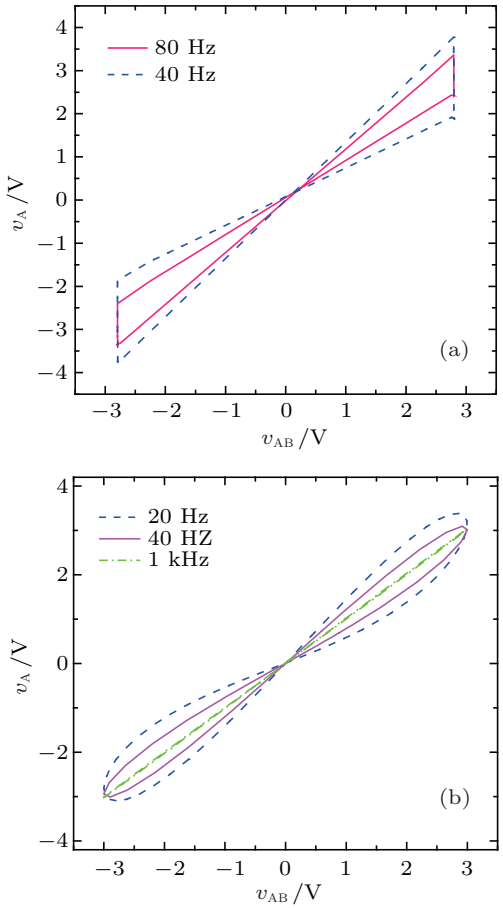


Fig. 5. (color online) Simulated results (a) v_A versus v_{AB} with the forcing voltage of the square wave, (b) v_A versus v_{AB} with the forcing voltage of the sinusoidal wave.

Then, a forcing voltage of $v_{AB} = 3\cos(2\pi ft)$ is used to further test this memristor emulator. Figure 5(b) displays the Lissajous curves of v_A versus v_{AB} at $f = 20$ Hz, $f = 40$ Hz, and $f = 1$ kHz, respectively, while the memductance in terms of v_{AB} is displayed in Fig. 6. Figure 5(b) clearly shows that the Lissajous curves in the voltage–current plane appear in a pinched hysteresis loop as an inclined "8". By comparing these three curves, as the frequency increases, the pinched hysteresis loop gradually degenerates to a straight line passing through the origin, of which the slope depends on the amplitude and shape of the excited voltage signal. In other words, at a very high frequency, there is not enough time for any kind of memristance change during a period of the control parameter, so that this emulator operates as a linear resistor. This simulated result is in good agreement with the theoretical analysis of Eq. (11).

Figure 6 demonstrates that for a given value of forcing voltage v_{AB}, there are two possible values of memductance, where the bigger value associates with the rising region of v_{AB} in the time domain. Note that, all the three curves are symmetric in terms of the coordinate point (0, 0.0303) on the voltage versus the memductance plane and the maximal and minimal values of the memductance both emerge at $v_{AB} = 0$ V; these simulation results show great agreement with the theoretical analysis. Based on Eq. (1) and the given system parameters, varying intervals of the emulator memductance can be calculated within one excitation voltage period, namely, (0.0161, 0.0445), (0.0232, 0.0374), and (0.0300, 0.0359) mS.

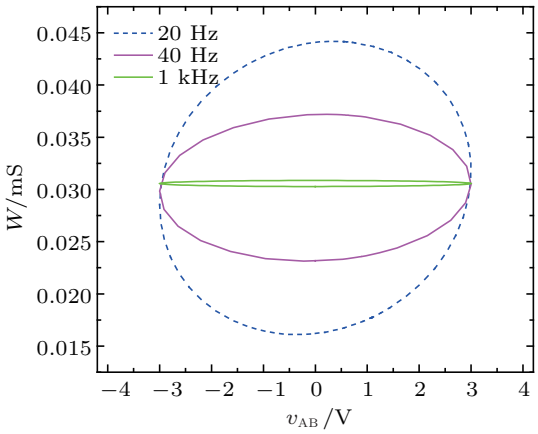


Fig. 6. (color online) Calculated curve of memductance.

4.2. Meminductive and memcapacitive emulators

From Eq. (24) we can clearly see that the flux of the equivalent meminductance in Fig. 2(b) is actually proportional to the voltage across the memristor, namely v_{DB}. By setting $R_x = 10$ kΩ, $C_x = 1$ μF, $v_{DE} = 4.56\sin(2\pi ft)$, this circuit is tested using SPICE and the curves of testing results are plotted in Fig. 7. As discussed in Ref. [32], i_x is proportional to v_D with coefficient R_1 and since flux φ_L is in proportion to v_{DB}, v_D and v_{DB} are collected instead here to represent i_x and φ_L, respectively. To probe the time domain behaviors of the equivalent meminductor, v_D, v_{DB}, and v_{DE} are measured at $f = 24.1$ Hz and the Lissajous curves at $f = 24.1$ Hz and $f = 11.6$ Hz are correspondingly drawn, as shown in Fig. 5. Figure 5(b) distinctly displays that the pinched hysteresis loop behaves also as an inclined number "8".

Equation (12) reveals that the current is zero whenever the flux is zero. Figure 5(b) also shows a pinched hysteretic loop exactly passing through the origin and there may be at most two values of the flux for a given current (using v_D instead). It has been discussed in Ref. [2] that the frequency-dependence of the pinched hysteresis loop is also an important property of the meminductor. This property can also be easily unfolded by comparing the two Lissajous curves given in Fig. 5(b). The area of each lobe of the pinched hysteresis loop shrinks as the frequency of the forcing signal increases. Actually, the relative decrements of current i_x and terminal voltage of memristor (v_{DB}), as shown in Fig. 7(b), indirectly reflect that the

impedance of the equivalent meminductor is increased by the higher forcing frequency. This characteristic is consistent with the regular resistive and inductive circuit.

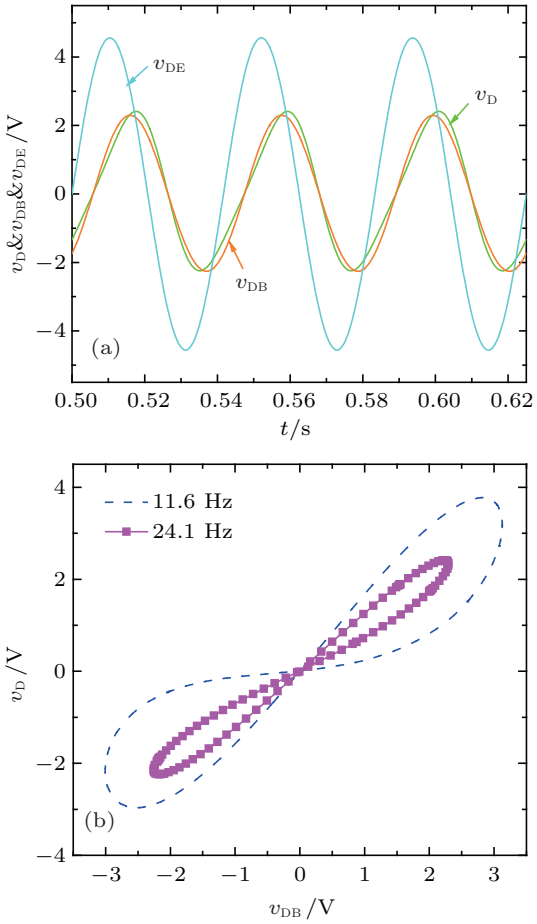


Fig. 7. (color online) Simulation results of the meminductive circuit (a) time domain waveforms of v_D, v_{DE}, and v_{DB}. (b) Lissajous curves.

From the equivalent circuit in Fig. 2(b), we can see that one linear resistor and one memristor are unavoidably connected in a series with the equivalent meminductor. Hence, there must be a phase difference between the terminal voltage and the internal current and the value of the phase difference can be adjusted by the forcing frequency and the resistor connected in the serial circuit. To show the phase difference, the time domain waveforms of terminal voltage v_{DB} and internal current (using v_D instead) are presented in Fig. 7(a). Evidently, the current lags behind the voltage and the phase difference confirms clearly that this proposed circuit possesses the meminductive property.

To test the memcapacitive behaviors, the forcing voltage, $v_{DE} = 3.78\sin(2\pi ft)$, is introduced to energize the circuit of Fig. 3(a). Although the voltage across memcapacitor v_{cm} is directly immeasurable, it can be calculated by $(v_{DE}–R_x i_x)$ based on simulation data. The simulation results in the time-domain are displayed in Fig. 8(a) as $f = 12.1$ Hz, from which it can be seen that forcing voltage v_{DE} is lagging behind current i_x but ahead of v_{cm} in terms of phase, and the phase difference between current i_x and v_{cm} is always $\pi/2$. These circuit characteristics clearly indicate that our newly proposed circuit has the resistive and nonlinear capacitive property. The waveform shapes of current i_x and voltage v_{cm} are noticeably nonstandard sinusoidal, which can partially reflect the nonlinearity of the σ_x controlled memcapacitance.

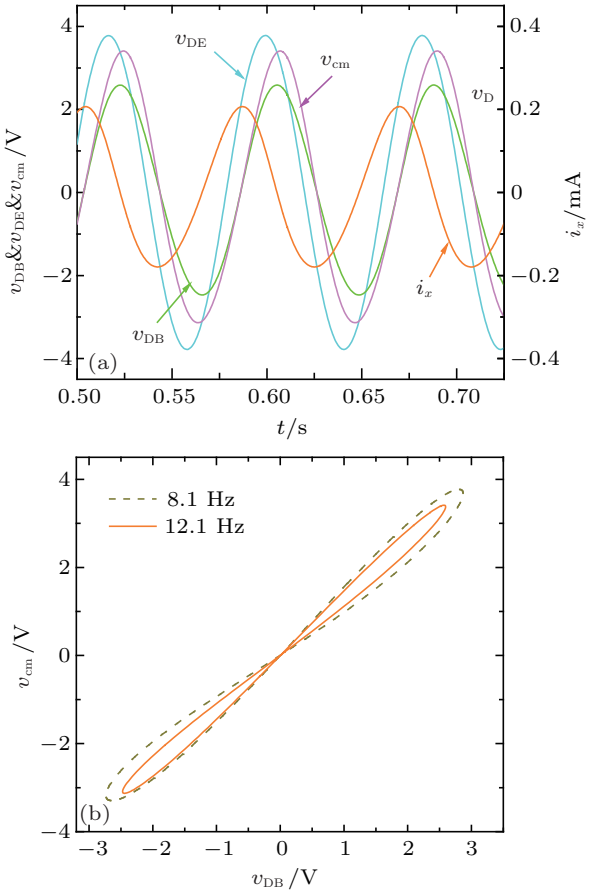


Fig. 8. (color online) Simulation results of the equivalent memcapacitive circuit (a) time domain waveforms of i_x, v_{DE}, v_{cm}, and v_{DB}. (b) Lissajous curves.

The Lissajous curves in the voltage–charge plane corresponding to different forcing frequencies, as revealed in Fig. 8(b), reflects that the memcapacitance is also nonlinear frequency dependent and the terminal voltage of the serial memcapacitor is reduced as the frequency increases, which also displays the inherent resistive and capacitive property of this circuit.

As a matter of fact, when the forcing frequency increases towards infinity, both the equivalent meminductor and memcapacitor will act as linear inductor and capacitor, respectively.

5. Experimental results

Previously, meminductive and memcapacitive circuits are achieved based on the floating memristive emulator. From this point of view, the performance of the memristive emulator can be reflected by the experimental quality of meminductive and

memcapacitive circuits. Therefore, for the sake of simplicity, only meminductive and memcapacitive circuits are put into experimental confirmation of correctness and practicability.

5.1. Fundamental characteristics

Since current i_x is hard to measure precisely, differing from the simulated curves in Fig. 8(a), the terminal voltage of the equivalent memcapacitor is calculated by

$$v_{\rm cm} = v_{\rm DE} - v_{\rm rx} = v_{\rm DE} - \left(v_{\rm BE} - \frac{R_x}{R_1} v_{\rm D}\right), \qquad (31)$$

where $v_{\rm rx}$ is the voltage across the equivalent serial resistor in Fig. 3(b).

Based on the same parameters as in the simulation, the pinched hysteresis loops for meminductive and memcapacitive circuits are presented in Fig. 9. These experimental pinched hysteresis loops, which are of high similarity with the simulation results, behave as inclined number "8" passing through the origin and also can be shrunk as the forcing frequency increases. Via zooming in experimental loops, it can be noticed that there are slight differences of amplitudes in comparison with the simulated loops of Figs. 7(b) and 8(b). These small differences are of the highest possibility caused by the inaccuracy of practical components. In order to compare the experimental results with simulated results more precisely, by taking Fig. 9(a) for demonstration, amplitude spectrums of variables $v_{\rm D}$ and $v_{\rm DB}$ are captured by taking advantage of FFT. In accordance with the forcing frequency of 24 Hz, the amplitudes of Fourier components at $f = 0$ Hz, $f = 24.1$ Hz, $f = 48.2$ Hz, $f = 72.3$ Hz, and $f = 96.4$ Hz are extracted and exhibited in Table 2, respectively. By comparing the component amplitudes in Table 2, it can be numerically revealed that the difference between the experiment and simulation results is extremely small. Additionally, the amplitude differences corresponding to forcing frequency $f = 11.6$ Hz, as listed in Table 3, are also quite small but comparatively greater than those shown in Table 2. This result demonstrates that these experimental errors can be lessened by means of increasing the forcing frequency. Since these errors are very small, it can be concluded that the experimental results are in good agreement with the theoretical analysis and simulation results.

Note that, both experimental and simulated variables of $v_{\rm D}$ and $v_{\rm DB}$ have a relative small DC component, which can be attributed to the non-ideality raised in experimental implementation.

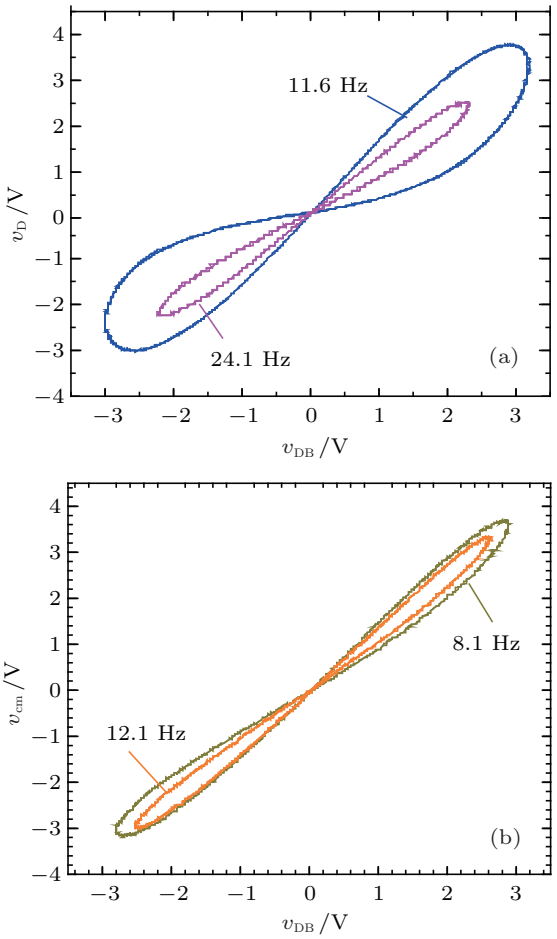


Fig. 9. (color online) Pinched hysteresis loops (a) meminductive loops (b) memcapacitive loops.

Table 2. Comparison of amplitude as forcing frequency $f = 24.1$ Hz.

f/Hz	$v_{\rm D}$/V			$v_{\rm DB}$/V		
	Experiment	Simulation	Error	Experiment	Simulation	Error
0	0.025	0.015	0.010	0.010	0.003	0.007
24.1	2.221	2.247	−0.026	2.255	2.276	−0.021
48.2	0.313	0.299	0.014	0.054	0.043	0.011
72.3	0.023	0.021	0.002	0.017	0.014	0.003
96.4	0.010	0.013	0.003	0.008	0.009	0.001

Table 3. Comparison of amplitude as forcing frequency $f = 11.6$ Hz.

f/Hz	$v_{\rm D}$/V			$v_{\rm DB}$/V		
	Experiment	Simulation	Error	Experiment	Simulation	Error
0	0.217	0.203	0.014	0.101	0.060	0.041
11.6	2.652	2.808	−0.156	2.934	3.094	−0.160
23.2	1.203	1.150	0.053	0.255	0.203	0.052
34.8	0.131	0.119	0.012	0.024	0.015	0.009
46.4	0.007	0.010	−0.003	0.001	0.001	0.000

5.2. Behaviors of meminductive circuit connected with capacitor

To test the dynamical characteristics of the meminductive circuit, here a canonical capacitor $C_{\rm r}$ is adopted for serial con-

nection with the meminductive circuit, which is denoted as the $R_{\rm m}L_{\rm m}C_{\rm r}$ circuit for simplicity, as shown in Fig. 10.

The set of state equations for describing this $R_{\rm m}L_{\rm m}C$ circuit can be expressed as

$$\begin{cases} \dfrac{{\rm d}q_{\rm xc}}{{\rm d}t} = \dfrac{W(\varphi_{\rm DB})}{C_x R_x}\left[\varphi_{\rm PE} - \varphi_{\rm PD} - q_{\rm xc}\left(R_x + \dfrac{1}{W(0.5\varphi_{\rm DB})}\right)\right], \\ \dfrac{{\rm d}\varphi_{\rm PD}}{{\rm d}t} = \dfrac{1}{C_{\rm r}} q_{\rm xc}, \\ \dfrac{{\rm d}\varphi_{\rm DB}}{{\rm d}t} = \dfrac{i_{\rm xc}}{W(\varphi_{\rm DB})}. \end{cases} \tag{32}$$

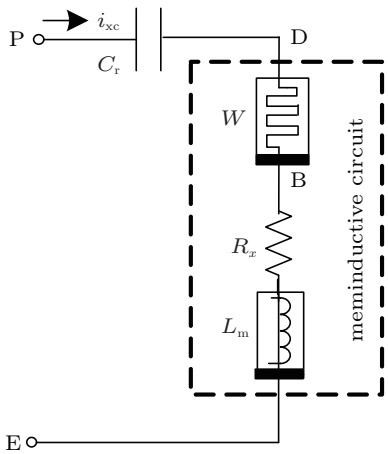


Fig. 10. Meminductive circuit connected with capacitor.

Despite the complexity of solving analytically, this second-order set of equations can be numerically computed. Here, we only focus on the dynamical characteristics of the meminductive circuit from the viewpoint of the experiment.

A sinusoidal voltage $v_{\rm PE} = 2.3\sin(2\pi ft)$ is then imposed on the terminals of this $R_{\rm m}L_{\rm m}C$ circuit for testing. Under the configuration of $f = 10.72$ Hz and $C_{\rm r} = 0.22$ μF, voltage waveforms of $v_{\rm PE}$, $v_{\rm PD}$, $v_{\rm D}$, and $v_{\rm DE}$ are painted by sampled data, as given in Fig. 11, of which $v_{\rm DE}$ is obtained by $v_{\rm PE}$–$v_{\rm PD}$ using computational function of the oscilloscope MATH button. Note that, based on the preceding analysis, the voltage of node D is proportional to the current $i_{\rm xc}$ going through this series circuit, therefore, $v_{\rm D}$ is employed here to display current $i_{\rm xc}$. Figure 11 shows that system current $i_{\rm xc}$ is ahead of terminal voltage $v_{\rm PE}$ with regard to phase, which reflects that, at $f = 10.72$ Hz, this serial system is apparently of a capacitive property. By rearranging the forcing frequency into $f = 20.42$ Hz, the corresponding experimental waveforms are depicted in Fig. 12. Interestingly, in this case, current $i_{\rm xc}$ lags behind terminal voltage $v_{\rm PE}$ with regard to phase, which indicates that this serial system can show dynamic behaviors of an inductive circuit under the forcing frequency of $f = 20.42$ Hz.

It worth noting that $v_{\rm DE}$ maintains the phase ahead of current $i_{\rm xc}$ even at different forcing frequencies, which means that the meminductive circuit, enclosed by the dashed-line frame, maintains the internal dynamical features of the inductive property. The nonstandard sinusoidal shapes of $v_{\rm D}$ and $v_{\rm DE}$ exactly illustrate the nonlinear characteristics of the meminductive circuit. These experimental results provide us with comprehensive confirmation that the newly proposed meminductive circuit can be used to construct a dynamic circuit with the meminductive characteristic.

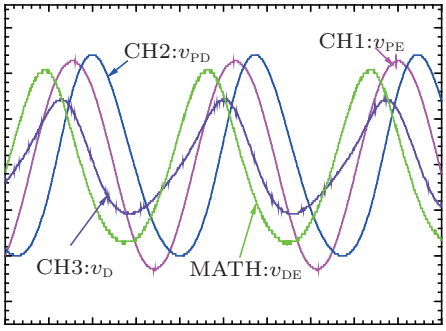


Fig. 11. (color online) Waveforms of $v_{\rm PE}$, $v_{\rm PD}$, $v_{\rm D}$, and $v_{\rm DE}$ at $f = 10.72$ Hz. The horizontal coordinate scale is 25 ms/division and the vertical coordinate scale is 1 V/division.

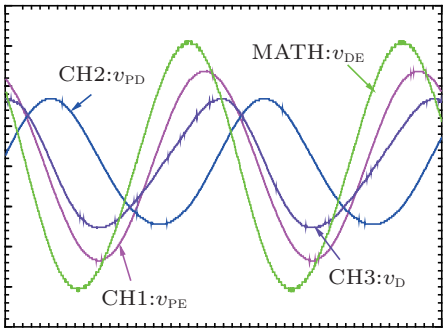


Fig. 12. (color online) Waveforms of $v_{\rm PE}$, $v_{\rm PD}$, $v_{\rm D}$, and $v_{\rm DE}$ at $f = 20.42$ Hz. The horizontal coordinate scale is 10 ms/division and the vertical coordinate scale is 1 V/division.

5.3. Behaviors of memcapacitive circuit as connected in Wien-bridge oscillator

The capacitive property of the memcapacitive circuit can also be confirmed by analyzing the phase relationships among waveforms of voltage and current in the time domain. By reconfiguring the forcing voltage as $v_{\rm DE} = 3.78\sin(24.2\pi t)$, the voltage waveforms of $v_{\rm DE}$, $v_{\rm DB}$, $v_{\rm cm}$, and $v_{\rm rx}$ are described in Fig. 13, where $v_{\rm rx}$ and $v_{\rm cm}$ are obtained by calculating Eq. (31) based on the sampled data. The $v_{\rm DB}$ is in proportion to the charge passing through the equivalent memcapacitor. The $v_{\rm DB}$ and $v_{\rm cm}$ are synchronously crossing the horizontal coordinate, which evidently accords with the simulated Lisssjous curves in Fig. 9(b). Since $v_{\rm rx}$ is proportional to the current going through terminals D and E, $v_{\rm rx}$ is adopted here to represent the current waveform and clearly, there is a phase-difference between forcing voltage $v_{\rm DE}$ and $v_{\rm rx}$, and circuit current i_x is leading ahead of forcing voltage $v_{\rm DE}$ with regard to phase. The phase difference among these waveforms reveals the resistive and capacitive property of this memcapacitive circuit.

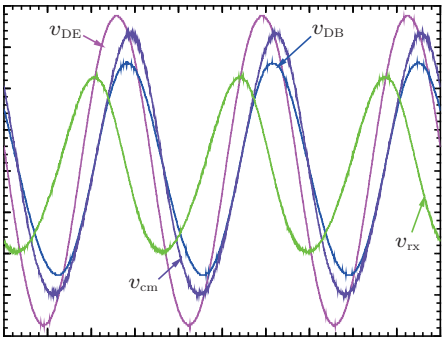


Fig. 13. (color online) Waveforms of v_{DE}, v_{DB}, v_{rx}, and v_{cm} at $f =$ 12.1 Hz. The horizontal coordinate scale is 25 ms/division and the vertical coordinate scale is 1 V/division.

In the next step, this memcapacitive circuit is applied into a typical self-excited oscillating circuit for the validation of practicability. The Wien-bridge oscillator has been widely used to produce sinusoidal voltage signals. As shown in Fig. 14, by connecting switch S to node g, a typical Wien-bridge oscillator can be achieved. An adjustable negative-feedback loop is constructed by R_8, R_9, and potentiometer R_p. The two diodes are introduced to stabilize the amplitude of the output voltage. In order to achieve optimal output u_o of sinusoidal voltage, the system parameters are usually configured as

$$C_2 = C_3, \quad R_{10} = R_{11}, \quad A_f = \frac{R_{p1} + R_9 + R_8 // R_D}{R_{p2}} \geq 2, \quad (33)$$

where A_f is the feedback gain of the op amp; R_D is the on-state resistance of the diode; node b is the non-inverting input terminal of the operational amplifier, and R_{p1} is the resistance between resistor R_9 and node b, while R_{p2} is the resistance between the ground and node b. The resonant frequency of this oscillator can be calculated by

$$f_{res} = \frac{1}{2\pi\sqrt{R_{10}R_{11}C_2C_3}} = \frac{1}{2\pi R_{10}C_2}. \quad (34)$$

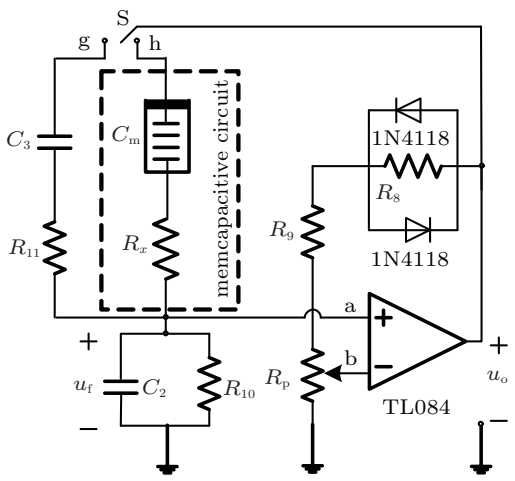


Fig. 14. Wien bridge oscillator.

The resonant frequency can be altered by changing the values of $R_{10}(R_{11})$ and $C_2(C_3)$. One attractive part of this oscillator is that changing frequency causes no influence on the amplitude and phase angle of the output sinusoidal waveform. It is worth noting that, there is another necessary condition for achieving self-excited oscillation of this oscillator, namely, the serial bridge arm must be of a capacitive circuit.

In order to test the dynamical property of the memcapacitive circuit in Fig. 3, by switching S to node h, the serial *RC* bridge arm is replaced by the memcapacitive circuit. In order to configure this oscillator properly, the resistance of R_x can be easily installed as the same value of R_{10}. In accordance with the preceding analysis, the memcapacitance of C_m is inconstant and defined by the amplitude and frequency of the voltage imposed on nodes h and a. Therefore, due to the influence from the nonlinear equivalent memcapacitor, the output waveform will be no longer standard sinusoidal, but include rich sub-harmonic components. However, as long as the value of feedback gain A_f is big enough, this circuit is capable of self-excited oscillating.

The parameters utilized for experimental validation are configured as: $R_8 = 6.8$ kΩ, $R_9 = 10$ kΩ, $R_{10} = 100$ kΩ, $C_2 = 1$ μF; R_P is a potentiometer with a maximum resistance of 10 kΩ, while R_{P1} and R_{P2} are initialized as 0 kΩ and 10 kΩ, respectively. The parameters employed here to implement the memcapacitive circuit are identical with those used for the preceding simulation analysis. Two diodes connected in the negative feedback loop are 1N4118 with a 0.45 V forward voltage drop. The quad operational amplifier chip TL084 is adopted here to achieve the self-oscillation, due to its advantages of low cost, low distortion, low noise, and low drift with wide bandwidth. By increasing the value of R_{P1} (decreasing R_{P2}), the output voltage will start to oscillate with a relative small amplitude and then evolve into a periodically alternating waveform. By adjusting R_{P2} into 185 Ω, the oscillating waveforms of output voltage u_o and u_f are obtained and shown in Fig. 15. The amplitude and period of these two oscillating waveforms are steady, but clearly in nonstandard sinusoidal shape. Similar to a typical Wien-bridge oscillator, u_o and u_f also simultaneously passes through zero. However, in each period, the negatively oscillating duration T_1 (13.6 ms), as marked in Fig. 15, is much less than the duration of positive voltage, T_2. The distortion of output voltage, as compared to the typical Wien-bridge oscillator, can be attributed to the nonlinearity and time-variant capacitance of the equivalent memcapacitor. The fundamental frequency of this oscillating voltage signal is measured at about 32.2 Hz, which discloses the equivalent average memcapacitance approximately equaling to 24.76 nF.

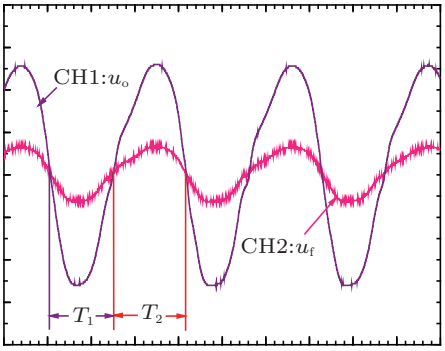


Fig. 15. (color online) Waveforms of u_o and u_f. The horizontal coordinate scale is 10 ms/division and the vertical coordinate scales are CH1: 5 V/division, CH2: 200 mV/division.

By continuously decreasing R_{P2}, amplitude saturation appears in the output voltage waveform, of which the maximal value is equivalent to 13.7 V. By taking $R_{P2} = 178\ \Omega$ for demonstration, the fundamental frequency of the output voltage is measured at 23.7 Hz, as drawn in Fig. 16, which also noticeably exhibits amplitude saturation. Due to the influence from the output voltage, the voltage across capacitor C_2, u_f, is forced into a flat top waveform as well, with the maximal amplitude equivalent to 142 mV. The time duration of positive voltage in each period is stabilized to 22 ms, while the time duration of negative voltage is 20 ms. This experimental result reveals that differing from a typical Wien-bridge oscillator, the output oscillating frequency can be decreased by the increment of R_{P1}. However, the ability of self-excited oscillation testifies that this new memcapacitive circuit possesses an explicit resistive and capacitive property and can be applied in ordinary electronic circuits without grounded restriction.

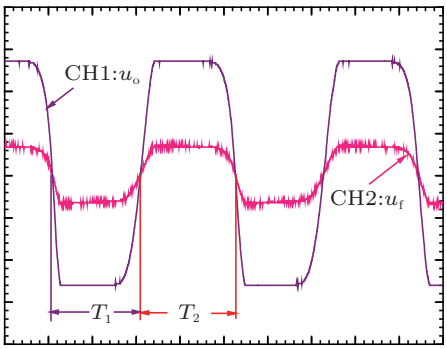


Fig. 16. (color online) Waveforms of u_o and u_f. The horizontal coordinate scale is 10 ms/division and the vertical coordinate scales are CH1: 5 V/division, CH2: 200 mV/division.

6. Conclusions

In this paper, an interface circuit which can transfer a memristor into nonlinear meminductive and memcapacitive circuits is presented. The unavoidable serial resistor and floating terminals explore the main specific features of these meminductive and memcapacitive circuits. The Pspice based simulation and experimental results manifest that these newly proposed meminductive and memcapacitive circuits are capable of providing reliable operational performance. The most attractive feature of these new meminductive and memcapacitive circuits are their convenient experimental implementations and potential practical applications in electronic circuits. All the circuit components used in this design are common purchasable devices and there is no requirement for any special or expensive components.

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