Positive gate-bias temperature instability of ZnO thin-film transistor*

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The positive gate-bias temperature instability of a radio frequency (RF) sputtered ZnO thin-film transistor (ZnO TFT) is investigated. Under positive gate-bias stress, the saturation drain current and OFF-state current decrease, and the threshold voltage shifts toward the positive direction. The stress amplitude and stress temperature are considered as important factors in threshold-voltage instability, and the time dependences of threshold voltage shift under various bias temperature stress conditions could be described by a stretched-exponential equation. Based on the analysis of hysteresis behaviors in current–voltage and capacitance–voltage characteristics before and after the gate-bias stress, it can be clarified that the threshold-voltage shift is predominantly attributed to the trapping of negative charge carriers in the defect states located at the gate–dielectric/channel interface.

Keywords: thin-film transistors (TFTs), zinc oxide, gate-bias instability, threshold-voltage shift

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1. Introduction

Thin-film transistors (TFTs) are extensively used as switching devices in active-matrix liquid-crystal display (AM-LCD) and active-matrix organic light-emitting diode (AM-OLED) display. Although hydrogenated amorphous Si TFTs are the current industry standard, for next-generation TFT technology, ZnO-based TFTs have attracted considerable attention due to their high carrier mobilities, low processing temperatures, and high transparencies compared with conventional amorphous silicon and polycrystalline silicon TFTs.[1–4]

It is well known that the electrical properties and stability of ZnO-based TFT are strongly influenced by the active layer, gate dielectric layer, and the interface between them.[5–7] In the past few years, a lot of research has been done to improve the performances of ZnO-based TFTs. For instance, many deposition methods have been used for the fabrication of high-quality oxide thin films, such as magnetron sputtering,[8] pulsed laser deposition,[9] and atomic layer deposition.[10] In addition, doped ZnO thin films such as InZnO,[11] InGaZnO,[12] MgZnO,[13] AlZnO,[14] and HfZnO[15] were used as the channel layer to optimize the electrical performance of ZnO-based TFT. However, in order to achieve manufacturability of ZnO-based TFT, it is crucial to solve the problems of the threshold-voltage ($V_{\rm th}$) shift of the transistor with time under prolonged bias. Any shift in the threshold voltage of the driving transistor under gate- and drain-bias stress conditions will cause a change in its output drain current, leading to circuit malfunction. Thus, device degradation due to bias-induced instability is a critical issue that must be solved. The bias-induced instabilities were universally observed in ZnO-based TFTs.[16–20] Several studies suggested that bias-induced instabilities could be suppressed by inserting a protective layer[18] or changing the gate dielectric.[19] A recent report pointed out that doping with metal elements with a high oxygen-binding energy in oxide semiconductor materials could improve the stability under long-term bias stresses.[15]

So far, several mechanisms have been proposed to explain the bias-induced instability, such as charge trapping or creation of extra trapping states in the gate dielectric or at the gate–dielectric/channel interface. However, these mechanisms were developed only from the output and transfer characteristics of ZnO-based TFTs.[20,21] There are not enough experimental results to support these deductions. Thus, in this work, the electrical instabilities of the ZnO TFT are investigated under positive gate-bias stress as a function of time and temperature. In particular, the mechanism of the threshold-voltage shift is further clarified based on the analysis of hysteresis behaviors in current–voltage and capacitance–voltage characteristics before and after the gate-bias stress.

2. Experimental details

Heavily-doped n-type silicon wafer acted as both the substrate material and gate electrode (G) for fabricating the device. Firstly, the silicon wafer was treated by the standard RCA method to achieve a clean surface. Secondly, the silicon

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was kept in hydrofluoric acid (with a concentration of 10%) for 30 s to remove the native oxide layer and then washed with deionized water. Then, SiO_2 film was grown by thermal dry oxidation at 1000 °C for 3.5 h as the gate-oxide layer. The SiO_2 film on the backside of the silicon substrate was removed to form the gate contact of the ZnO TFT device. Subsequently, ZnO film was deposited on the gate oxide layer using radio-frequency (RF) magnetron sputtering with sintered ZnO (99.999%, purity) serving as the target material. The sputtering process was carried out at a base pressure of 4×10^{-4} Pa, a substrate temperature of 400 °C, and an RF power of 60 W. The mixing gas ratio of O_2/Ar was 2/5 with a working pressure of 0.5 Pa. Finally, aluminum was vacuum-evaporated through a shadow mask to form the source/drain (S/D) electrodes of the transistor. The channel width (W) and length (L) of the device were 600 μm and 30 μm, respectively. The schematic structure of the ZnO TFT with a top S/D contact configuration after fabrication is shown in Fig. 1.

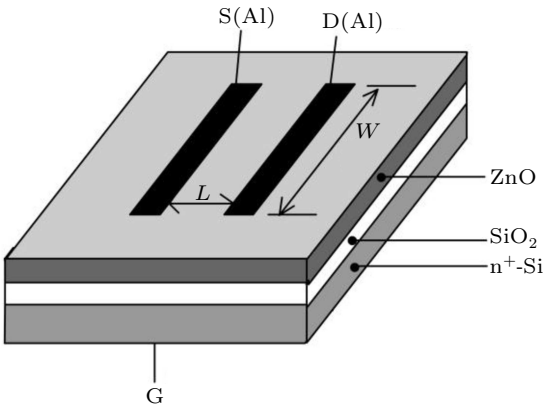


Fig. 1. Schematic structure of the ZnO TFT.

The thickness values of the SiO_2 film and ZnO film were measured to be 100 nm and 110 nm by spectroscopic reflectometer, respectively. The device characterization and stress measurements were carried out in the dark and air using an Agilent 4156C semiconductor parameter analyzer. Capacitance–voltage (C–V) measurements were performed by using a conventional LCR meter (Agilent 4284A). All electrical measurements were implemented on wafer using a probe station. To evaluate the effects of the positive gate-bias stress on the electrical characteristics of the device at different temperatures, the transfer characteristics needed to be measured periodically during the stress experiments, and fast measurements and a small number of measured points per transfer curve were required to minimize the influence of the measurement process on the overall bias stress experiment. Since the bias-stress instability was reversible after the removal of the bias for a relatively long time, to avoid the variations among different devices, all the bias-stress measurements were performed on the same device.

3. Results and discussion

3.1. Typical electrical properties

Typical output and transfer characteristics of a freshly prepared ZnO TFT are shown in Fig. 2. It can be seen from Fig. 2(a) that the ZnO TFT shows good saturation behavior. There is no current crowding at low source–drain biases, demonstrating the ohmic nature of the contact at the interface between the ZnO layer and Al S/D electrodes. The device shows an n-channel enhancement-mode behavior because a positive gate voltage is required to induce a conducting channel. From the transfer characteristics shown in Fig. 2(b), effective carrier mobility is calculated to be 2.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$; ON/OFF current ratio is determined to be 7×10^5; OFF-state source–drain leakage current is of the order of 10^{-10} A; and threshold voltage of 23.5 V is extracted from the slope of the linear region for a drain voltage of 30 V. In addition, a subthreshold slope is 2.5 $V \cdot dec^{-1}$, indicating a relatively high defect density in the interfacial region between the channel and dielectric layer.

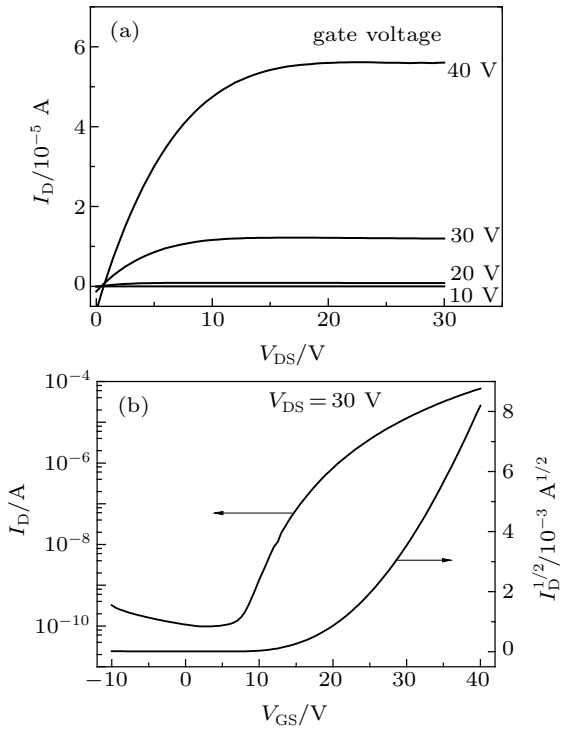


Fig. 2. Electrical properties of a typical ZnO TFT: (a) output characteristics for some different gate voltages; (b) transfer characteristics for a drain voltage of 30 V.

3.2. Positive gate-bias instability at room temperature

In order to test the electrical instability of the ZnO TFT under positive gate-bias stress, various positive gate biases were applied to the gate electrode with the source and drain connected to the ground ($V_{DS} = 0$ V). Figure 3 shows the evolutions of typical transfer characteristics of the ZnO TFT subjected to a positive gate-bias voltage of 30 V for different stress times at room temperature ($T = 25$ °C). It can be

observed that there is a parallel shift of the transfer curve toward the positive direction, and the shift is from rapid to slow with stress time increasing. The threshold-voltage shift ($\Delta V_{\rm th}$) after 6000 s under the gate-bias stressing is 8.0 V. The OFF-state current decreases slightly with stress time increasing because the trapped holes which are not emitted immediately after stressing may cause a reduction in effective defect state. On the other hand, the subthreshold swing (SS) and carrier mobility do not change after the transistor has undergone the gate-bias stressing, indicating that the creation of extra electron trapping states at the semiconductor/dielectric interface is not significant.

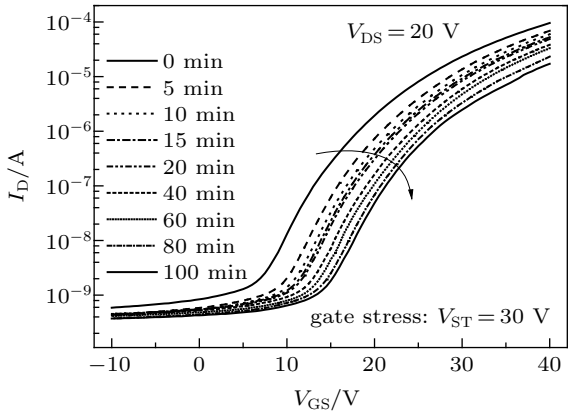


Fig. 3. Transfer characteristics of the ZnO TFT for variable stress times at stress voltage of $V_{\rm ST} = 30$ V and $V_{\rm DS} = 0$ V.

Figure 4 shows the time dependences of $\Delta V_{\rm th}$ under different positive gate-bias stresses at room temperature. The threshold voltage shifts rapidly and then is saturated quickly with the increase of stress time for various gate-bias stresses, and the higher the gate-bias stress, the larger will the $V_{\rm th}$ shift under the same stress time be. Previous studies reported that the time dependence of $\Delta V_{\rm th}$ for ZnO TFT under bias stress followed a logarithmic time-dependence model,[22] but our results show that the time dependence of $\Delta V_{\rm th}$ can be fitted well with a stretched-exponential equation for all stress conditions, which has been developed to model the $\Delta V_{\rm th}$ based on the charge trapping mechanism in a-Si TFT. The stretched-exponential equation for the time-dependent $\Delta V_{\rm th}$ is determined as[23]

$$\Delta V_{\rm th} = \Delta V_{\rm th0} \left\{ 1 - \exp[-(t/\tau)^{\beta}] \right\}, \qquad (1)$$

where $\Delta V_{\rm th0}$ is the $\Delta V_{\rm th}$ at infinite time, approximating the voltage drop across the insulator; t is the stress time; τ represents the characteristic trapping time of carriers; β is the stretched exponential constant. Figure 4 shows that the time dependences of $\Delta V_{\rm th}$ can be fitted with the stretched-exponential equation with a characteristic trapping time of 1×10^4 s and a stretched exponential constant of 0.45. Moreover, τ and β hardly depend on the bias stress amplitude, but $\Delta V_{\rm th0}$ shows a strong dependence on the bias stress. The fitting parameters are listed in Table 1. These results are consistent with those for InGaZnO TFT,[24] where the value of $\Delta V_{\rm th0}$ is mainly determined by the gate-stress amplitude and interface quality.

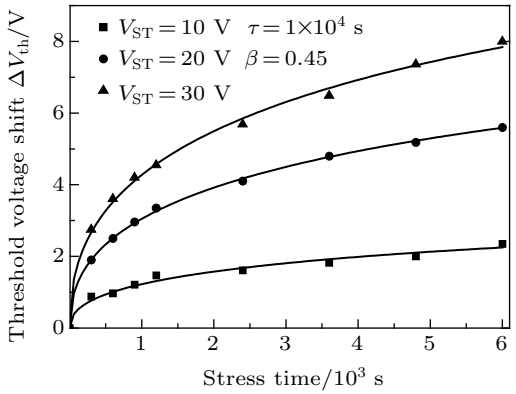


Fig. 4. Time dependences of threshold-voltage shift ($\Delta V_{\rm th}$) for different values of positive gate-bias stress $V_{\rm ST}$, the full lines are fitted curves using the stretched-exponential equation.

Table 1. Fitting parameters to different positive gate-bias stresses in the stretched-exponential model.

Gate-bias stress $V_{\rm ST}$/V	$\Delta V_{\rm th0}$/V	β	τ/s
10	4.1	0.45	1.0×10^4
20	10.2	0.45	1.0×10^4
30	14.3	0.45	1.0×10^4

In order to further clarify the mechanism of the instability, the hysteresis test of the transfer curve is conducted before and after stressing when a positive gate-bias stress of 30 V is applied to the ZnO TFT for 6000 s. The transfer curve is obtained by sweeping the gate voltage from negative to positive value (forward sweeping) and then in the reverse direction (reverse sweeping) under a fixed drain voltage of 20 V as shown in Fig. 5. The $V_{\rm th}$ shifts toward a more positive voltage in the return sweep of the hysteresis loop before and after stressing. The positive shift of $V_{\rm th}$ suggests that negative charge carriers are trapped at the channel/gate-oxide interface or injected into the dielectric from the channel.[25] However, the variation of $V_{\rm th}$ shift is negligible after stressing, indicating that the positive gate-bias stress does not cause new defect states at the interface between the channel and dielectric layer.

Normally, capacitance–voltage measurement is an intrinsically useful technique for investigating the charge phenomenon in TFT because measured capacitance varies with the trapped charges in the semiconductor bulk and at the insulator/semiconductor interface, as well as applied gate voltage.[26,27] To further investigate the effect of positive gate-bias stress on the charge state at the gate dielectric/ZnO interface in the ZnO TFT, figure 6 shows the C–V hysteresis curves of the ZnO TFT before and after stressing for different gate-bias stresses at a frequency of 500 kHz. It is obvious that the

distortions of the *C–V* curves are not obviously observed before and after stressing for different gate-bias stresses (hysteresis size and direction, and the slope from accumulation to depletion are unchanged), indicating again that the positive gate-bias stress does not induce new defect states at the interface between the channel and dielectric layer.

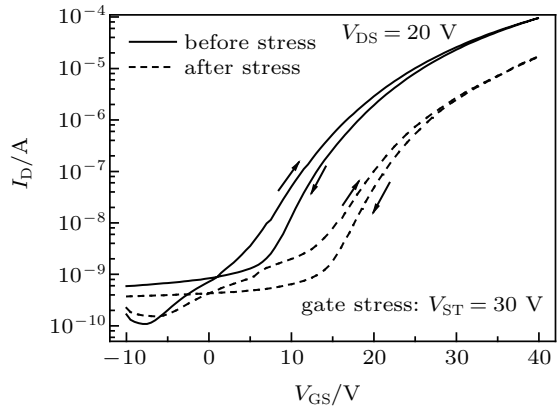


Fig. 5. Hysteresis loops of transfer curves before (solid line) and after (dashed line) stressing at a fixed drain voltage of 20 V when the positive gate-bias stress of 30 V has been applied to the ZnO TFT for 6000 s. The arrows indicate the sweep directions of the gate bias voltage.

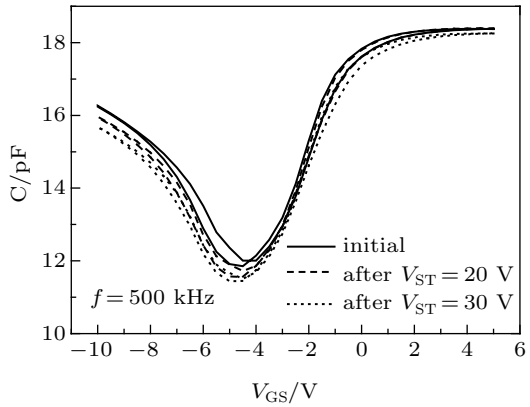


Fig. 6. *C–V* hysteresis curves of the ZnO TFT before and after stress under different gate bias stresses (V_{ST}).

3.3. Positive gate-bias instability at elevated temperatures

To further investigate the trapping dynamics, the gate-bias stress is exerted at several stress temperatures. Figure 7 illustrates the evolutions of the transfer characteristics when the ZnO TFT is subjected to a gate-bias stress of 20 V at various temperatures. It is evident that the threshold-voltage shift becomes larger with stress temperature rising for the same stress time, while the changes of subthreshold swing and carrier mobility are negligible for various stress temperatures. The time dependence of ΔV_{th} can also be well fitted by a stretched-exponential equation for all stress temperatures as shown in Fig. 8. The fitting parameters are listed in Table 2. The characteristic trapping time decreases with the increase of stress temperature, but the stretched exponential constant remains unchanged. In addition, several studies reported on humps appearing in the subthreshold region of the transfer curve for ZnO TFTs,[28] InGaZnO TFTs,[29] and MgZnO TFTs[30] under various circumstances. Humps have also been identified in as-fabricated devices without any bias stress. Nevertheless, in most cases, humps appear after the gate or drain bias stressing, and the hump phenomenon in the transfer curve becomes more severe as the gate-bias voltage (or stress temperature) increases. However, for our devices, the hump phenomenon does not appear after the positive gate-bias stressing at various stress temperatures. A possible reason is that high partial pressure of oxygen suppresses the formation of oxygen vacancies in the ZnO film in the sputtering process. In addition, better crystallization in the ZnO film fabricated at high substrate temperature (400 °C) could provide better resistance to metastable defect creation under a positive gate-bias stressing, even at high stress temperature.

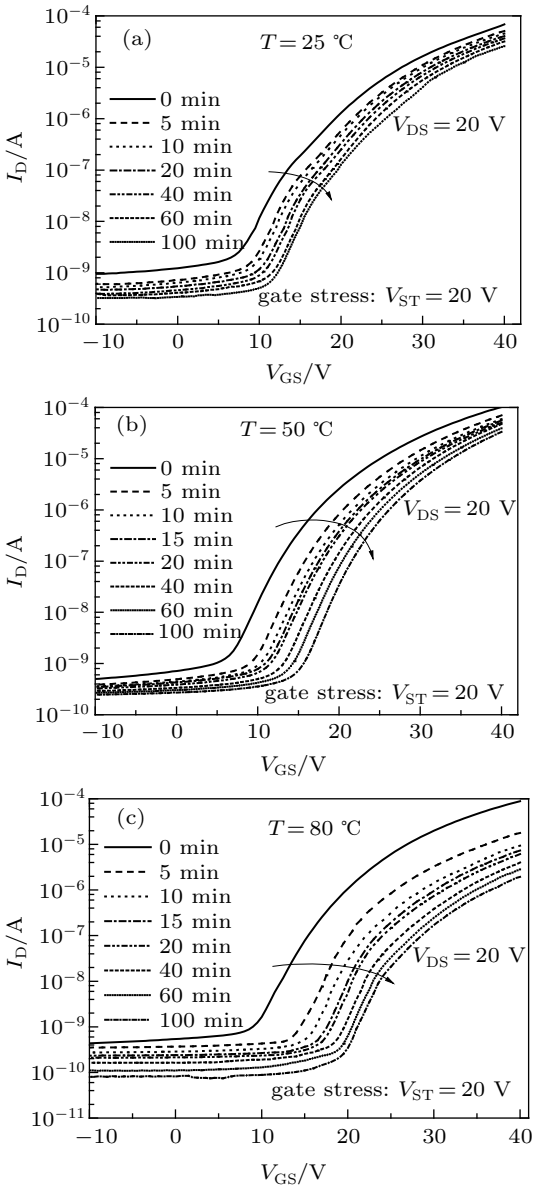


Fig. 7. Evolutions of transfer characteristics for the ZnO TFT under a positive gate-bias stress of 20 V at various temperatures.

Table 2. Fitting parameters to positive gate-bias stress of 20 V at different stress temperatures in the stretched-exponential model.

Stress temperature/°C	ΔV_{th0}/V	β	τ/s
25	10.5	0.44	1.12×10^4
50	16.3	0.44	9.22×10^3
80	18.6	0.44	4.31×10^3

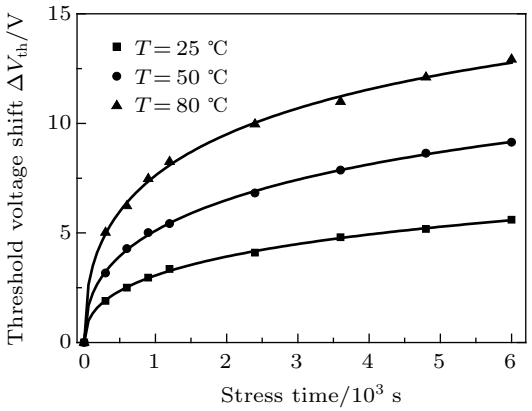


Fig. 8. Time dependences of threshold-voltage shift for a positive gate-bias stress of 20 V at different stress temperatures. The full lines are the fitted curves using the stretched-exponential equation.

Figure 9 shows the hysteresis curves of the transfer characteristics before and after stressing after a positive gate-bias stress of 20 V has been applied to the ZnO TFT for 6000 s at various stress temperatures. Similarly, the V_{th} shifts toward a more positive voltage in the return sweep of the hysteresis loop before and after stressing at various stress temperatures due to negative charge carriers trapped at the channel/gate-oxide interface or injected into the dielectric from the channel.[25] Before stressing, the size of the initial hysteresis voltage increases with the increasing of measurement temperature. This is due to the fact that carrier charges are easily trapped in the defect states during the forward sweeping at higher temperature, while the trapped carriers are not emitted immediately during the reverse sweeping, thus resulting in larger hysteresis at higher measurement temperature. It is noted that the hysteresis voltage does not become larger after stressing, but slightly smaller than before stressing, and this phenomenon is more obvious at higher stress temperature (Fig. 9(c)). This can be explained by the fact that trapped carriers in the defect states during stressing are not emitted immediately, thus resulting in a relative reduction of effective defect state.

Similarly, to analyze the influence of the positive gate-bias stress on charge state at the ZnO/SiO_2 interface under various stress temperatures, figure 10 shows the *C*–*V* hysteresis curves of the ZnO TFT before and after stressing at a gate bias of 20 V for different stress temperatures at a frequency of 500 kHz. It is obvious that distortions of the *C*–*V* curve are not obvious before and after stressing for different stress temperatures (hysteresis size and direction, and the slope from accumulation to depletion is unchanged), indicating that the positive gate-bias stress does not induce new defect states at the interface between the channel and dielectric layer for various stress temperatures. However, the stress temperature could speed up the process of carrier trapping during the positive gate-bias stress, thus causing a larger threshold-voltage shift at higher stress temperature for the same stress time. In addition, deep-level defects could trap the charge carriers more easily at higher stress temperature during the gate-bias stress, resulting in a larger shift of threshold voltage in the saturation region. Based on the above analyses of hysteresis behaviors in current–voltage and capacitance–voltage characteristics before and after stressing for various positive gate-bias stresses at different temperatures, it can be deduced that the threshold-voltage shifts under positive gate-bias stresses at various temperatures predominantly originate from the trapping of negative charge carriers in the defect states located at the gate dielectric/channel interface, and irrelative to the creation of extra trapping states.

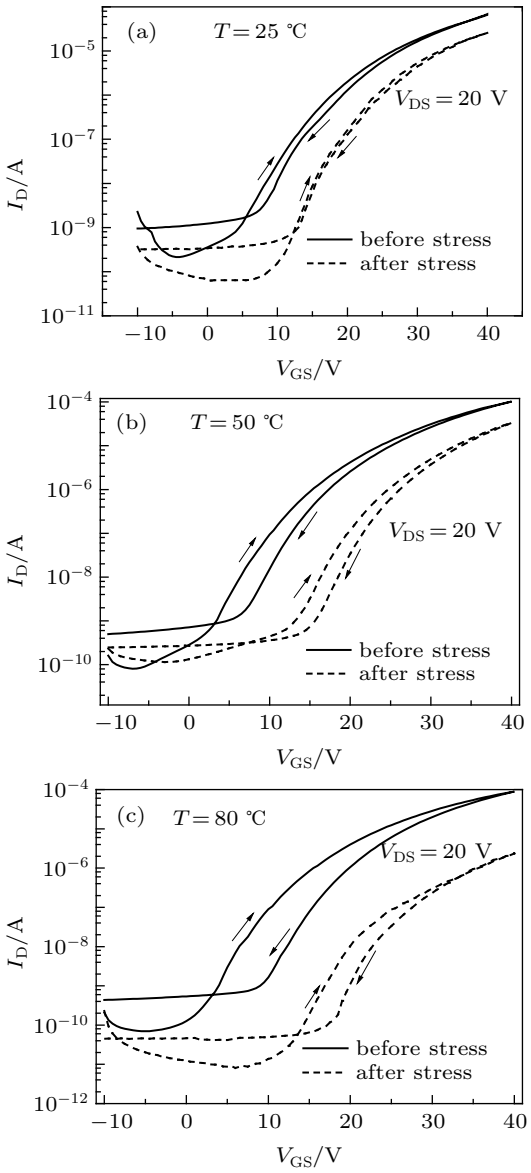


Fig. 9. Hysteresis loops of transfer curves before (solid line) and after (dashed line) stress at a fixed drain voltage of 20 V after the positive gate-bias stress of 20 V has been applied to the ZnO TFT for 6000 s at stress temperatures (a) 25 °C, (b) 50 °C, and (c) 80 °C. The arrows indicate the sweep directions of the gate bias voltage.

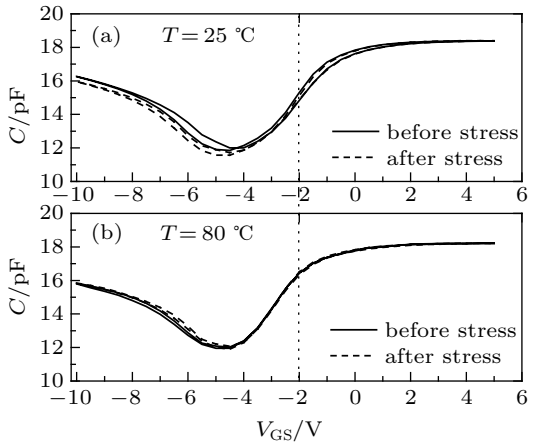


Fig. 10. *C–V* hysteresis curves of the ZnO TFT before and after a gate bias stress of 20 V for various temperatures.

4. Conclusions

The electrical instability of ZnO TFT under positive gate-bias stress is investigated as a function of stress time, stress voltage, and stress temperature. Experimental results show that the saturation drain current and OFF-state current of the TFT decrease, and its threshold voltage shifts toward the positive direction. The stress amplitude and stress temperature have an important effect on the threshold-voltage instability, and the time dependences of threshold-voltage shift for different stress voltages and stress temperatures could be described by a stretched-exponential equation. Based on the analysis of hysteresis behaviors in current–voltage and capacitance–voltage characteristics before and after the gate-bias stress, it can be clarified that the threshold-voltage shift is predominantly attributed to the trapping of negative charge carriers in the defect states located at the gate–dielectric/channel interface. The positive gate-bias stress does not generate new defect states at the interface between the channel and dielectric layer for various stress temperatures.

References

[1] Carcia P F, McLean R S, Reilly M H and Nunes G 2003 *Appl. Phys. Lett.* **82** 1117
[2] Chiang H Q, Wager J F, Hoffman R L, Jeong J and Keszler D A 2005 *Appl. Phys. Lett.* **86** 013503
[3] Li M, Zhang H Y, Guo C X, Xu J B and Fu X J 2009 *Chin. Phys. B* **18** 1594
[4] Lin C Y, Chien C W, Wu C H, Hsieh H H, Wu C C, Yeh Y H, Cheng C C, Lai C M and Yu M J 2012 *IEEE Trans. Electron Dev.* **59** 1701
[5] Ye Z and Wong M 2012 *IEEE Eelectron Dev. Lett.* **33** 549
[6] Lee J K and Choi D K 2012 *J. Nanosci. Nanotechnol.* **12** 5859
[7] Li S S, Liang C X, Wang X X, Li Y H, Song S M, Xin Y Q and Yang T L 2013 *Acta Phys. Sin.* **62** 077302 (in Chinese)
[8] Zhang L, Li J, Zhang X W, Jiang X Y and Zhang Z L 2009 *Appl. Phys. Lett.* **95** 072112
[9] Yoshida T, Tachibana T, Maemoto T, Sasa S and Inoue M 2010 *Appl. Phys. A* **101** 685
[10] Carcia P F, Mclean R S and Reilly M H 2006 *Appl. Phys. Lett.* **88** 123509
[11] Zhang G M, Guo L Q, Zhao K S and Yan Z H 2013 *Acta Phys. Sin.* **62** 137201 (in Chinese)
[12] Park J S, Jeong J K, Mo Y G, Kim H D and Kim C J 2008 *Appl. Phys. Lett.* **93** 033513
[13] Chiu H C, Wang H C, Lin C K, Chiu C W, Fu J S, Hsueh K P and Chien F T 2011 *Electrochem. Solid-state Lett.* **14** H385
[14] Lu A, Sun J, Jiang J and Wan Q 2010 *Appl. Phys. Lett.* **96** 043114
[15] Kim W S, Moon Y K, Kim K T, Shin S Y, Ahn B D, Lee J H and Park J W 2011 *Thin Solid Films* **519** 6849
[16] Suresh A and Muth J F 2008 *Appl. Phys. Lett.* **92** 033502
[17] Huang H Q, Sun J, Liu F J, Zhao J W, Hu Z F, Li Z J, Zhang X Q and Wang Y S 2011 *Chin. Phys. Lett.* **28** 128502
[18] Kim W S, Moon Y K, Kim K T, Shin S Y and Park J W 2011 *Thin Solid Films* **520** 578
[19] Cross R B M, De Souza M M, Deane S C and Young N D 2008 *IEEE Trans. Electron Dev.* **55** 1109
[20] Li M, Lan L F, Xu M, Wang L, Xu H, Luo D X, Zou J H, Tao H, Yao R H and Peng J B 2011 *J. Phys. D: Appl. Phys.* **44** 455102
[21] Yuh J T and Bae B S 2010 *Electron. Mater. Lett.* **6** 221
[22] Cross R B M and De Souza M M 2008 *IEEE Trans. Dev. Mater. Reliab.* **8** 277
[23] Libsch F R and Kanicki J 1993 *Appl. Phys. Lett.* **62** 1286
[24] Lee J M, Cho I T, Lee J H and Kwon H I 2008 *Appl. Phys. Lett.* **93** 093504
[25] Lee J S, Park J S, Pyo Y S, Lee D B, Kim E H, Stryakhilev D, Kim T W, Jin D U and Mo Y G 2009 *Appl. Phys. Lett.* **95** 123502
[26] Grecu S, Roggenbuck M, Opitz A and Brutting W 2006 *Org. Electron.* **7** 276
[27] Itoh E and Miyairi K 2006 *Thin Solid Films* **499** 95
[28] Park S H K, Hwang C S, Ryu M, Yang S, Byun C, Shin J, Lee J I, Lee K, Oh M S and Im S 2009 *Adv. Mater.* **21** 678
[29] Tsai C T, Chang T C, Chen S C, Lo I, Tsao S W, Hung M C, Chang J J, Wu C Y and Huang C Y 2010 *Appl. Phys. Lett.* **96** 242105
[30] Tsai Y S and Chen J Z 2012 *IEEE Trans. Electron Dev.* **59** 151