Partial-SOI high voltage laterally double-diffused MOS with a partially buried n^+-layer*

Hu Sheng-Dong(胡盛东)[a)b)†], Wu Xing-He(武星河)[a)], Zhu Zhi(朱 志)[a)], Jin Jing-Jing(金晶晶)[a)], and Chen Yin-Hui(陈银晖)[a)]

[a)] College of Communication Engineering, Chongqing University, Chongqing 400044, China
[b)] National Laboratory of Analogue Integrated Circuits, No. 24 Research Institute of China Electrics Technology Group Corporation, Chongqing 400044, China

(Received 12 October 2013; revised manuscript received 11 December 2013; published online 10 April 2014)

A novel partial silicon-on-insulator laterally double-diffused metal–oxide–semiconductor transistor (PSOI LDMOS) with a thin buried oxide layer is proposed in this paper. The key structure feature of the device is an n^+-layer, which is partially buried on the bottom interface of the top silicon layer (PBNL PSOI LDMOS). The undepleted interface n^+-layer leads to plenty of positive charges accumulated on the interface, which will modulate the distributions of the lateral and vertical electric fields for the device, resulting in a high breakdown voltage (BV). With the same thickness values of the top silicon layer (10 μm) and buried oxide layer (0.375 μm), the BV of the PBNL PSOI LDMOS increases to 432 V from 285 V of the conventional PSOI LDMOS, which is improved by 51.6%.

Keywords: silicon-on-insulator, breakdown voltage, interface charges, electric field

PACS: 71.10.–w, 73.20.–r, 73.40.Qv, 73.40.Ty **DOI:** 10.1088/1674-1056/23/6/067101

1. Introduction

Laterally double-diffused metal–oxide–semiconductor (LDMOS) based on silicon-on-insulator (SOI) technology has been widely studied and applied due to the advantages of SOI technology, such as superior isolation, high speed, and low loss.[1,2] SOI LDMOS suffers from a low vertical breakdown voltage (BV) and self-heating-effect (SHE). To solve the former problem, several new structures with the enhanced electric fields of buried oxide layers (BOX) have been proposed.[3–8] For the latter problem, a SOI substrate with a thin BOX or partial-SOI (PSOI) substrate is helpful.[9–13] The following PSOI LDMOSs with various structures were proposed: PSOI LDMOS with a combination of uniform and variation in lateral doping (UVLD) profiles for the drift region,[14] PSOI LDMOS characterized by oxide trenches on the top interface of the BOX,[15] PSOI LDMOS where the buried oxide layer consisted of two sections with a step shape,[16] PSOI structure consisting of two windows in the BOX with p-type doping silicon at the source side and n-type doping at the drain side,[17] PSOI LDMOS with dual p^- and n^- charge accumulation layers near the source and the drain,[18] PSOI LDMOS with low-*k* dielectric BOX,[19,20] and PSOI LDMOS with a near-triangular buried-oxide.[21] In 2012, Hu *et al.*[22] proposed a novel interface charge island PSOI structure, and improvement the BV of the device by the inversion holes located in the spacing of two n^+-regions. A new PSOI LDMOS with a buried n-type layer was introduced to achieve BV above 600 V in Ref. [23]. A new technique in which negative and positive charges were incorporated at the surface of the BOX was studied in Ref. [24]. High voltage power devices-based PSOI substrates are still gradually followed with interest.

In this paper, we study a thin BOX PSOI LDMOS with a partially buried n^+-layer (PBNL PSOI LDMOS). The modulated lateral electric fields in the drift and the vertical electric field in the p^- substrate lead to a high BV for the proposed PBNL PSOI LDMOS in comparison with the conventional PSOI LDMOS. The work mechanism of the device is discussed. The electrical characteristics of the device are analyzed in detail.

2. Structure and mechanism

The schematic cross-section view of the PBNL PSOI LDMOS is shown in Fig. 1(a). A partially buried n^+-layer is introduced on the bottom surface of the SOI layer, whose length (L_{n+}) is larger than that of the silicon window (L_w). When the device is on the off-state, the top and bottom surfaces of the partially buried n^+-layer will be partially depleted, and high concentration ionized donors are accumulated at the position. Moreover, the undepleted interface n^+-layer can prevent the extracting effect on the inversion holes of the lateral electric field in the drift region, and therefore, an inversion hole layer is formed at the interface beside the interface n^+-layer. The

*Project supported by the Natural Science Foundation of Chongqing Science and Technology Commission (CQ CSTC) (Grant No. cstcjjA40008), the Fundamental Research Funds for the Central Universities, China (Grant No. CDJZR12160003), the China Postdoctoral Science Foundation (Grant Nos. 2012M511906 and 2013T60835), and Chongqing University Postgraduates' Science and Innovation Fund, China (Grant No. CDJXS12161105).

†Corresponding author. E-mail: hushengdong@hotmail.com

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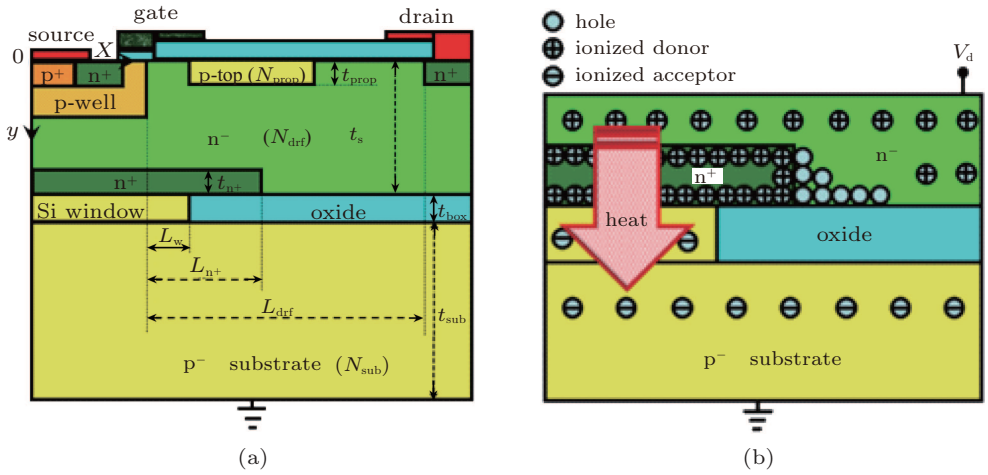


Fig. 1. (color online) Schematic cross section of the PBNL PSOI LDMOS (a) and the working mechanism (b).

charge distribution for the PBNL PSOI LDMOS is shown in Fig. 1(b). In horizontal orientation, the positive charges at the interface will modulate the distribution of the lateral electric field, and uniform equipotential contours can be obtained. In vertical orientation, an n^+p^- abrupt junction with a high reverse bias is formed on the silicon window (the high reverse bias results from the modulated electric field in the drift region), and therefore, the depleted region in the p^- substrate is thicker, leading to a higher voltage undertaken by the substrate. Just because of the modulation effect of the interface charges, a high BV can be achieved for the PBNL PSOI LDMOS compared with for the conventional PSOI LDMOS. A p-top layer on the top surface of the drift region is conducive to the depletion of the drift region and leads to an enhanced RESURF effect for the PBNL PSOI LDMOS. The silicon window offers a heat conduction path and reduces SHE while achieving a high BV. The structure parameters for the PBNL PSOI LDMOS are shown in Table 1.

Table 1. Device parameters used in the simulation.

Parameter	Value
Length of n^- drift region, L_{drf}/μm	25–45
Length of n^+ layer on the interface, L_{n+}/μm	0–30
Length of surface p-well at the source, L_S/μm	5
Length of surface n^+ silicon at the drain, L_D/μm	3
Length of silicon window under the source, L_w/μm	4–15
Thickness of top silicon layer, t_S/μm	10
Thickness of BOX layer, t_{box}/μm	0.375
Thickness of n^+ layer on the interface, t_{n+}/μm	0.5
Thickness of p-top layer, t_{ptop}/μm	1
Thickness of p^- substrate, t_{sub}/μm	20
Concentration of n^- drift region, N_{drf}/cm^{-3}	need to be optimized
Concentration of p-top layer, N_{p-top}/cm^{-3}	need to be optimized
Concentration of p^- substrate, N_{sub}/cm^{-3}	8×10^{14}
Concentration of interface n^+ layer, N_{n+}/cm^{-3}	1×10^{18}

3. Results and discussion

Figure 2 gives the distributions of the vertical electric field and potential for the PBNL PSOI LDMOS and the conventional PSOI LDMOS at breakdown. From Fig. 2(a), larger electric fields under the source both in the top silicon layer and the substrate are achieved for the PBNL PSOI LDMOS than for the conventional PSOI LDMOS because of the interface charges as shown in Fig. 1(b). The maximum electric field peaks of the PBNL PSOI LDMOS are 2.974×10^5 V/cm in the top silicon layer and 2.173×10^5 V/cm in the substrate layer, and those of the conventional PSOI LDMOS are only 1.929×10^5 V/cm and 0.895×10^5 V/cm, respectively. At the same time, the substrate depleted region is thicker for the PBNL PSOI LDMOS than for the conventional PSOI LDMOS. From Fig. 2(b), an optimal substrate depletion is similarly obtained for the PBNL PSOI LDMOS under the drain. Moreover, the accumulated holes shield the electric field on the bottom surface of the top silicon layer, thereby avoiding silicon layer premature breakdown at the position for the PBNL PSOI LDMOS. Figure 2(c) shows the vertical electric potentials at $x = 5.5$ μm and $x = 40.5$ μm. Voltage undertaken by the substrate for the PBNL PSOI LDMOS is much higher than for the conventional PSOI LDMOS, which is caused by the optimized vertical electric field. In addition, voltage undertaken by the BOX is very small, and therefore, the PBNL PSOI LDMOS is suitable for the device with a thin BOX.

Figure 3 shows the charge distributions while breakdown occurs for the PBNL PSOI LDMOS. Figure 3(a) exhibits the distributions of the electron concentration under the source. The gray pattern indicates the depleted n^+-layer at the interface. It can be seen that there is an obvious depletion in both surfaces of the n^+-layer under the source ($\leq L_w$), especially in the bottom surface because of the n^+p^- abrupt junction with a high reverse bias on the silicon window. The situations of

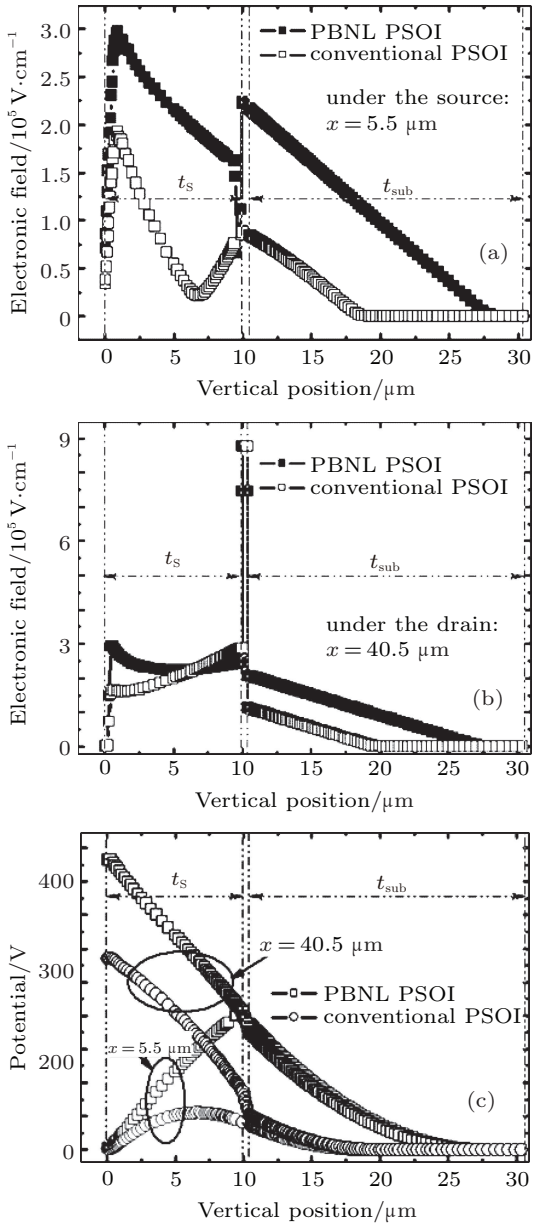


Fig. 2. Distributions of the vertical electric field and potential for the PBNL PSOI LDMOS ($L_{n+} = 15$ μm, $L_w = 10$ μm, $L_{drf} = 35$ μm) and the conventional PSOI LDMOS ($L_{n+} = 0$ μm, $L_w = 10$ μm, $L_{drf} = 35$ μm). (a) The vertical electric field under the source ($x = 5.5$ μm). (b) The vertical electric field under the drain ($x = 40.5$ μm). (c) The vertical potential.

different lateral positions have no significant distinction. Figure 3(b) shows the hole concentration along the bottom surface of the top silicon layer ($y = 9.999$ μm). It is clear that plenty of holes (10^{17} cm^{-3}) are accumulated at the interface beside the n$^+$-layer for the PBNL PSOI LDMOS. The introduced charges effectively modulate the distributions of lateral and vertical electric fields for the PBNL PSOI LDMOS.

Figure 4 shows the distributions of the lateral surface electric field for the PBNL PSOI LDMOS and the conventional PSOI LDMOS at breakdown. It can be seen that because of the modulation effect of the interface positive charges, a more uniform surface electric field is obtained for the PBNL PSOI LDMOS than for the conventional PSOI LDMOS, which means a higher lateral BV.

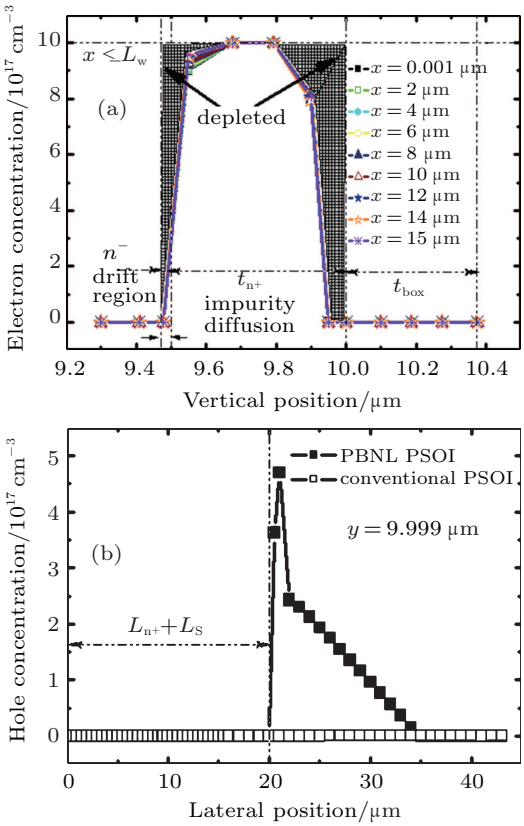


Fig. 3. (color online) Charge distributions at the breakdown for the PBNL PSOI LDMOS ($L_{n+} = 15$ μm, $L_w = 10$ μm, $L_{drf} = 35$ μm). (a) Electron concentration under the source ($x \leq L_w$). (b) Hole concentration along the bottom surface of the top silicon layer ($y = 9.999$ μm).

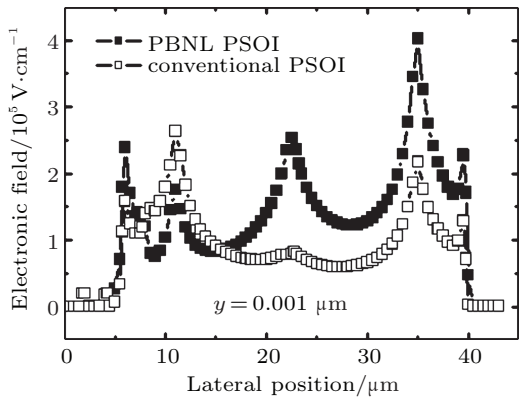


Fig. 4. Distributions of the lateral surface electric field ($y = 0.001$ μm) for the PBNL PSOI LDMOS ($L_{n+} = 15$ μm, $L_w = 10$ μm, $L_{drf} = 35$ μm) and the conventional PSOI LDMOS ($L_{n+} = 0$ μm, $L_w = 10$ μm, $L_{drf} = 35$ μm).

Figures 5(a) and 5(b) show the equipotential contour distributions at breakdown for the PBNL PSOI LDMOS and the conventional PSOI LDMOS, respectively. The equipotential contours in the drift region for the PBNL PSOI LDMOS almost averagely flow to the source side and the drain side. Firstly, this precludes the interface silicon electric field from crowding, which avoids a premature breakdown at the position just as the *P*-point of the conventional PSOI LDMOS as

shown in Fig. 5(b). Secondly, a higher potential is formed under the source for the PBNL PSOI LDMOS, which offers a higher reverse bias to the interface n^+p^- abrupt junction, and therefore, a thicker substrate depletion region (t_{dep}) is achieved for the PBNL PSOI LDMOS ($t_{dep} = 16.206$ μm) than for the conventional PBNL PSOI LDMOS ($t_{dep} = 8.526$ μm). Above all, compared with the BV of 285 V for the conventional PSOI LDMOS, the optimized electric field by the interface charges results in a high BV of 432 V for the PBNL PSOI LDMOS.

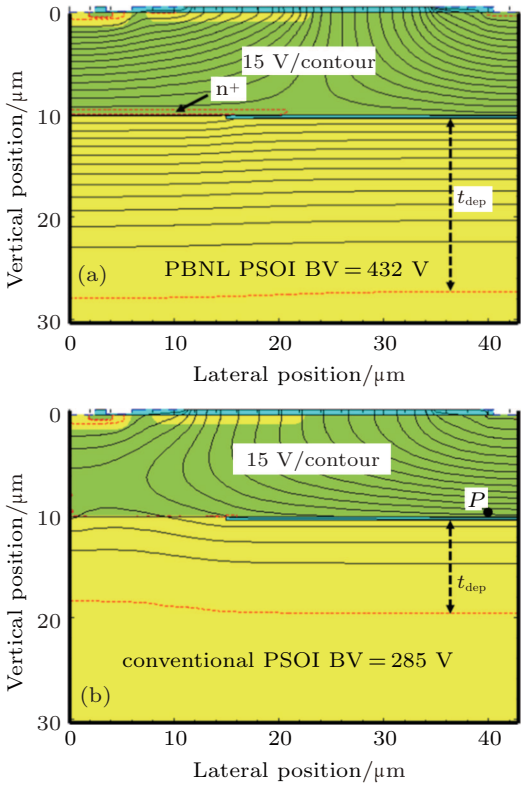


Fig. 5. (color online) Equipotential contour distributions at breakdown for the PBNL PSOI LDMOS ($L_{n+} = 15$ μm, $L_w = 10$ μm, $L_{drf} = 35$ μm) and the conventional PSOI LDMOS ($L_{n+} = 0$ μm, $L_w = 10$ μm, $L_{drf} = 35$ μm). (a) Equipotential contour distribution for the PBN PSOI LDMOS ($N_{drift} = 7 \times 10^{14}$ cm^{-3}, $N_{ptop} = 3.1 \times 10^{16}$ cm^{-3}). (b) Equipotential contour distribution for the PBN PSOI LDMOS ($N_{drift} = 1.4 \times 10^{15}$ cm^{-3}, $N_{ptop} = 3 \times 10^{15}$ cm^{-3}).

Figure 6 shows the influences of the structure parameters on device characteristics for the PBNL PSOI LDMOS. Figure 6(a) shows the BV against L_{n+} in the cases of L_{drf} from 25 μm–45 μm. The maximum BV (BV_{max}) increases with the increase of L_{drf} when L_{drf} is less than 35 μm, and when $L_{drf} \geq 35$ μm, values of BV_{max} are saturated at about 435 V because they are limited by the vertical BV. For a fixed L_{drf}, there is an optimized L_{n+} corresponding to the achieved BV_{max}, and the optimized L_{n+} is larger for a longer L_{drf}. Figure 6(b) shows the influences of L_w on BV and on-state temperature with $L_{drf} = 35$ μm and $L_{n+} = 15$ μm. It can be seen that L_w is unrelated to the BV for steady L_{drf} and L_{n+}, however, the maximum temperature (T_{max}) in the device on the on-state decreases with the increase of L_w because of a wider heat conduction path, which indicates that L_w should be chosen to be as wide as possible if only it satisfies the condition of $L_w \leq L_{n+}$.

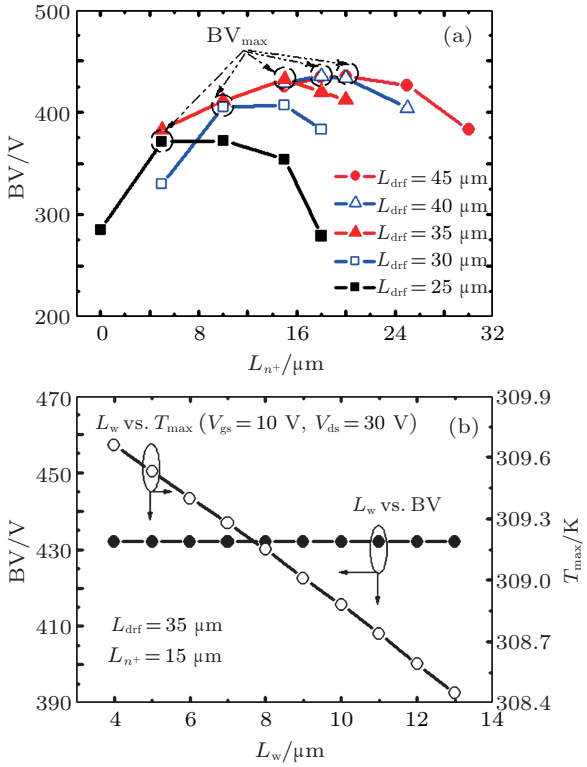


Fig. 6. (color online) (a) Dependences of BV on L_{n+} for different values of L_{drf}, and (b) dependences of BV and T_{max} on L_w at $L_{drf} = 35$ μm, $L_{n+} = 15$ μm. $V_{gs} = 10$ V, and $V_{ds} = 30$ V for T_{max} for PBNL PSOI LDMOS.

Figure 7 shows the major fabrication steps for the PBNL PSOI LDMOS based on the SIMOX (Separating by IMplanting OXide) technology: (a) O^{2+} implanting; (b) PSOI substrate after having been annealed at high temperature; (c) arsenic implanting to form an interface n^+ layer; (d) epitaxy to form the PBNL PSOI substrate. Only an additional process of n-type impurity implantation is needed to form PBNL PSOI LDMOS. Other fabrication processes are fully compatible with the conventional PSOI LDMOS.

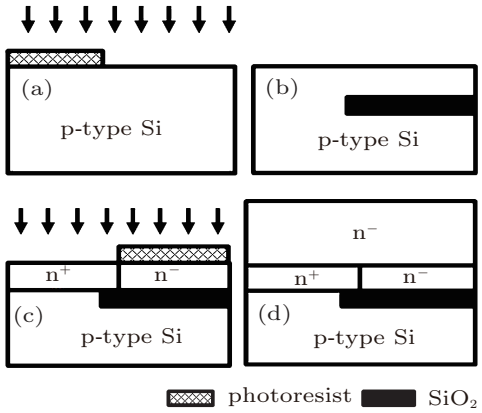


Fig. 7. Major fabrication steps for the PBNL PSOI LDMOS.

4. Conclusion

A novel high voltage PSOI LDMOS (PBNL PSOI LDMOS) is studied in this paper. With the same thickness values of top silicon layer and buried oxide layer, the BV of PBNL PSOI LDMOS is improved to 432 V from 285 V of the conventional PSOI LDMOS. The PBNL PSOI LDMOS could potentially be applied in high voltage power integrated circuits.

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