Retarded thermal oxidation of strained Si substrate*

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Strained Si is recognized as a necessary technology booster for modern integrated circuit technology. However, the thermal oxidation behaviors of strained Si substrates are not well understood yet despite their importance. In this study, we for the first time experimentally find that all types of strained Si substrates (uniaxial tensile, uniaxial compressive, biaxial tensile, and biaxial compressive) show smaller thermal oxidation rates than an unstrained Si substrate. The possible mechanisms for these retarded thermal oxidation rates in strained Si substrates are also discussed.

Keywords: strained Si, uniaxial and biaxial, tensile and compressive stresses, thermal oxidation rates

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1. Introduction

The Si complementary metal–oxide–semiconductor (CMOS) device is a key element of modern integrated circuit technology. The qualities of the Si/SiO_2 interface and the SiO_2 film are critical for obtaining a high performance Si CMOS device. Even in the era when high permittivity (k) gate dielectrics were used to replace SiO_2 as new gate oxides, a thin SiO_2 layer still existed in the gate stack and could significantly affect the performances and reliability behaviors of the metal–oxide–semiconductor (MOS) device. On the other hand, from the 90-nm technology node, strain engineering has become a standard process for enhancing the performances of the Si CMOS device.[1] This new process could at the same time change many aspects of the MOS device, such as device reliability properties, etc., besides enhancing the carrier mobility.[2–6]

It has been reported that the strained-$Si/Si_{1-x}Ge_x$/Si substrate might have a thinner gate oxide than the unstrained one.[7–10] However, there is no detailed information given in their reports. Meanwhile, only one type of stress, the biaxial tensile stress, is mentioned in Ref. [7] since the purpose of their work was not to study the thermal oxidation of strained Si substrate. Furthermore, CMOS technology has entered into the 20-nm node and the 14-nm technology is being developed by many chip manufacturers. In the sub-20-nm technology nodes, in order to introduce the stress into the device channel, the biaxial strained Si and silicon on insulator (SOI) substrate were considered.[11] As a result, the thermal oxidation of the strained Si substrate was inevitably involved during the device preparation process. However, so far, there have been few reports about the thermal oxidation process of strained Si.

In this work, we experimentally study the thermal oxidation rates of the Si substrates with different types of stresses, including biaxial tensile, biaxial compressive, uniaxial tensile, and uniaxial compressive ones. The results in our study show that all types of stresses could reduce the thermal oxidation rate of Si. This phenomenon might be due to the increase of the activation energy in the thermal oxidation process for the strained Si substrate.

2. Experimental details

All types of stresses were introduced into the thermal oxidation process with the mechanical bending method, as shown in Fig. 1. The four kinds of wafer bending equipment were home-made, which were made of pure Al_2O_3 ceramics, thereby guaranteeing that no contamination was introduced during the high temperature oxidation. Boron-doped p-type Si wafers with a (100) orientation and a resistivity range of 0.1 Ω·cm–1 Ω·cm were used in this study, which were processed with the standard Radio Corporation of America (RCA) cleaning procedure before being loaded into the furnace for thermal oxidation. The thermal oxidation processes were performed in a pure oxygen environment at 800 °C for different times, resulting in different SiO_2 thickness values. The strained substrates and unstrained one were loaded in the same furnace for processing in order to eliminate the process-induced error.

In order to investigate the electrical properties of

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SiO_2/strained-Si gate stacks, Au and Al were deposited by the thermal evaporation as the top electrode and back contact of the capacitors respectively. The high-resolution cross-sectional transmission electron microscopy (HR-TEM) images of stacked gate dielectrics were acquired using an FEI Tecnai^{TM} G2 F-20 microscope, and the protective layer on the gate dielectrics (SiO_2) for HR-TEM testing was platinum (Pt). The electrical properties including the capacitance–voltage (C–V) curves, of the fabricated metal–oxide–semiconductor (MOS) capacitors were measured using a precision *LCR* meter (Agilent 4284A).

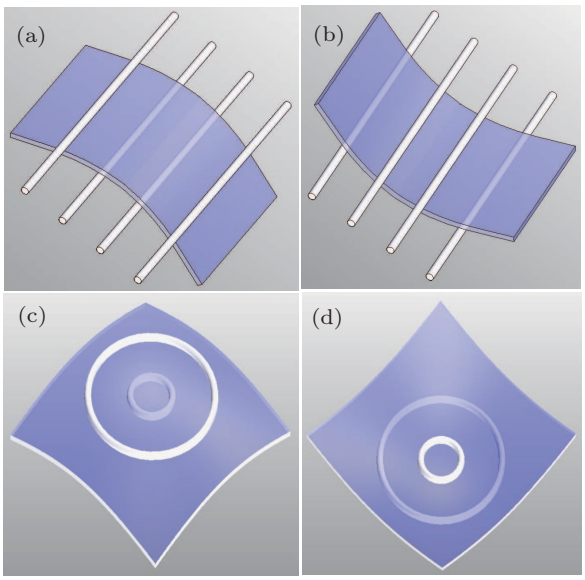


Fig. 1. (color online) Wafer bending systems made of Al_2O_3 ceramics used for testing the four types of stresses, i.e., (a) uniaxial tensile stress, (b) uniaxial compressive stress, (c) biaxial tensile stress, and (d) biaxial compressive stress.

3. Results and discussion

The SiO_2 thickness values are extracted from the capacitance–voltage (C–V) curves of the MOS capacitors. Figure 2 shows the C–V curves of the MOS capacitors with the gate oxides grown in the cases with and without the uniaxial stresses in the Si substrate.

It can be found that the capacitance value of the gate oxide (C_{ox}) increases when the unaxial stress (tensile or compressive) is applied to the Si substrate during the thermal oxidation. The oxide thickness values of all samples, which are extracted from the C–V curves in Figs. 2(a)–2(c), are summarized in Fig. 2(d). As shown in the figure, obviously, the uniaxially strained Si substrates have much smaller SiO_2 thickness values after the thermal oxidation or, in other words, have lower oxidation rates than the unstrained one. Moreover, in our study, the case of the biaxial stress (tensile or compressive) is also investigated. It is similar to the case of uniaxial stress that the biaxial stress can also reduce the oxidation rate of the Si substrate (Fig. 3).

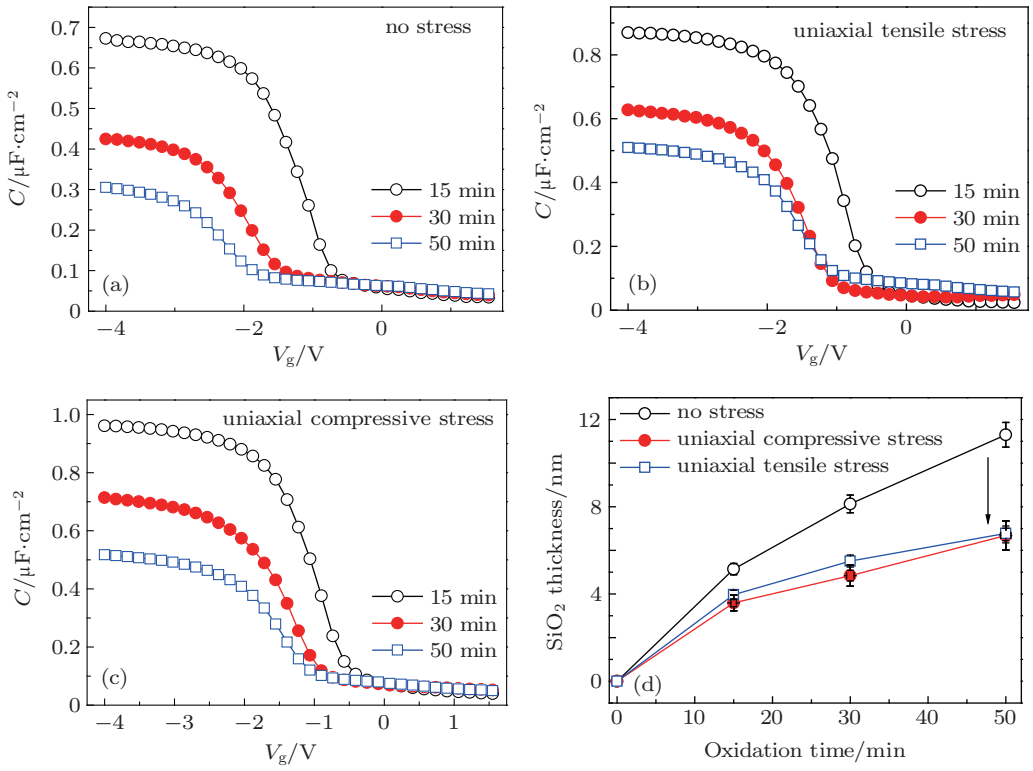


Fig. 2. (color online) C–V characteristics of the Si MOS capacitors, whose oxides are thermally grown without stress (a), with uniaxial tensile stress (b), and with uniaxial compressive stress (c) after different oxidation times; thickness values of SiO_2 grown under no stress, uniaxial tensile stress, and biaxial compress stress in the Si substrates versus oxidation time (d).

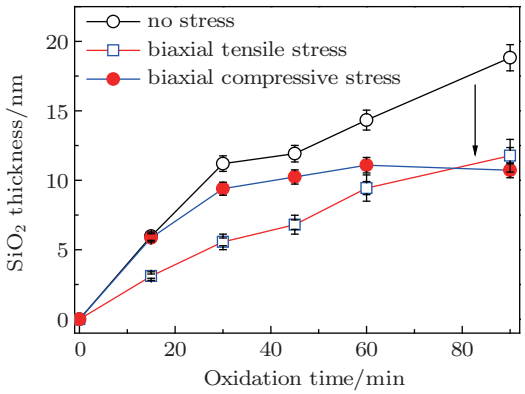


Fig. 3. (color online) Thickness values of SiO_2 samples grown under no stress, biaxial tensile stress, and biaxial compressive stress in the Si substrates versus oxidation time, respectively.

In order to more carefully confirm the above experimental results, some samples (biaxially tensile strained, biaxially compressive strained, and unstrained) were also examined with high-resolution transmission electron microscope (TEM) measurements to precisely determine the SiO_2 thickness values. It could be observed from the TEM images in Fig. 4 that the SiO_2 thickness does decrease when the Si substrate is strained during the thermal oxidation.

The possible reason for the above results might be as follows. The thermal oxidation rate, as is well known, is determined by the reaction rate at the interface and the diffusion rate of oxygen in SiO_2.[12] Thus, the influence of the stress in the Si substrate on the thermal oxidation rate could be discussed from these two points. The stress could make the bond length(s) of one (some) direction(s) increase and also cause the bond length(s) of one (some) direction(s) to decrease to keep the crystal volume unchanged as shown in Fig. 5.

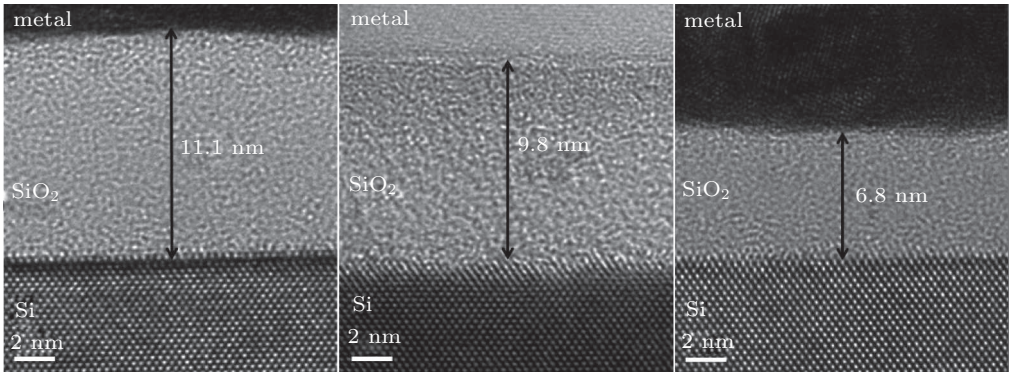


Fig. 4. (color online) TEM images of SiO_2/Si interface of Si MOS fabricated under (a) no stress, (b) biaxial compressive stress, and (c) biaxial tensile stress.

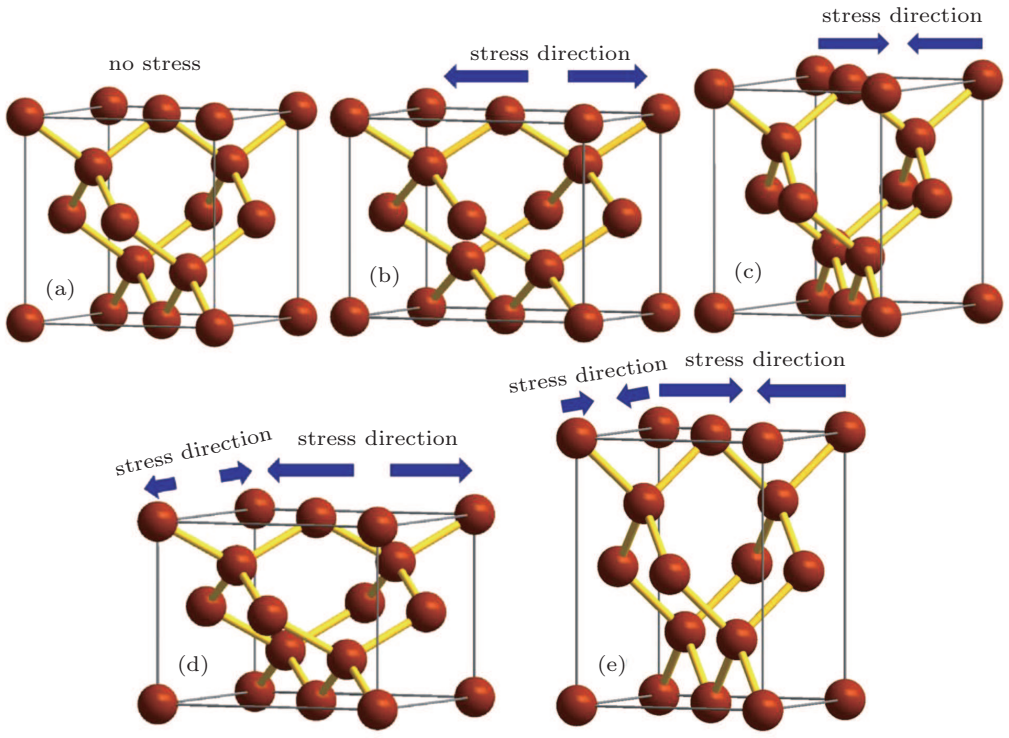


Fig. 5. (color online) Schematic diagrams of Si lattice structures under (a) no stress, (b) uniaxial tensile stress, (c) uniaxial compressive stress, (d) biaxial tensile stress, and (e) biaxial compressive stress.

The longer bond-length bonds each have a low energy barrier (activation energy) for the thermal oxidation, while the shorter bond-length bonds each will have a higher energy barrier to accomplish the thermal oxidation process (Fig. 6).

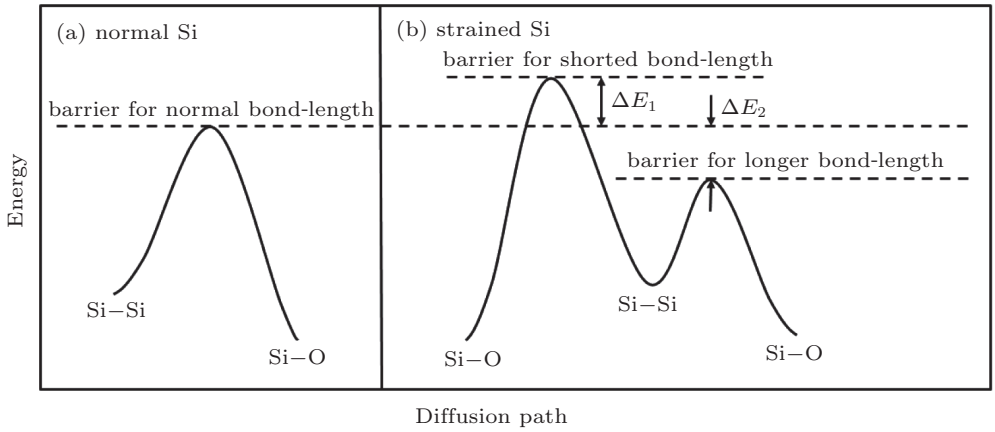


Fig. 6. Schematic diagram of activation energy barrier of oxidation for (a) normal silicon and (b) strained silicon with longer bond length and shorter bond length.

When considering the micro-thermal oxidation process, the final reaction rate should be determined by the higher activation energy, since the barrel is determined by the shortest slab.[13] Thus, all the types of strained Si substrates have lower thermal oxidation rates than the unstrained one. On the other hand, we find no direct evidence for the oxygen diffusion-constant difference in SiO_2 film between the strained and unstrained samples. The most possible cause, which leads to the oxygen-diffusion-constant difference, is the film density difference. Therefore, we measure the refractivities of SiO_2 films of strained and unstrained samples since the density of SiO_2 could be roughly equal to the square of the refractivity.[14] We do not observe any difference in SiO_2 refractivity between strained and unstrained samples (their data are not shown here). Therefore, it is very possible that the retarded thermal oxidation in strained Si substrate originates from the increase in the activation energy of the thermal oxidation process as discussed above. However, further study is still strongly needed for understanding the physical mechanism under this phenomenon.

4. Conclusions

We experimentally investigated the influences of different stresses (uniaxial tensile, uniaxial compressive, biaxial tensile, and biaxial compressive) in the Si substrate on the thermal oxidation rate. It is confirmed for the first time that all the four types of stresses can reduce the thermal oxidation rate of the Si substrate. The experimental results should be very important for further understanding the influences of the strain engineering on the behaviors of strained-Si and other semiconductor devices.

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