A voltage-controlled chaotic oscillator based on carbon nanotube field-effect transistor for low-power embedded systems*

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This paper presents a compact and low-power-based discrete-time chaotic oscillator based on a carbon nanotube field-effect transistor implemented using Wong and Deng's well-known model. The chaotic circuit is composed of a nonlinear circuit that creates an adjustable chaos map, two sample and hold cells for capture and delay functions, and a voltage shifter that works as a buffer and adjusts the output voltage for feedback. The operation of the chaotic circuit is verified with the SPICE software package, which uses a supply voltage of 0.9 V at a frequency of 20 kHz. The time series, frequency spectra, transitions in phase space, sensitivity with the initial condition diagrams, and bifurcation phenomena are presented. The main advantage of this circuit is that its chaotic signal can be generated while dissipating approximately 7.8 μW of power, making it suitable for embedded systems where many chaos-signal generators are required on a single chip.

Keywords: chaos generator, carbon nanotube field-effect transistor, bifurcation, random noise generator

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1. Introduction

Chaos theory and its applications have received considerable attention in various fields, and the hardware implementation of chaotic systems has been a subject of continuing research in recent years. Some efforts have been made by designing electronic discrete-time chaotic systems,[1–5] and such efforts are particularly important for the development of chaos communication and chaotic neural networks.[6,7] Most of these systems were implemented by using the metal oxide semiconductor (MOS) technology.

In the era of complementary metal oxide semiconductor (CMOS) technology, the well-known problems and limitations due to the scaling of the conventional CMOS technology make it unsuitable for low-power and low-voltage applications in the near future. This has led researchers to exploit novel nanotechnologies. One of the most promising and feasible nanotechnologies is the carbon nanotube field-effect transistor (CNFET) technology. Some of the advantages of CNFETs are that they are faster, have lower power consumption, exhibit higher performance, and simplify the process of mass fabrication of the transistors as compared with current MOSFET-based designs.[8] In this paper, we focus on the concept of building a chaotic circuit based on the CNFET instead of the traditional CMOS to realize a compact, effective, and low-power chaotic system. The excellent electronic properties of CNFETs make them more smoothing for applications in the future, particularly for high-performance and low-power embedded systems. The operation of the chaotic circuit is verified with the SPICE program to show its performance.

2. Carbon nanotube field-effect transistor for chaotic oscillator

For this research, an accurate CNFET device model with a more complete circuit-compatible structure, which incorporates typical device circuit non-idealities, is necessary to evaluate the potential performance of the CNFET. Some device models of CNFETs have been reported; however, most of them suffer from some drawbacks, wherein, for example, several effects are ignored, idealized[9–11] or require intensive calculations for a result that is inaccurate and difficult to implement in a SPICE program.[9,10] In contrast, Deng and Wong's model takes care of most of the drawbacks of the previous models, specifically by including practical device effects for non-idealities to maintain compatibility with both large (digital) and small (analog) signals.[12,13] As a result, Deng and Wong's model is chosen to implement our design in Cadence with the HSPICE-D simulator and to evaluate the CNFET performance before using it for a chaotic circuit design.

Figure 1 shows the structure and the characteristic curve of the CNFET, while Table 1 shows the key parameters of the CNFET model, with their values and brief descriptions.

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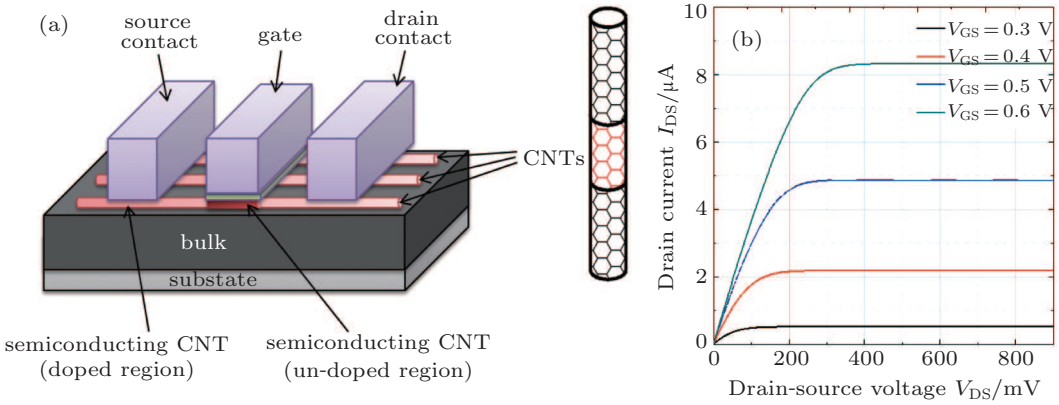


Fig. 1. (color online) Structure and *I*–*V* curves of an n-type carbon nanotube transistor.

Table 1. CNFET model key parameters.

Parameter	Description	Value
Fixed parameters		
C_{sub}	coupling capacitance between the channel region and the substrate	40 pF/m
T_{ox}	thickness of high-k top gate dielectric material	4 nm
K_{gate}	dielectric constant of high-k top gate dielectric material	16
L_{dd}	length of doped CNT drain-side extension region	32 nm
L_{ss}	length of doped CNT source-side extension region	32 nm
L_{geff}	mean free path in the intrinsic CNT channel	100 nm
L_{ch}	length of the channel	32 nm
Variable parameter		
Tubes	number of carbon nanotubes per device	

As shown in Fig. 1, the CNFET has a structure similar to the MOSFET, except that the channel material, as would be found in a conventional MOSFET, is replaced by carbon nanotubes, the resulting *I*–*V* characteristics of the CNFET are similar to those of the MOSFET. The results obtained from the simulation by using Deng and Wong's model show that a better *I*–*V* characteristic for the CNFET is obtained owing to the higher mobility in between the channel, as compared with the *I*–*V* characteristic for the MOSFET. Because of the low on currents and a low threshold voltage, the CNTFET is appropriate for ultra-low-power embedded systems, and this is the rationale for choosing the device to build a chaotic oscillator in this paper.

3. Design of voltage-controlled chaotic oscillator

Generally, a discrete-time chaotic oscillator can generate a chaotic series by means of an iterative application of a suitably chosen, nonlinear function as follows:

$$x(t+1) = f(x(t)), \tag{1}$$

where x is a state variable, and $f(x)$ is a one-dimensional chaos map of the system. The map can be implemented by using an integrated circuit to generate an approximate map, typically, the tent map, the logistic map, or other well-known nonlinear maps. In order to implement Eq. (1), in addition to a nonlinear circuit, a discrete-time chaotic oscillator needs both storage cells and a buffer cell, as depicted in Fig. 2.

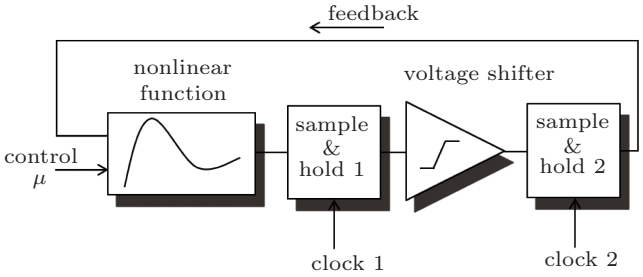


Fig. 2. Block diagram of the chaotic oscillator using CNT transistors.

From Figs. 2 and 3, the difference equation (1) can be represented as

$$x(t+1) = g \cdot f(x(t-1), \mu), \tag{2}$$

where μ is a variable control factor, and f and g are the functions of the nonlinear and the voltage shifter cells, respectively. The proposed circuit in this study consists of only seven CNFETs and two capacitors and is divided into four cells: a nonlinear function block (NFB) cell that is formed by three CNFETs with negative differential resistances to feature the chaos map, two sample and hold (S/H) cells that are used as memory and delay elements for feedback to the nonlinear circuit, and a voltage shifter block (VSB) cell that works as a buffer and adjusts the output of the NFB cell. Figure 3 shows the schematic diagram of the chaos-based CNFET circuit.

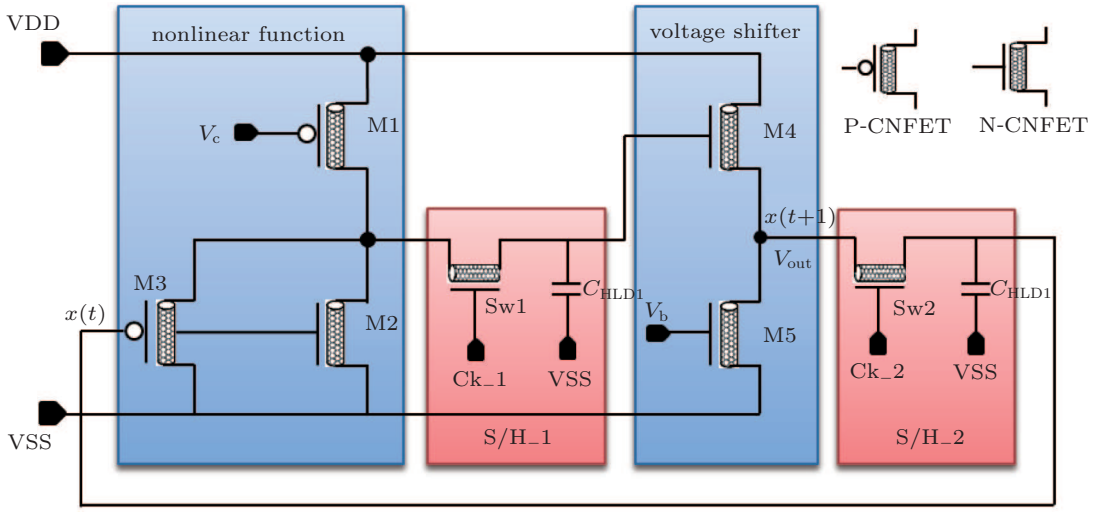


Fig. 3. (color online) Carbon nanotube transistor based chaotic oscillator.

The core cell of the proposed circuit is the chaos map, and its transfer curves are shown in Fig. 4(a), it is used to implement the nonlinear function $f(\cdot)$. Figures 4(b) and 5 show the VSB and its transfer curve and the S/H circuit, which are driven by two non-overlapping phases (Φ_A and Φ_B), respectively.

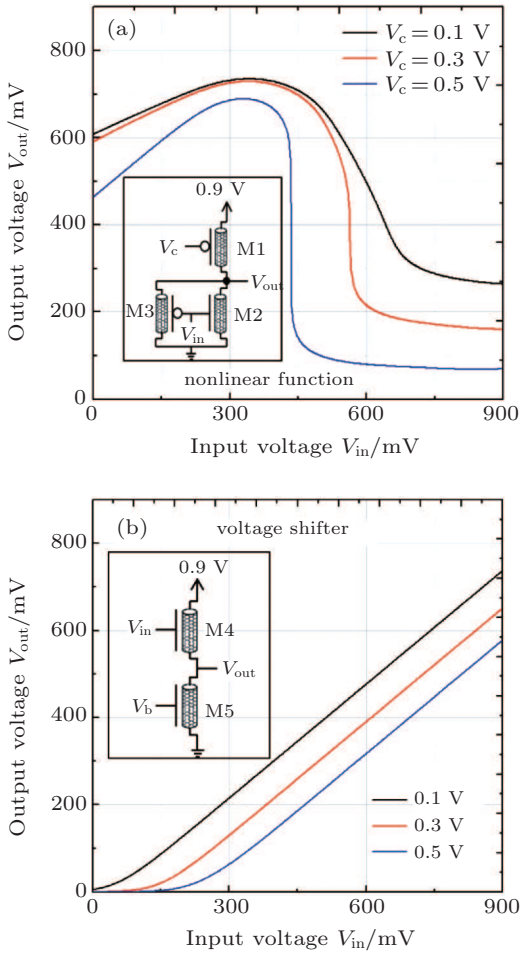


Fig. 4. (color online) Transfer curves of (a) nonlinear function and (b) voltage shifter.

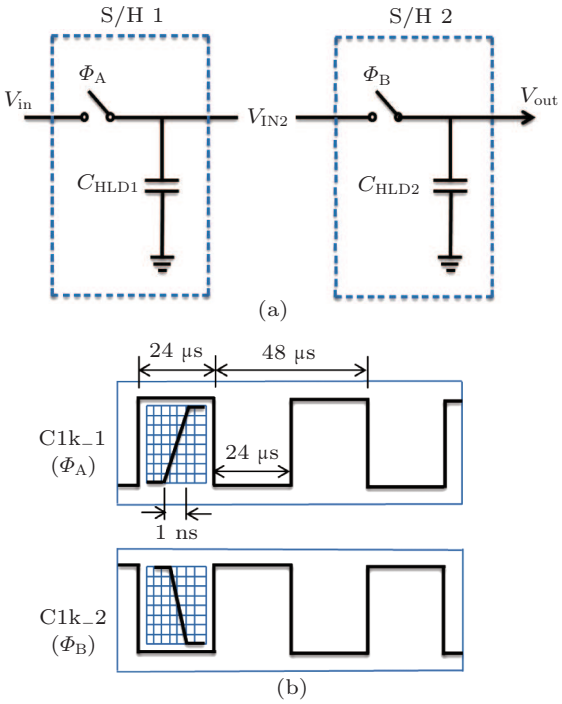


Fig. 5. (color online) (a) S/H block and (b) two non-overlapping clock sources.

In designing a chaotic circuit, the key problem is the design of a nonlinear function depending on the system parameters which are used to control the nonlinear function, so that they have an effect on the output chaotic sequence. An NF cell based on three CNFETs is used to create an easily adjustable chaos map. Figure 4(a) shows the transfer curves that are controlled by changing the control voltage V_c. The value of V_c determines whether the circuit can be used for generating chaotic or periodic signals. In an NF cell, the currents that flow through M1 are the sum of the currents from M2 and M3. If the input voltage is less than the threshold voltage of transistor M2, M2 will be switched off. Transistor M3 is placed in a voltage control block configuration, with transistor M1 as a load, producing the positive slope of the transfer curve

shown in Fig. 4(a). As the input voltage is increased beyond the threshold voltage of transistor M2, M2 enters the saturation region and begins to sink current, forming an inverter with M1 as a load. The system thus moves away from the transfer curve peak if the input voltage continues to increase. The output voltage will then decrease so that M3 turns off. Finally, M2 will enter the triode region.

Two N-CNFET types (M4 and M5) are connected in series to construct a voltage shifter, as shown in Fig. 4(b). The voltage shifter works as a buffer and adjusts the output voltage to the feedback signal. M5 is biased at a fixed voltage of V_b ($V_b < V_T = 200$ mV) for operation in the triode region to play the role of a resistance load, while M4 works as a source flower so that the drain current of M4 is transformed to the output voltage by the active load M5, as follows from Ohm's law ($V = I \times R$). Figure 4(b) shows the transfer curves of this block.

The variation in the critical parameters, however, can fade out the chaotic operation of the system so that the output behaves as a simple, periodic signal. The obtained transfer functions are $f(\cdot)$ and "like-linear" function $g(\cdot)$, which relates V_{in} and V_{out} with its sensitivity to the given parameters V_c and V_b. In particular, Fig. 4(a) shows the effect due to the variation in V_c, while the effect of V_b is shown in Fig. 4(b).

Additionally, two S/H blocks are used to generate a discrete-time series. It is important to appropriately choose these clocks to ensure that overlapping does not occur. The circuit is controlled by two phase-complementary clock signals, as shown in Fig. 5(b). At each time step, only one capacitor is connected to the input of the nonlinear function block, while the other is connected to the output.

The simple operation of the proposed circuit is as follows. When ϕ_A is active, the output of the NFB cell is sampled on C1. In the following time step (i.e., when ϕ_B is active), the sampled voltage is captured on the output of the VSB (or the input of the NFB cell) for feedback according to Eq. (2) to generate a sequence of output signals. The computation will iterate one time per cycle so that a discrete dynamic system is generated by continuous cycles to implement the iterated map.

4. Simulation results

The CNFET-based chaotic oscillator was simulated using a compact SPICE model, which was proposed in Deng and Wong's reports[12,13] in the HSPICE-D circuit simulator. The simulation was performed at room temperature at a supply voltage of 0.9 V using 20 kHz frequency clocks, and the value of V_b was fixed at 100 mV. It should be noted that the capacitors of the S/H cells (C_{HLD1} and C_{HLD2}) must be chosen to ensure the complete settling value of the outputs, which depends on the power consumption of the system so that the outputs reach equilibrium for a proper operation. The design was optimized in terms of the number of tubes of each transistor to generate a chaos map in Fig. 5(a). These values are shown in Table 2.

Table 2. Circuit specifications of the chaotic oscillator.

Circuit element	Value	Circuit element	Value
M1	1 tube	M5	1 tube
M2	2 tube	Sw1	1 tube
M3	1 tube	Sw2	1 tube
M4	4 tube	C1, C2	50 fF

To verify the behavior of the chaotic oscillator, V_c was varied in the range of 0–0.9 V. The value of V_c determines the kind of signal that can be generated at the output of the chaotic circuit. Figure 6(a) shows the simulated time series with the chaotic output signal for $V_c = 400$ mV (Fig. 7(a)); a periodic signal for $V_c = 600$ mV is shown in Fig. 7(b). Figures 7 and 8 present the frequency spectra and the transitions in the phase state according to the time series shown in Figs. 6(a) and 6(b), respectively.

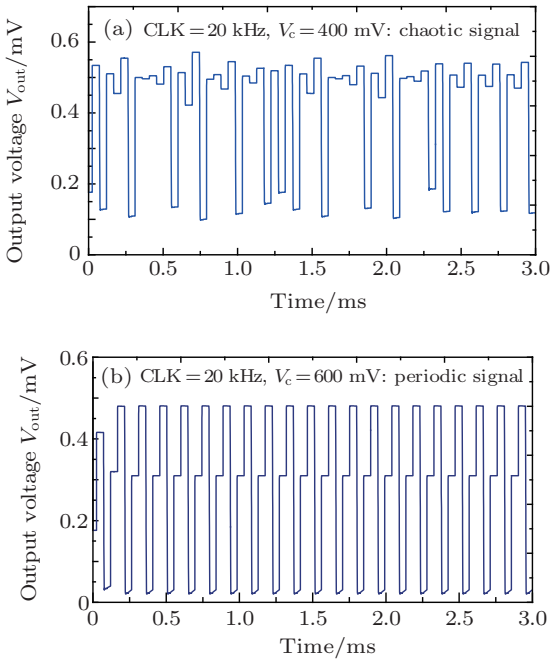


Fig. 6. (color online) Time series of the chaotic oscillator: (a) chaotic signal, (b) periodic signal.

The frequency spectrum provides an answer to the question of how much of the signal is at a frequency to determine the chaotic signal. The frequency spectrum was examined by applying the fast Fourier transform (FFT) technique to the corresponding time series. Figure 7(a) shows the broadband components to verify that the signal shown in Fig. 6(a) is a chaotic signal, while Fig. 7(b) shows the peaks and the relative low background noise for the periodic signal in Fig. 6(b). The plots in Figs. 8(a) and 8(b) exhibit the transitions in the phase state of the time series shown in Figs. 6(a) and 6(b), showing an enormously complex behavior for the chaos signal and a simple behavior for the periodic signal.

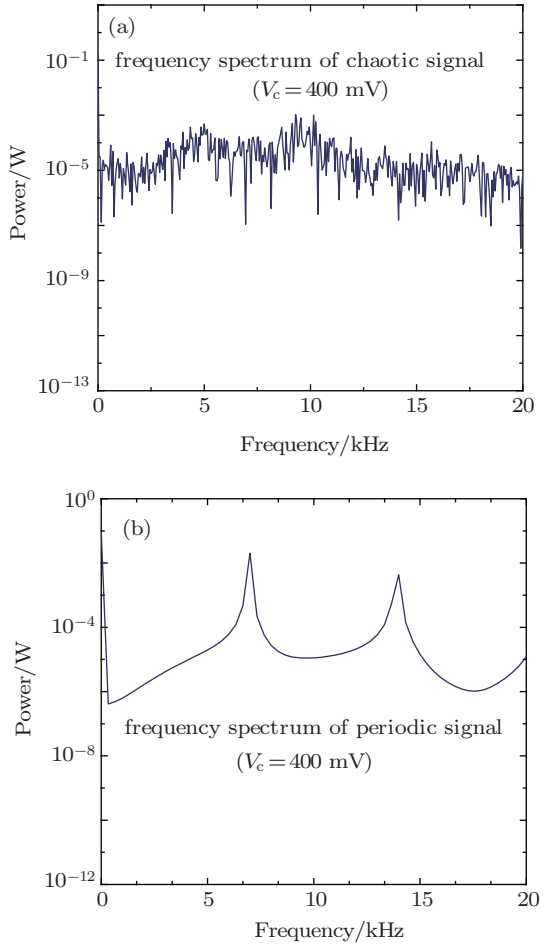


Fig. 7. (color online) Frequency spectra: (a) chaotic signal, (b) periodic signal.

Furthermore, to verity that the signal appearing on the output is a chaotic signal, it was verified that is is sensitive to the initial conditions: an important property of chaos. Figures 9(a) and 9(b) show the sensitivity with the initial conditions, while Fig. 10 illustrates the bifurcation of the proposed chaotic circuit.

Small differences in the initial conditions yield widely diverging outcomes if the system is chaotic, while the system settles down if the output voltage is periodic. In Fig. 9(a), different initial conditions of V_c diverge the output rapidly, while it settles down when the initial conditions are different with a periodic signal in Fig. 9(b). These simulation results demonstrate very clearly the existence of chaos in the proposed circuit.

Finally, the examination of the bifurcation of the chaotic circuit is an important measure to study the characteristics of dynamic chaos and to confirm the existence of chaotic attractors. It also can be used to detect the value of the control factor μ (V_c) for chaos and to show that the behavior of the circuit depends on V_c. The bifurcation diagram of the relation between V_c and V_{out} is shown in Fig. 10. By the shift of the transfer curves according to V_c, as shown in Fig. 4(a), the bifurcation structure is changed from periodic to chaotic. The domain of existence of chaos for different values of V_c is in from 0.37 V to 0.44 V (V_b is fixed).

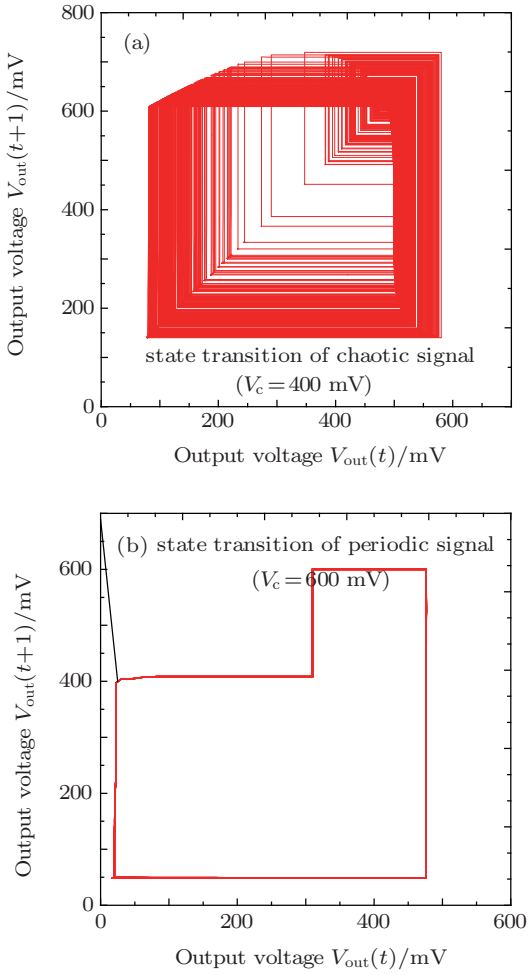


Fig. 8. (color online) Transitions in the phase space: (a) chaotic signal, (b) periodic signal.

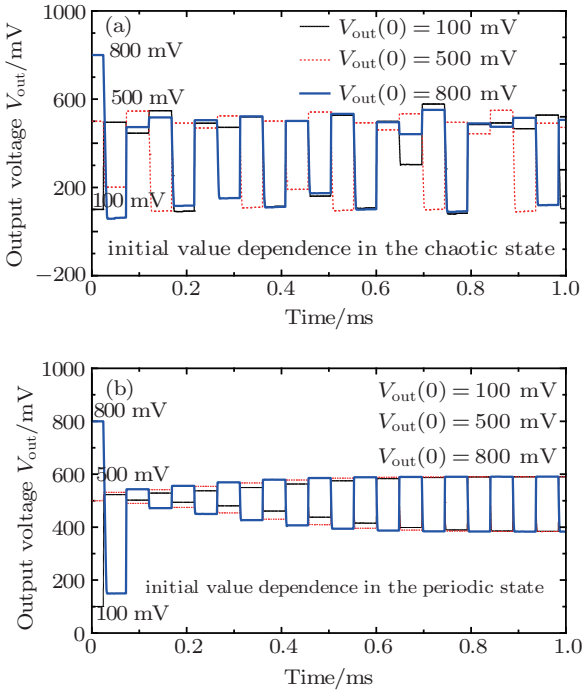


Fig. 9. (color online) Sensitivity with initial conditions: (a) chaotic state, (b) periodic state.

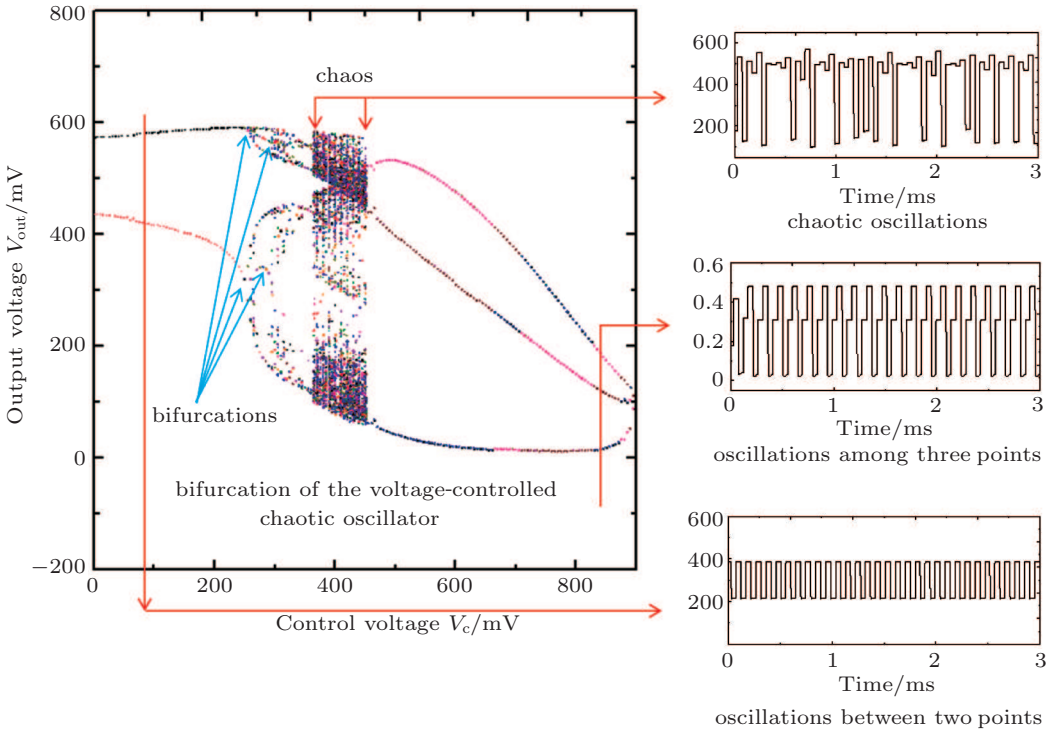


Fig. 10. (color online) Simulated bifurcation diagram for V_{out} versus V_c ($V_b = 0.1$ V).

The proposed circuit is a low-power consumption circuit, with a mixed-circuit between analog and digital. In this chaotic circuit, the power consumption due to the switching of S/H is very low and can be neglected, while the analog parts consume more power and account for the majority of the power consumption. The simulation results show that the total power consumption of the proposed circuit is approximately 7.8 μW. In comparison with the reported circuit in Ref. [4] based on CMOS, the CNFET-based chaotic oscillator consumes power that is several times less owing to the excellent characteristics of the CNFET.

5. Conclusion

In summary, we have proposed a novel, compact, and low-power CNFET-based chaotic oscillator. The proposed chaotic circuit was analyzed by SPICE and was based on the compact and suitable CNFET model of Deng and Wong. The main advantages of the proposed circuit are that it occupies a smaller space (attributed to its compact design) and has lower power dissipation (owing to the use of CNT transistors) than the circuit based on the conventional CMOS technology. The overall performance makes it particularly well suited as a basic element for integration of low-power embedded systems, where many chaos signal generators are required on a single chip. It can also be used in secure communication and chaotic neural networks.

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