Model of hot-carrier induced degradation in ultra-deep sub-micrometer nMOSFET*

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The degradation produced by hot carrier (HC) in ultra-deep sub-micron n-channel metal oxide semiconductor field effect transistor (nMOSFET) has been analyzed in this paper. The generation of negatively charged interface states is the predominant mechanism for the ultra-deep sub-micron nMOSFET. According to our lifetime model of p-channel MOFET (pMOFET) that was reported in a previous publication, a lifetime prediction model for nMOSFET is presented and the parameters in the model are extracted. For the first time, the lifetime models of nMOFET and pMOSFET are unified. In addition, the model can precisely predict the lifetime of the ultra-deep sub-micron nMOSFET and pMOSFET.

Keywords: n-channel metal oxide semiconductor field effect transistor, hot carrier, degradation, lifetime model

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1. Introduction

In ultra-deep sub-micrometer technologies, the continuous shrink of transistor channel length and dielectric thickness without a corresponding reduction of the supply voltage provokes the device operation at high drain current I_d and high gate voltage V_g. However, hot-carrier (HC) degradation remains a critical reliability challenge for metal oxide semiconductor field effect transistor (MOSFET) devices.[1–5]

Many people have studied the question of HC degradation and they have obtained lots of results. For n-channel MOSFETs (nMOSFETs) the substrate current is used as the lifetime predictor because the worst device degradation appears under the stress condition in the saturation region (gate voltage V_g at maximum substrate current).[6] While for p-channel MOSFETs (pMOSFETs) the gate current is used as the lifetime predictor because the stress at the maximum gate current leads to the fastest degradation.[7,8] However, there is no model that can be used to predict the HC degradation in both nMOSFETs and pMOSFETs.

In this paper, we examine HC degradations of nMOSFETs with different sizes under different stress conditions. At the same time, the factors that influence the device characteristics are analyzed, and the relevant parameters are extracted. Based on the results, the HC degradation lifetime of nMOSFETs has been evaluated using the previously reported model.[8] The lifetime models of nMOFETs and pMOSFETs are unified.

2. Devices and experiments

The nMOSFETs used in this work were fabricated by 90 nm CMOS technology with lightly doped drain (LDD) structure and a shallow trench isolation (STI) scheme. The gate oxide was 1.4 nm thick and it was formed in a decoupled plasma nitridation (DPN) process. The gate length was varied from 90 nm up to 0.22 μm, and the gate width was changed from 2 μm to 10 μm.

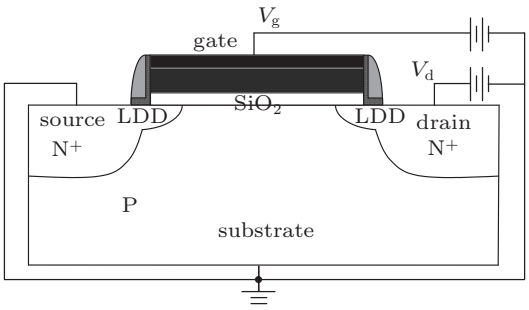


Fig. 1. Schematic diagram of HC stress.

For the experimental measurements, the samples were subjected to the worst stress ($V_g = V_d = 1.4$ V, 1.6 V, 1.8 V, 2.0 V, with the bulk and the source grounded).[9,10] Figure 1 shows the schematic diagram of hot carrier stress. All electrical tests and stresses were performed by an Agilent B1500A high precision semiconductor parameter analyzer at ambient temperature. In all cases, the stress was interrupted at regular intervals and the device parameters were measured. By ana-

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lyzing the changes of the device parameters, the degradations of the threshold voltage (V_{th}), the maximal transconductance (G_{mmax}), and the drain currents in linear (I_{dlin}) and saturation (I_{dsat}) regime were monitored.

3. Results and discussion

3.1. HC degradations of nMOSFETs

Figure 2 present the output and the transfer characteristic degradations of nMOSFETs with 0.09 μm channel length (L) and 10 μm channel width (W) under $V_d = V_g = 1.8$ V stressing. It is evident that the HC induced degradations are significant.

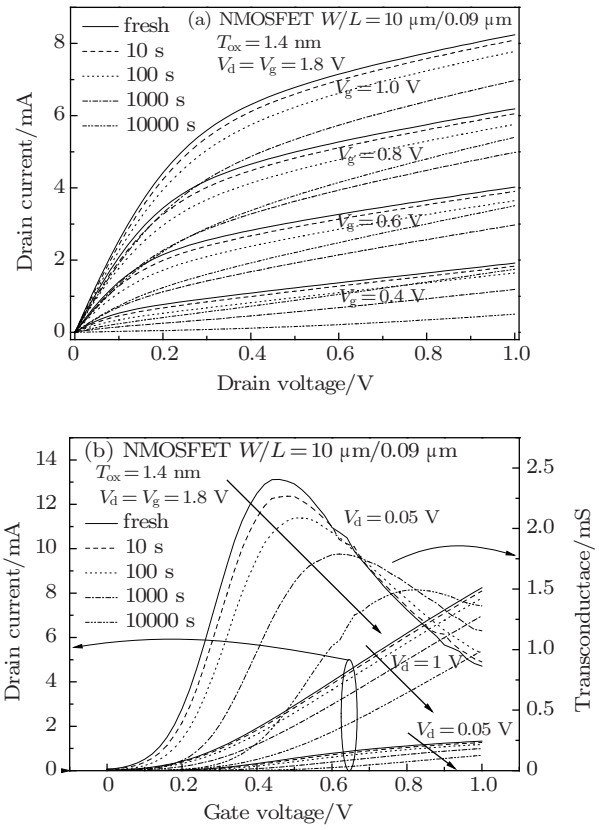


Fig. 2. Device characteristic degradations under $V_d = V_g = 1.8$ V hot carrier stress: (a) output characteristics, (b) transfer characteristics at the linear region $V_d = 0.05$ V and the saturation region $V_d = 1$ V.

After 10^4 s, the drain current is clearly degraded for any given bias condition (e.g, I_{dlin} and I_{dsat}). The changes in both transconductance peak magnitude and position as a function of the stress time are shown in Fig. 2(b). The G_{mmax} decreases after the HC stress, and the transconductance peak position shifts to a more positive V_g. Consequently, the V_{th} extracted by the maximal transconductance method is positively shifted (increases) after the stress.

We examine the mechanism responsible for the device degradation by examining the change in the threshold voltage. Figure 3 shows the degradation in the threshold voltage with stress time by plotting the change in the threshold voltage with time, the threshold voltage is normalized to the initial threshold voltage (V_{th0})

$$\Delta V_{th} = \frac{(V_{th} - V_{th0}) \times 100\%}{V_{th0}}. \quad (1)$$

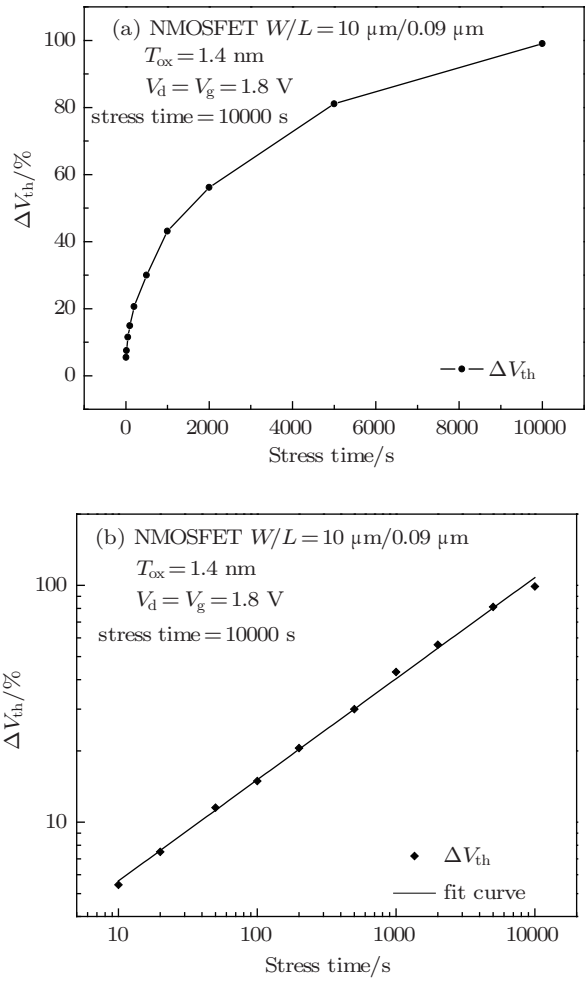


Fig. 3. Normalized changes in V_{th} with stress time: (a) in linear coordinate, (b) in log–log scale coordinate.

The degradation of V_{th} observed in Fig. 3 indicates negative charge generating in the gate oxide, which arises from the electron trapping in the dielectric bulk or the negatively charged interface states creating at the dielectric interface. It may be difficult to draw a distinction between the two phenomena because it is difficult to distinguish between bulk and interface traps in the case of ultra-thin dielectrics. Since the electron trapping has a logarithmic dependence on time while the increase in V_{th} is a power-law function of time (see Fig. 3(b)), as expressed in Eq. (2), which is accordant with the interface generation model,[11] the degradation is predominantly caused by the generation of the interface states

$$\Delta V_{th} \propto t^n. \quad (2)$$

The parameter n is the slope of the fitting line in Fig. 3(b).

Figure 4 presents the energy-band diagrams, which are used to illustrate the influence of the acceptor interface state

on the device performances. In the saturation region, the band edge bends downward, as shown in Fig. 4(a). The intrinsic level (E_i) is closer to, but remains higher than, the Fermi level (E_F). As a result, the acceptor interface state is not occupied by electrons and is neutral. When the device is biased in the linear region, the bands bend downward even more, as described in Fig. 4(b). The acceptor interface state below E_F is occupied by electrons and becomes negatively charged. The effective gate voltage decreases due to the generation of the interface traps. Accordingly, V_{th} increases and G_{mmax}, I_{dlin}, and I_{dsat} decrease.

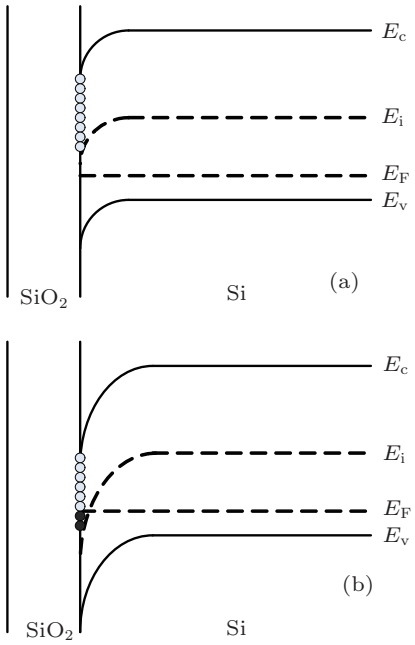


Fig. 4. Schematic diagram of interface traps for nMOSFETs in (a) the saturation region and (b) the linear region.

3.2. Parameter extraction of the HC lifetime model

Figures 5(a)–5(c) show the changes in normalized V_{th} degradation during stressing in log–log scale with the channel width, the channel length, and the stress voltage as the varying parameter, respectively. All of the plots seem to follow the power-law format, and the time evolution coefficient n in Eq. (2) is about 0.43. Figure 5(a) demonstrates that more degradation caused by the HC stress appears in smaller channel width devices. Moreover, in all samples, the relatively short channel length devices are subjected to more serious degradation, as shown in Fig. 5(b). In Fig. 5(c), the degradation becomes severe as the stress voltage increases.

Figures 6(a)–6(c) show the relationships between V_{th} degradation induced by the HC stress after 10^4 s and $1/W$, $1/L$, and $1/V_d$, respectively. Obviously, as shown in Figs. 6(a) and 6(b), the V_{th} degradation follows a power-law dependence on $1/W$ with a slope of $a = 0.21$ and a power-law dependence on $1/L$ with a slope of $b = 6.35$. The formulas are expressed as

$$\Delta V_{th} \propto (1/W)^a, \tag{3}$$

$$\Delta V_{th} \propto (1/L)^b. \tag{4}$$

In addition, the degradation of V_{th} versus $1/V_d$ is plotted in the ln–linear scale, as shown in Fig. 6(c), and is fitted with the following expression:

$$\Delta V_{th} \propto \exp(c/V_d). \tag{5}$$

The parameter c is equal to -13.58 which is the slope of the fitting curve.

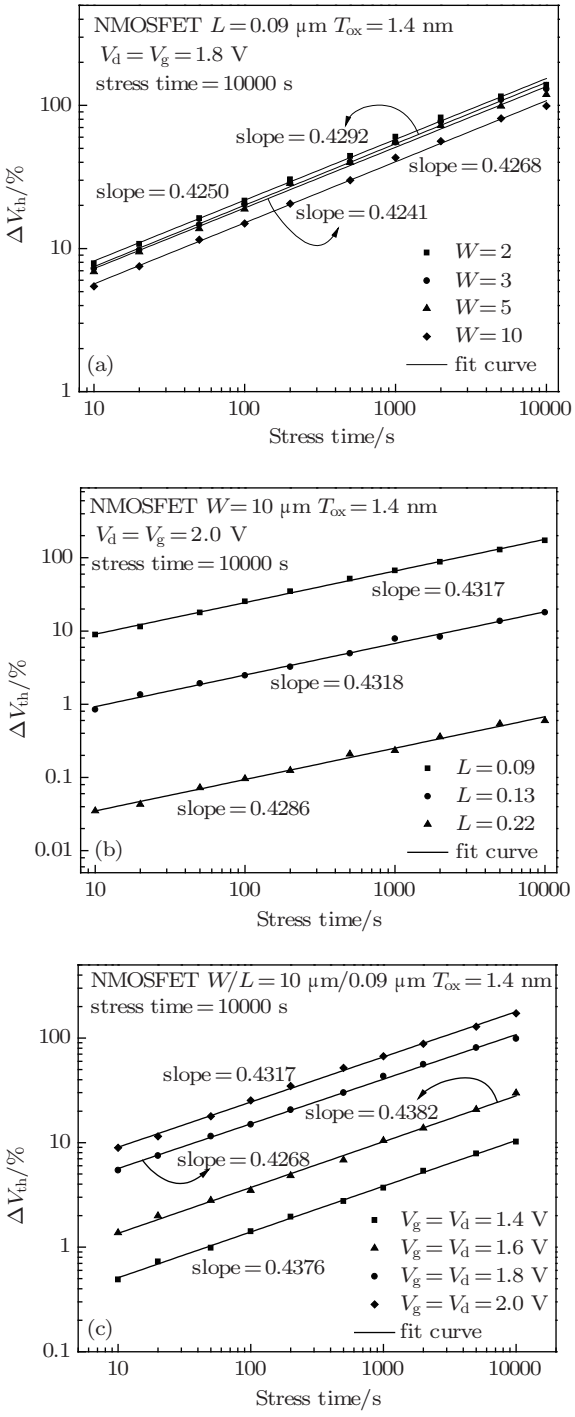


Fig. 5. Changes in normalized V_{th} degradation during stressing with (a) the channel width, (b) the channel length, and (c) the stress voltage as the varying parameter.

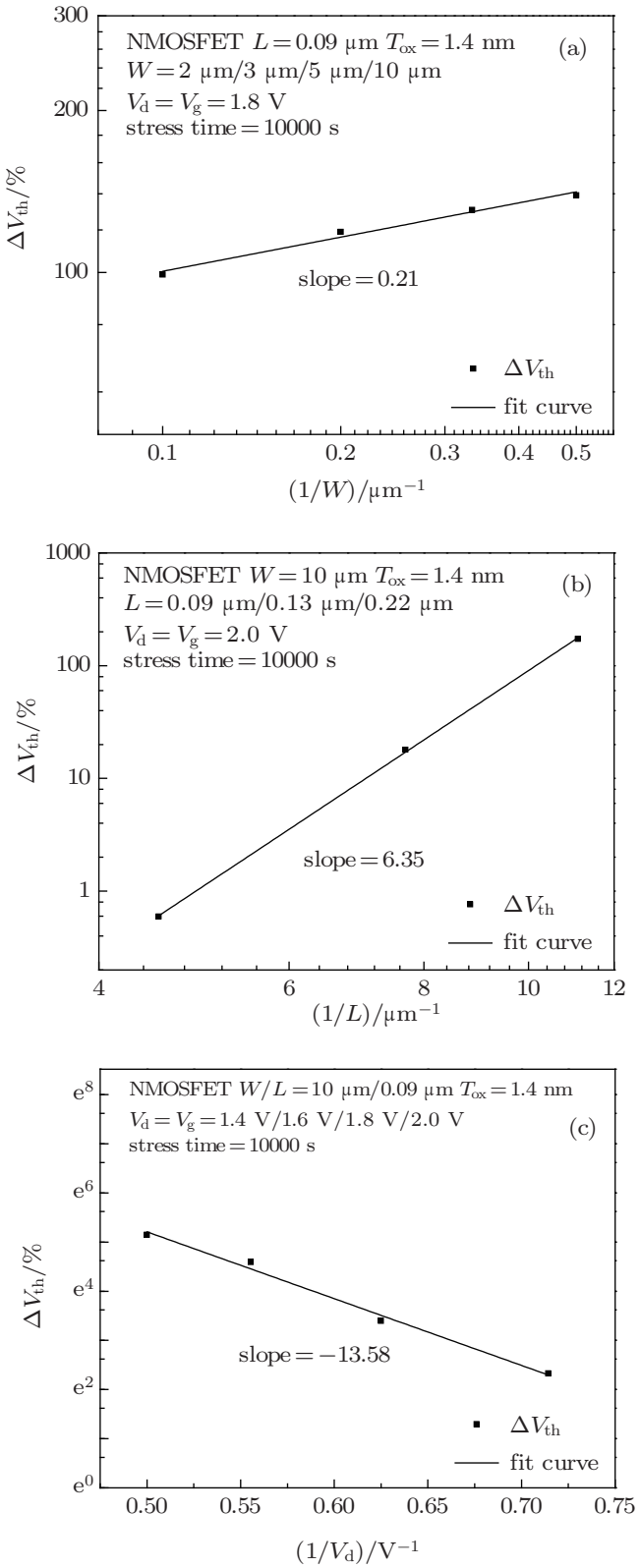


Fig. 6. Relationships between V_{th} degradation and (a) $1/W$, (b) $1/L$, and (c) $1/V_d$.

Therefore, based on expressions (2)–(5), the V_{th} degradation model can be expressed as

$$\Delta V_{th}=Ct^n\,(1/W)^a\,(1/L)^b\exp\left(c/V_d\right), \tag{6}$$

where C is a constant that depends on technology and can be extracted from the experiment data.

3.3. HC lifetime prediction

The lifetime model for nMOSFET is obtained by a procedure similar to that for pMOSFET, as already described in Ref. [8], and has the same formula as Eq. (7) by changing the parameters

$$\tau=P/\left[C\,(1/W)^a\,(1/L)^b\exp\left(c/V_d\right)\right]^{1/n}. \tag{7}$$

In other words, the lifetime models of nMOFETs and pMOSFETs are unified.

A 10% degradation in V_{th} is considered as the failure criterion conventionally. Figure 7 presents the device lifetime for ten samples listed in the inserted table. As can be observed, the model can precisely predict the lifetime of ultra-deep submicron nMOSFETs and pMOSFETs.

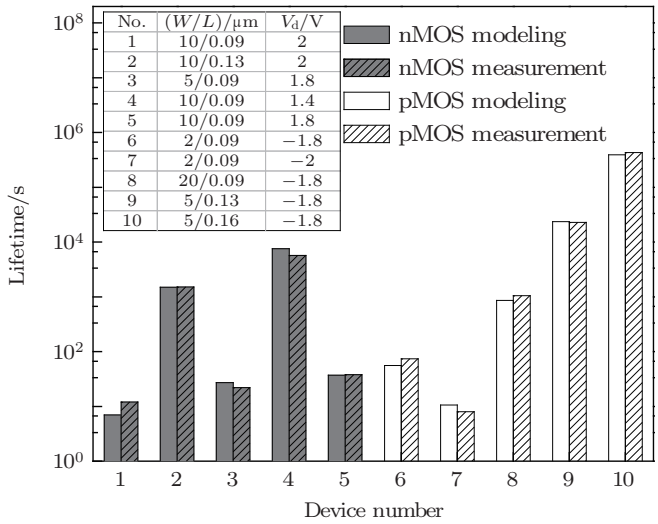


Fig. 7. Comparison of the device lifetime between measurement values and model values.

4. Conclusion

The hot carrier degradation in ultra-deep sub-micron nMOSFETs with different sizes under different stress conditions has been analyzed. For ultra-deep sub-micron nMOSFETs, the predominant degradation mechanism has been found to be the generation of negatively charged interface states at the dielectric interface. Based on the experimental data and the previously reported model of pMOSFETs,[8] the lifetime model of nMOSFETs is proposed and the model parameters are extracted. According to our verification, the model could be used to predict the lifetime with great precision. In addition, the lifetime models of nMOFETs and pMOSFETs are unified for the first time.

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