Interface states in Al_2O_3/AlGaN/GaN metal-oxide-semiconductor structure by frequency dependent conductance technique*

Liao Xue-Yang(廖雪阳)[a)b)†], Zhang Kai(张 凯)[b)], Zeng Chang(曾 畅)[a)], Zheng Xue-Feng(郑雪峰)[b)], En Yun-Fei(恩云飞)[a)], Lai Ping(来 萍)[a)], and Hao Yue(郝 跃)[b)]

[a)] *Science and Technology on Reliability Physics and Application of Electronic Component Laboratory, the 5th Electronics Research Institute of the Ministry of Industry and Information Technology, Guangzhou* 510610, *China*

[b)] *Key Laboratory for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an* 710071, *China*

(Received 25 April 2013; revised manuscript received 23 October 2013; published online 18 March 2014)

Frequency dependent conductance measurements are implemented to investigate the interface states in Al_2O_3/AlGaN/GaN metal-oxide-semiconductor (MOS) structures. Two types of device structures, namely, the recessed gate structure (RGS) and the normal gate structure (NGS), are studied in the experiment. Interface trap parameters including trap density D_{it}, trap time constant τ_{it}, and trap state energy E_T in both devices have been determined. Furthermore, the obtained results demonstrate that the gate recess process can induce extra traps with shallower energy levels at the Al_2O_3/AlGaN interface due to the damage on the surface of the AlGaN barrier layer resulting from reactive ion etching (RIE).

Keywords: Al_2O_3/AlGaN/GaN, interface trap states, conductance, capacitance

PACS: 73.20.–r, 73.20.At, 73.40.Kp, 73.40.Qv **DOI:** 10.1088/1674-1056/23/5/057301

1. Introduction

GaN based high-electron-mobility transistors (HEMTs) have been widely applied in the areas of high power, high frequency, and high temperature due to their large band gap, high breakdown field, and high thermal conductivity. However, poor reliability induced by excess gate leakage is an issue that limits the commercial application of these devices. Various kinds of gate insulators have been used in AlGaN/GaN metal-insulator-semiconductor (MIS) HEMTs[1–6] to suppress the gate leakage and thus to improve the long-term reliablity. Among them, Al_2O_3 dielectric seems to be attractive due to its large bandgap and relatively high dielectric constant. Nevertheless, these gate insulators are mostly deposited *ex-situ*, possibly introducing additional defects related to material growth and device processes. Furthermore, the quality of the interface between the insulator and semiconductor remains the critical factor which affects the fulfillment of the expected performance of the structure. A poor interface can lead to the threshold voltage instability by changing charging conditions of trap states and the increased leakage current by trap-assisted tunneling. On the other hand, the gate recessing process has been frequently utilized as a method of increasing the transconductance, which is reduced by the inclusion of gate insulators. However, to date, there has been a lack of adequate information about the trap characterization of devices subjected to gate recessing. Therefore, it is greatly worthwhile to investigate quantitatively the interface trap states between the insulator and the semiconductor before and after gate recessing.

Nowadays, many techniques are widely used for the characterization of trap states in GaN-based HEMTs such as deep-level transient spectroscopy (DLTS),[7] gate-drain conductance[8,9] measurement, and capacitance–frequency–temperature (C–f–T) mapping.[10] In this paper, a frequency dependent conductance method has been implemented to analyze the Al_2O_3/AlGaN interface trap states in two types of MOS diodes.

2. Experimental details

The AlGaN/GaN epitaxial layer was grown by metal-organic chemical vapor deposition (MOCVD) on SiC substrates. From the top down, the epitaxial structure consists of a 16 nm to 18 nm $Al_{0.3}Ga_{0.7}N$ barrier layer, a 1-nm AlN interlayer, a 1.5-μm GaN buffer layer, and a 100 nm to 140 nm AlN nucleation layer. A 5-nm Al_2O_3 oxide layer was deposited by atomic layer deposition (ALD) as the gate insulator to reduce the gate leakage current. Two types of MOS diodes are investigated in this article, as shown in Fig. 1. Both were fabricated in the same process except that the barrier layer under the gate electrode of one type was recessed about 5 nm by Cl_2-based reactive ion etching (RIE) in order to increase transconductance. For simplicity, we herein call them the recessed gate structure (RGS) and the normal gate structure (NGS), respectively. Circular shaped MOS diodes are utilized for conductance and capacitance measurements with a circular gate contact whose diameter is 130 μm. The gate contact is surrounded by ohmic contact with an Ohmic–Schottky separation of 30 μm (see Fig. 1(c)). Electrical characterizations of these MOS Schottky diodes were carried out using a Keithley 4200SCS semiconductor parameter analyzer.

*Project supported by the National Basic Research Program of China (Grant No. 2011CBA00606).

†Corresponding author. E-mail: vicki_216@163.com

© 2014 Chinese Physical Society and IOP Publishing Ltd

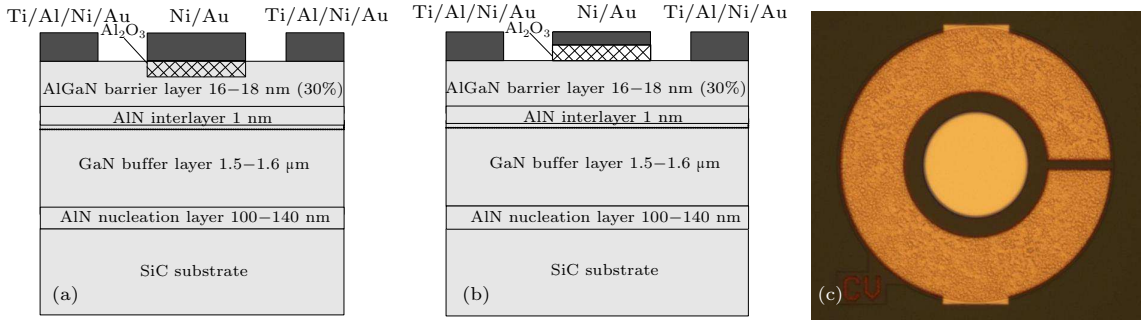


Fig. 1. (color online) Cross sectional view of (a) RGS and (b) NGS. (c) Planform of Al_2O_3/AlGaN/GaN MOS-diodes.

The reverse gate leakage current of the two structures are measured to be 1.45×10^{-6} A and 3.01×10^{-8} A respectively, at a voltage across Schottky–Ohmic contact $V_{SO} = -20$ V, as plotted in Fig. 2. Obviously, the leakage current of the RGS is two orders of magnitude higher than that of the NGS, which suggests the possible existence of relatively higher trap densities at the Al_2O_3/AlGaN interface in RGS.

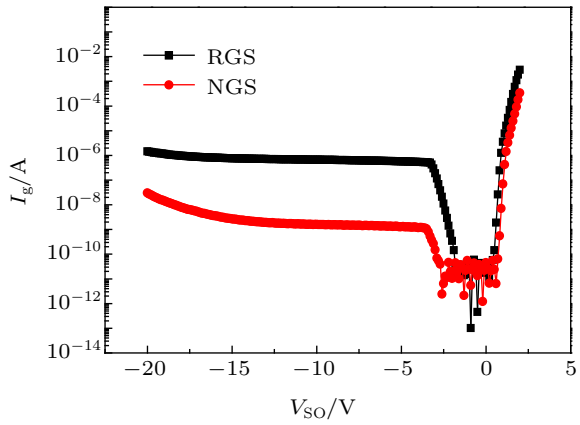


Fig. 2. (color online) Schottky characteristics of Al_2O_3/AlGaN/GaN MOS diodes.

The capacitance–conductance experiments were performed in the voltage range from −5 V to 1.6 V and in the frequency range from 10 kHz to 1 MHz at room temperature to evaluate trap time constant (τ_{it}) and trap state density (D_{it}). Interface trap states between Al_2O_3 and AlGaN can be explicitly studied by biasing diodes at voltages above 0 V. The equivalent circuit of the MOS diodes at forward biases is illustrated in Fig. 3(a), where C_{ox} is oxide capacitance, and C_{AlGaN} is the capacitance of the AlGaN barrier layer. Here, the electrical behavior of Al_2O_3/AlGaN interface trap states is modeled by a parallel combination of the interface state capacitance C_{it} and the interface state conductance G_{it}, whereas the possible contribution from interface trap states at the AlGaN/GaN heterostructure is not included because the trapping/de-trapping processes of AlGaN/GaN interface states do not take place at forward biases.[11]

From the simplified circuit model (see Fig. 3(b)), equivalent parallel conductance (G_p/ω) values can be expressed as[12]

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_m}{\omega^2 (C_m - C_{ox})^2 + G_m^2}, \tag{1}$$

where C_m and G_m are the capacitance and conductance measured at different frequencies and gate biases, respectively, C_{ox} is given by

$$C_{ox} = \frac{A\varepsilon_0\varepsilon_s}{d}, \tag{2}$$

where the area of oxide layer A is 1.33×10^{-4} cm^2, the thickness d is 5 nm, and the dielectric constant ε_s is estimated to be 8.9. Thus, C_{ox} can be calculated to be 209 pF.

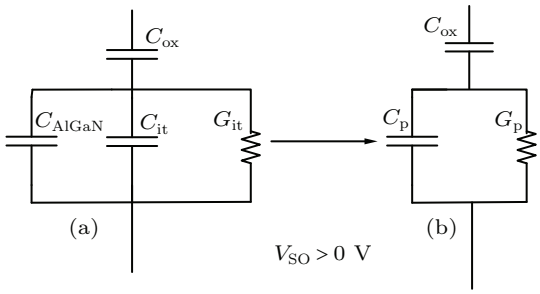


Fig. 3. (a) Equivalent circuit for the conductance method at forward biases. (b) Diagram of the simplified circuit model.

The characterization of trap states deduced from the capacitance and parallel conductance curves is made by assuming that traps are localized either in a single energy level or in continuum states.[13]

For a single energy level, G_p/ω is given by

$$\frac{G_p}{\omega} = \frac{qD_{it}\omega\tau_{it}}{1 + \omega^2\tau_{it}^2}. \tag{3}$$

For a continuum of states, G_p/ω is given by

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2]. \tag{4}$$

With resultant G_p from Eq. (1), parameters D_{it} and τ_{it} are extracted by fitting the experimental G_p/ω values according to Eq. (3) or (4). Then, G_p/ω values are plotted against ω at selected forward Schottky–Ohmic biases (V_{SO}) to investigate trap states with different energy levels.

3. Results and discussion

Typical C–V curves for RGS and NGS are depicted in Fig. 4 at frequencies of 10 kHz and 50 kHz, respectively. As can be seen, the threshold voltage of the RGS is about 0.3 V higher than that of the NGS, resulting from the shorter gate-to-channel distance due to gate recessing. At the same time, we find that capacitance dispersions in the vicinity of respective threshold voltage are almost unobservable, reflecting that trap states at the AlGaN/GaN heterostructure are negligible. Nevertheless, the frequency dispersion becomes significant for positive voltages from 1 V to 1.6 V for both structures. This is caused by the response of interface trap states at the Al_2O_3/AlGaN interface to the measurement signal. Furthermore, capacitance as a function of frequency (C–f) at different voltages is measured as shown in Fig. 5. Large capacitance fluctuations in the low frequency range from 10 kHz to 100 kHz are obvious, whereas capacitance becomes nearly constant at higher frequencies. At low frequencies, electrons trapped at the Al_2O_3/AlGaN interface can follow the signal, resulting in a high capacitance value. As the frequency increases, less trapped electrons are capable of tracing the high frequency signal and, as a consequence, the measured capacitance starts to decrease and reaches an almost constant value at 1 MHz.

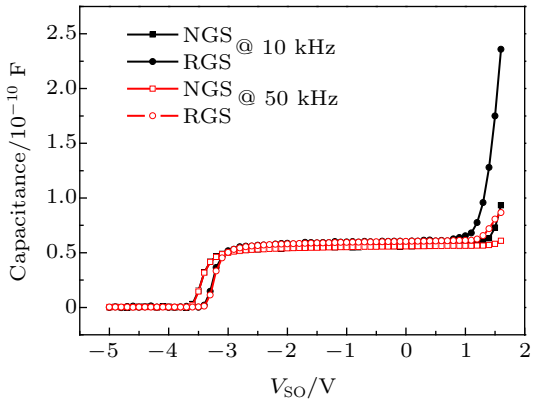


Fig. 4. (color online) The C_m–V characteristics of Al_2O_3/AlGaN/GaN MOS diodes.

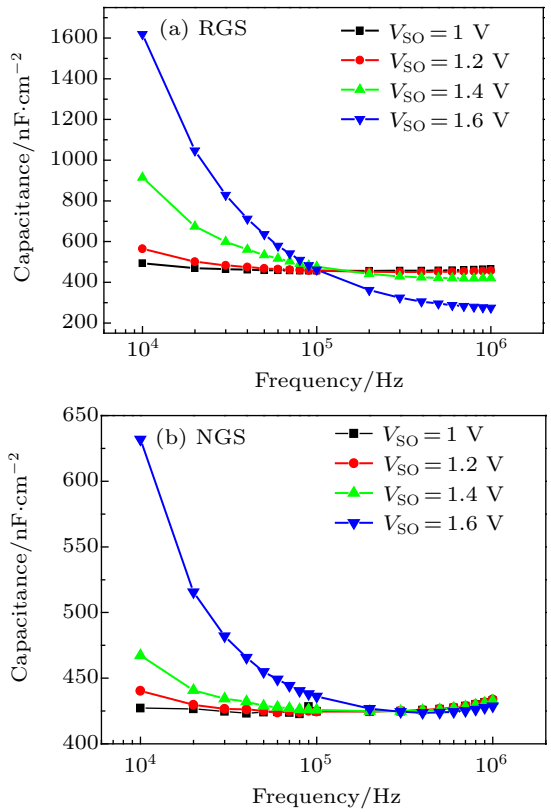


Fig. 5. (color online) Measured capacitance C_m versus frequency at several biases V_{so} for (a) RGS and (b) NGS.

Figure 6 shows fitting results obtained according to Eq. (3) or (4). Taking a single energy level into account specifically, good agreement with experimental data can be achieved, indicating the validity of the model used. The trap density D_{it} at the Al_2O_3/AlGaN interface of the RGS is extracted to be about 1.17×10^{13}–1.41×10^{13} eV^{-1}·cm^{-2} with a corresponding τ_{it} of 5.5–0.125 μs, while D_{it} of the NGS is about 0.32×10^{13}–1.37×10^{13} eV^{-1}·cm^{-2} with a corresponding τ_{it} of 75.6–1.34 μs.

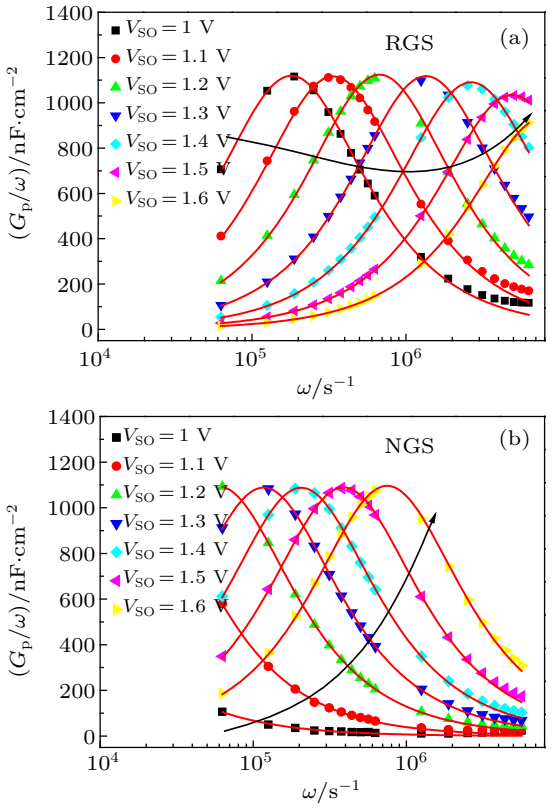


Fig. 6. (color online) Frequency dependent parallel conductance at the Al_2O_3/AlGaN interface at selected biases V_{SO} (from 1 V to 1.6 V, step = 0.1 V) for (a) RGS and (b) NGS. Solid lines are fitting results.

The trap state energies are estimated using the expression[10]

$$\tau = (\sigma_T N_c \upsilon_t)^{-1} \exp\left(\frac{E_T}{kT}\right), \quad (5)$$

where the capture cross section of trap states $\sigma_T = 3.4 \times 10^{-15}$ cm^2, the density of states in the conduction band $N_c = 2.2 \times 10^{18}$ cm^{-3} and the average thermal velocity of carriers $\upsilon_t = 2.6 \times 10^7$ cm/s.[14] The resulting relationships between trap state densities and their energy levels are illustrated in Fig. 7(a). Trap state energies in the RGS are in the range from 0.361 eV to 0.263 eV, which appear to be lower than those in the NGS as a whole. The detailed data are shown in Table 1. From the figure, it can be concluded that a higher density of interface trap states with shallower energy levels exists in the RGS when compared with the NGS. Thus, we assume that the gate recessing process induces extra trap states at the Al_2O_3/AlGaN interface due to the damage on the surface of the AlGaN barrier layer introduced by RIE. The unfavorable effect should be responsible for the increased leakage current exhibited in Fig. 2. Additionally, figure 7(b) shows the resulting τ_{it} as a function of the applied voltage. Exponential τ_{it}–V_{SO} dependencies obtained for both devices are obvious. This can be ascribed to be the good interface uniformity between Al_2O_3 and AlGaN in our experiment. Besides, this also indicates that the gate recessing process used here does not bring about interface nonuniformity. As revealed in Eq. (5), the trap time constant depends exponentially on the trap energy, which varies linearly with the applied voltage. That means, for a uniform insulator/semiconductor interface, the time constant should be an exponential function of the voltage. No deviation from the expected exponential function suggests the absence of the surface potential fluctuation due to nonuniformities in interface traps. As a comparison, recently, excess traps at deep energy levels of 0.52 eV below the conduction band with D_{it} of 4×10^{12} eV^{-1}·cm^{-2} were reported for thin 2-nm-AlN based AlGaN/GaN MIS structures.[15] Kordoš *et al.* identified two dominant trap states, fast and slow, at Al_2O_3/AlGaN/GaN/Si MISHEMTs by temperature dependent conductance measurements. Fast traps had a density of 1.4×10^{12} eV^{-1}·cm^{-2} at an energy level of 0.27 eV, while the density of the slow traps increased with the increase of the temperature up to 8×10^{13} eV^{-1}·cm^{-2}.[16] Compared with these published data, Al_2O_3/AlGaN interface trap density shows nearly one order of magnitude higher. In general, trap density and its energy levels can vary with insulators. We estimate that oxygen related bonding at the Al_2O_3/AlGaN interface is an important resource for the higher trap density. The exact physical origin of this, however, needs to be further studied in the future. On the other hand, traps located in the mid gap cannot be probed since they cannot sufficiently respond to AC signals during the present *C*–*V* measurements, limiting the D_{it} characterization near the conduction band edge. Therefore, frequency dependent conductance measurements at higher temperatures and ultra violet irradiation are necessary to obtain the distribution of deeper trap states in the band gap.

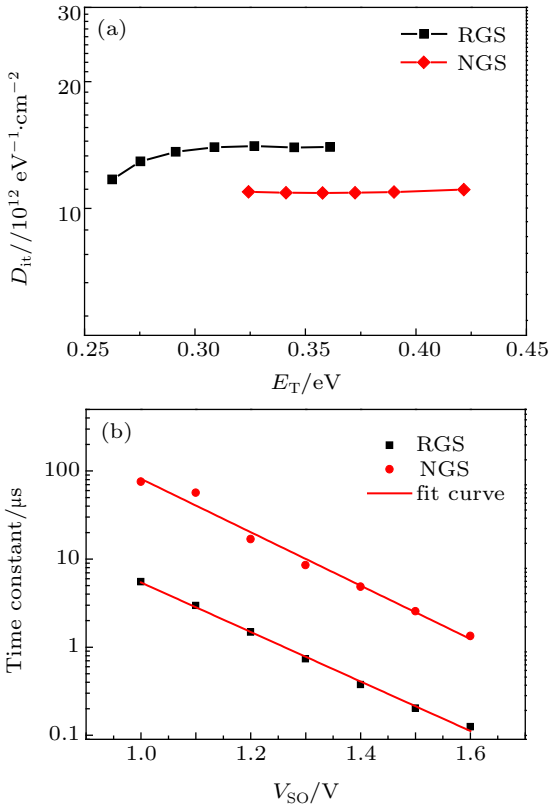


Fig. 7. (color online) (a) Trap states density as a function of their energies. (b) Trap time constant as a function of gate voltages.

Table 1. Details about trap states at the Al_2O_3/AlGaN interface.

	RGS MOS structure			NGS MOS structure		
Voltage	Trap density	Time constant	Energy level	Trap density	Time constant	Energy level
V_{SO}/V	D_{it}/eV^{-1}·cm^{-2}	τ_{it}/μs	/eV	D_{it}/eV^{-1}·cm^{-2}	τ_{it}/μs	/eV
1.0	1.399×10^{13}	5.5	0.361	3.247×10^{12}	75.6	0.429
1.1	1.396×10^{13}	2.97	0.345	1.391×10^{13}	56.8	0.422
1.2	1.406×10^{13}	1.49	0.327	1.367×10^{13}	16.8	0.39
1.3	1.398×10^{13}	0.74	0.309	1.361×10^{13}	8.55	0.372
1.4	1.363×10^{13}	0.38	0.291	1.36×10^{13}	4.86	0.358
1.5	1.293×10^{13}	0.2	0.275	1.362×10^{13}	2.57	0.341
1.6	1.172×10^{13}	0.13	0.263	1.37×10^{13}	1.34	0.324

4. Conclusions

In summary, trap states at the Al_2O_3/AlGaN interface in Al_2O_3/AlGaN/GaN MOS structures have been investigated by frequency dependent conductance measurements. Trap characteristics in RGS and NGS structures are compared. According to the results, a conclusion can be achieved that the gate recessing process can induce excess trap states with shallower energy levels at the Al_2O_3/AlGaN interface since RIE can damage the surface of the AlGaN barrier layer. Aggravated Schottky leakage characteristics after gate recessing can be a result of increased trap states at the Al_2O_3/AlGaN interface. Therefore, the impact of various processes on Al_2O_3/AlGaN interface trap states, such as pretreatment before Al_2O_3 deposition and high temperature annealing after gate formation, need to be investigated further to reduce trap density and eliminate the damage by gate recessing.

References

[1] Huang L H and Lee C T 2007 *J. Electrochem. Soc.* **154** H862
[2] Ostermaier C, Lee H C, Hyun S Y, Ahn S I, Kim K W, Cho H I, Ha J B and Lee J H 2008 *Phys. Stat. Solid C* **5** 1992
[3] Freedsman J J, Kubo T, Selvaraj S L and Egawa T 2011 *Jpn. J. Appl. Phys.* **50** 04DF03
[4] Yue Y Z, Hao Y and Zhang J C 2008 *Chin. Phys. B* **17** 140505
[5] Bi Z W, Feng Q and Hao Y 2010 *Chin. Phys. B* **19** 077303
[6] Wang Z G, Chen Y F and Chen C 2010 *Chin. Phys. B* **19** 107305
[7] Okino T, Ochiai M, Ohno Y, Kishimoto S, Maezawa K and Mizutani T 2004 *IEEE Electron Device Lett.* **25** 523
[8] Miller E J, Dang X Z and Wieder H H 2000 *J. Appl. Phys.* **87** 8070
[9] Quan S, Hao Y and Ma X H 2011 *Chin. Phys. B* **20** 018101
[10] Shih H, Kudo M and Suzuki T 2012 *Appl. Phys. Lett.* **101** 043501
[11] Chu R M, Zhou Y G, Chen K J and Lau K M 2003 *Phys. Stat. Sol.* **07** 2400
[12] Sze S M and Kwok K N 2008 *Physics of Semiconductor Devices* (3rd edn.) (Xi'an: Xi'an Jiaotong University Press)
[13] Nicollian E H and J R Brews 1982 *MOS Physics and Technology* (New York: Wiley)
[14] Gregušová D, Stoklas R and Mizue Ch 2010 *J. Appl. Phys.* **107** 106104
[15] Freedsman J J, Kubo T and Egawa T 2011 *Appl. Phys. Lett.* **99** 033504
[16] Kordoš P, Stoklas R and Gregušová D, Gaži Š and Novák J 2010 *Appl. Phys. Lett.* **96** 013505