# 4H-SiC Schottky barrier diodes with semi-insulating polycrystalline silicon field plate termination*

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(Received 18 July 2013; revised manuscript received 25 November 2013; published online 25 March 2014)

Based on the theoretical analysis of the 4H-SiC Schottky-barrier diodes (SBDs) with field plate termination, 4H-SiC SBD with semi-insulating polycrystalline silicon (SIPOS) FP termination has been fabricated. The relative dielectric constant of the SIPOS dielectric first used in 4H-SiC devices is 10.4, which is much higher than that of the $SiO_2$ dielectric, leading to benefitting the performance of devices. The breakdown voltage of the fabricated SBD could reach 1200 V at leakage current 20 μA, about 70% of the theoretical breakdown voltage. Meanwhile, both of the simulation and experimental results show that the length of the SIPOS FP termination is an important factor for structure design.

**Keywords:** 4H-SiC, Schottky-barrier diodes, semi-insulating polycrystalline silicon, field plates termination

**PACS:** 71.20.Nr, 73.40.Sx, 77.22.Jp **DOI:** 10.1088/1674-1056/23/5/057102

## 1. Introduction

The SiC material, as the typical third generation semiconductor material, has more advantages than Si material. The critical breakdown electrical field of SiC is ten times higher than Si, which makes it an attractive material for the applications in high-voltage and high-power devices. Nowadays, the 4H-SiC Schottky-barrier diodes (SBDs) have already shown a great potential in power systems because of their low-conduction loss, fast switching speed, and high-temperature environments.[1–3] To suppress the effect of electrical field crowding on the breakdown voltage of high voltage SiC devices, the edge termination is necessary, such as field plates (FP), guard rings (GR), and junction termination extension (JTE).[4–6] Among them, FP termination is the simplest one which could be formed with the anode Schottky electrode at the same time. Many process steps such as ion implantation and high-temperature anneal are ignored, avoiding surface damage to degrade device performance, so FP termination is constantly applied in 4H-SiC SBD and silicon dioxide ($SiO_2$) is a commonly used dielectric material for FP termination. However, the relative dielectric constants of $SiO_2$ and SiC are 3.9 and 9.8 respectively, and the lower dielectric constant of $SiO_2$ compared with SiC material results in the electric field in $SiO_2$ to be about 2.5 times higher than that in SiC, therefore giving rise to premature breakdown of $SiO_2$ as the high voltage is applied. In this case, a low dielectric constant of $SiO_2$ dielectric layer will not be suitable for the application of FP termination in advance high voltage SiC devices, otherwise its thickness will be too thick to be unacceptable. To solve this problem, the dielectric materials with a higher relative dielectric constant are necessary and many attempts have been tried, for example, $Si_3N_4$, $Al_2O_3$, $HfO_2$,[7–9] and so on. As we know, the semi-insulating polycrystalline silicon (SIPOS) as a dielectric layer to form FP termination has been successfully used in Si power devices.[10] The relative dielectric constant of the SIPOS is about 10, higher than that of $SiO_2$ and also SiC, which will not only guarantee breakdown occurring in the SiC material in order to give full play to the SiC material advantage, but also it has a mature process. In addition, the length of FP termination is also an important factor. Appropriate length could inhibit the peak electric field on the surface and effectively improve the breakdown voltage of the SBD devices.

In this paper, a 4H-SiC SBD with SIPOS FP termination has been fabricated. The breakdown voltage of 1200 V was obtained, showing in a good agreement with simulation results based on taking no dielectric breakdown, which confirms that SIPOS is an attractive dielectric material used in 4H-SiC power devices with an outstanding performance.

## 2. Fabrication

The SBD schematic structure in this experiment is shown in Fig. 1. 4H-SiC epitaxial wafer was grown on a 4° off-axis N+type 4H-SiC substrate with a thickness of 380 μm and the doping concentration about $5\times10^{18}$ $cm^{-3}$, purchased from Cree Inc. The thickness of the epitaxial drift layer is 15 μm.

*Project supported by the National Natural Science Foundation of China (Grant Nos. 61234006 and 61274079), the Key Specific Projects of Ministry of Education of China (Grant No. 625010101), and the Science Project of State Grid, China (Grant No. SGRI-WD-71-13-004).

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The high frequency (1 MHz) capacitance–voltage ($C$–$V$) measurements for 4H-SiC epitaxial wafer are shown in Fig. 2. The inset displays the inverse square of capacitance $(1/C^2)$ as the function of the gate voltage ($V$). The drift layer doping concentration $N_d$ is about $6.5\times10^{15}$ cm$^{-3}$ extracted from the slope of the plot.

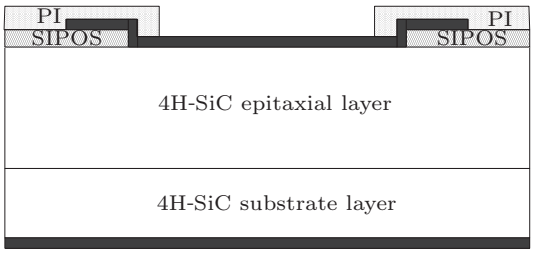



**Fig. 1.** Two-dimensional cross-sectional view of 4H-SiC SBDs.

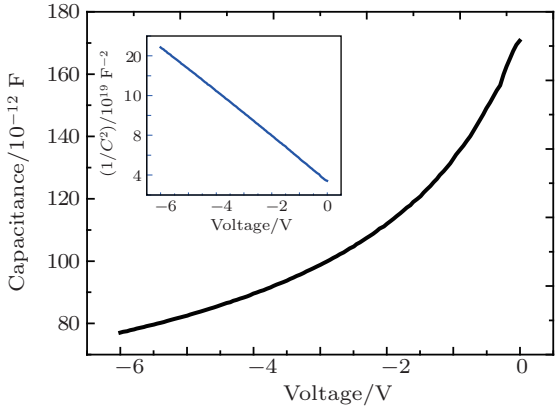



**Fig. 2.** (color online) The $C$–$V$ characteristics for 4H-SiC epitaxial wafer at a frequency of 1 MHz.

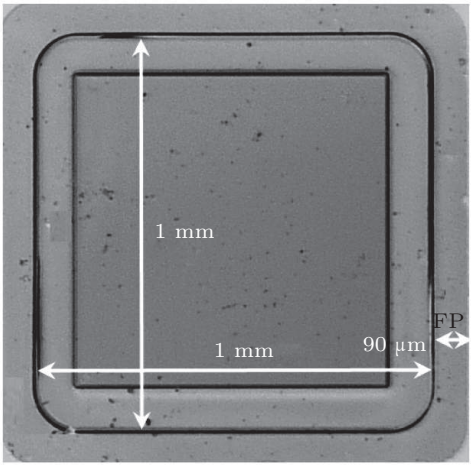



**Fig. 3.** Image of the fabricated 4H-SiC SBD device.

The fabrication process is as follows: after RCA cleaning, the SIPOS dielectric is deposited by using LPCVD technology. Then the Schottky contact windows are opened by wet etching. The backside ohmic contact is formed by sputtering 500-nm Ni with rapid thermal annealing (RTP) at 1000 °C in Ar for 3 min. In addition, 500-nm Ni is deposited on the topside as the Schottky contact soon afterwards,[11,12] with SIPOS FP structure forming at the same time. Finally, Polyimide about 5 μm is utilized as a second passivation layer. The fabricated 4H-SiC SBD cell is shown in Fig. 3. The device has a Schottky contact area of 1 mm×1 mm, including the field plate region.

## 3. Experimental result and discussion

The result of high frequency (1 MHz) retracing capacitance–voltage ($C$–$V$) measurements for the SIPOS dielectric layer is presented in Fig. 4. There are existing trapped charges in it, resulting in the hysteresis phenomenon in the $C$–$V$ curve. It can also be seen from this figure that the capacitance slowly approaches to an accumulation state with the applied voltage increasing, which is caused by leakage current across the dielectric layer.[13] The capacitance can be written as

$$C = \frac{\varepsilon_0 \varepsilon_1 S}{d},$$

where $S$ is the area of the electrode, $d$ is the thickness of the dielectric layer, $\varepsilon_0$ is the dielectric constant in a vacuum, and $\varepsilon_1$ is the relative dielectric constant. The thickness of the SIPOS dielectric layer measured by Profile-system is about 1.8 μm. The relative dielectric constant of the SIPOS dielectric layer is about 10.4 extracted from the Fig. 4, which exhibits consistency with the SIPOS dielectric constant reported in other literatures.[14]

The measured $I$–$V$ characteristics of the fabricated SIPOS MOS structure are shown in Fig. 5. The SIPOS MOS structure is not broken down at a voltage of 1050 V. Considering the thickness of the SIPOS dielectric 1.8 μm, the electrical field in the dielectric layer has reached at least $5.8\times10^6$ V·cm$^{-1}$. Figure 6 shows the simulated electric field distribution of the presented 4H-SiC SBD at the avalanche breakdown point of SiC by ISE-TCAD in order to compare the SIPOS and $SiO_2$ as FP dielectric. It is shown that the peak electrical field in the SIPOS dielectric only attends to $4.3\times10^6$ V·cm$^{-1}$, lower than the experiment result of $5.8\times10^6$ V·cm$^{-1}$, which illustrates that the SIPOS dielectric in our experiment does not breakdown before the SiC material reaches its avalanche breakdown point. On the contrary, the electrical field in the $SiO_2$ dielectric will reach $7.2\times10^6$ V·cm$^{-1}$, slightly higher than the theoretical critical electrical field of $7\times10^6$ V·cm$^{-1}$. Generally, the $SiO_2$ dielectric will breakdown in advance. According to the above results, it is proved that the SIPOS dielectric film in our experiment has an excellent quality and is more suitable for a SiC power device than $SiO_2$.

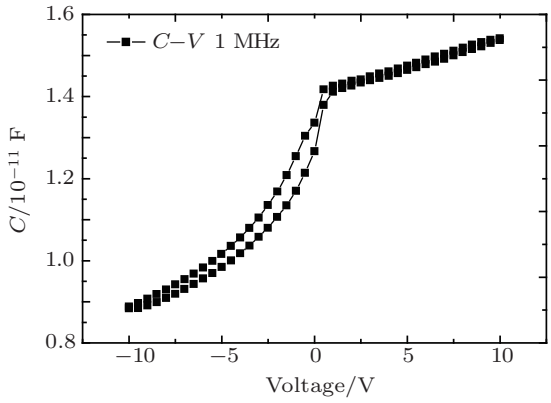



**Fig. 4.** The *C*–*V* characteristics for 4H-SiC epitaxial wafer at a frequency of 1 MHz.

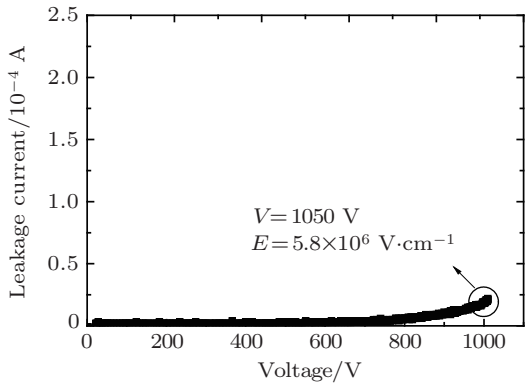



**Fig. 5.** The *I*–*V* characteristics of the 4H-SiC fabricated SIPOS MOS structure.

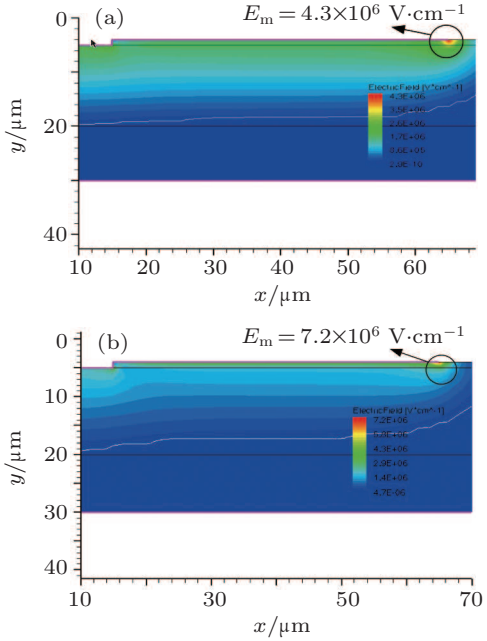



**Fig. 6.** (color online) Simulated electric field distribution of SBD at the breakdown point with SIPOS or $SiO_2$ as the FP dielectric. (a) SIPOS dielectric and (b) $SiO_2$ dielectric.

The *I*–*V* characteristics measurement of 4H-SiC SBD was carried out by using an Agilent B1500 semiconductor parameter analyzer and TEK370B at room temperature. The forward characteristics of 4H-SiC SBD with an area of 1 mm×1 mm are shown in Fig. 7. The forward voltage drop $V_F$ is 3.6 V when the current is 4 A, corresponding to a current density of 400 A/cm$^2$. The specific on-resistance ($R_{sp-on}$) extracted from Fig. 7 is 5.87 mΩ·cm$^2$. Further details of the forward *I*–*V* characteristics of the device are shown in the inset of the Fig. 7, which clearly reveals the turn-on voltage about 1.28 V. The ideality factor ($n$) and the Schottky barrier height ($\Phi_b$) are 1.02 and 1.62 eV respectively. Figure 8 displays the breakdown characteristics of the fabricated 4H-SiC SBD at room temperature. The breakdown voltage is 1200 V at the reverse current of 20 μA when the length of the SIPOS FP is 50 μm, reaching 70% of the theoretical breakdown voltage. Compared with the above results, the SIPOS dielectric in our experiment could be proved to not breakdown when the reverse voltage and leakage current reached to 1200 V and 20 μA.

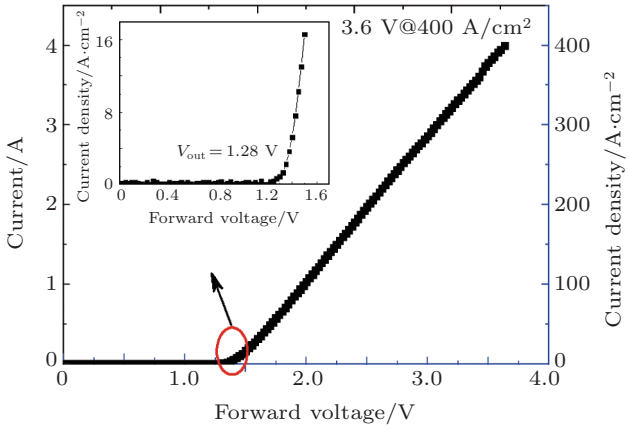



**Fig. 7.** (color online) Measured forward characteristics of the fabricated 4H-SiC SBD.

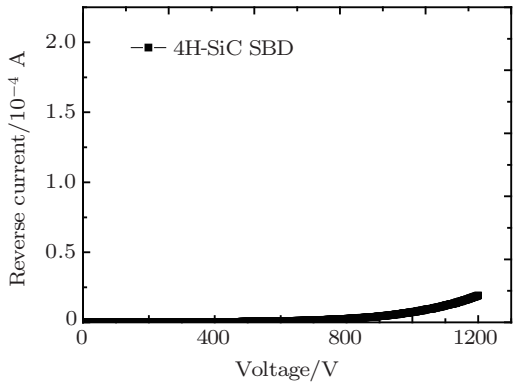



**Fig. 8.** Measured reverse blocking characteristics of the fabricated 4H-SiC SBD.

The reverse characteristics of the SBD versus the length of the FP termination are simulated by ISE-TCAD, without the dielectric layer breakdown considered. The simulated results, together with experiment results, are plotted in Fig. 9. As shown in Fig. 9, the breakdown voltage reaches about 1350 V, i.e., 130 V larger than the experimental result. The trends of simulation and experimental results present a good agreement,

which means the breakdown voltage is increasing with the increase of the length of the FP termination, and there is a knee point at the length of the FP at about 20 μm in this experiment.

Figure 10 shows the simulation results of distribution of the electric field at the interface of the Schottky junction. As can be seen from Fig. 10, there is one electric field peak at the corner of the Schottky junction of SBD without FP termination, leading to premature breakdown at the edge of the Schottky junction. With SIPOS FP termination, it exhibits two electric field peaks which are much lower than the value in the corner for $L_{FP} = 0$ μm and inhibit the peak electric field at the corner of the surface of the Schottky contact. The results also illustrate that it is a good idea to keep a reasonable distance between two peaks to protect the corner of the Schottky junction from premature breakdown.

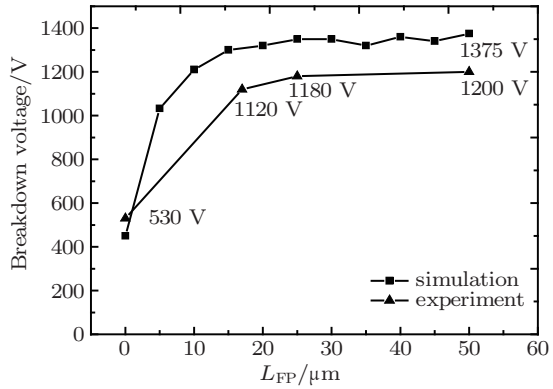



**Fig. 9.** The simulation and experimental results of the breakdown voltage versus the length of the FP.

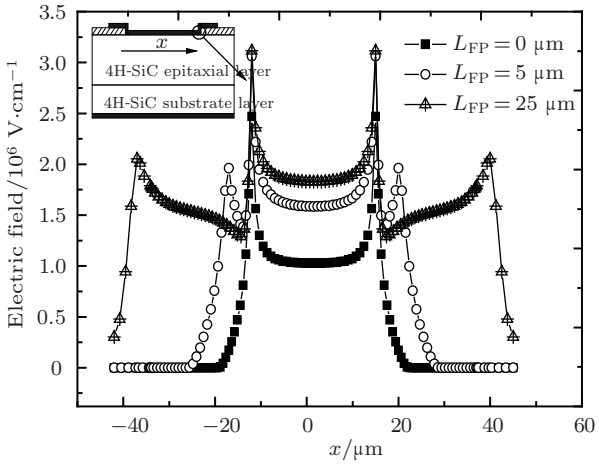



**Fig. 10.** Simulated reverse interface electric field distribution of 4H-SiC SBD.

However, it can be seen that the breakdown voltage of the fabricated 4H-SiC SBD is a little lower than the simulation results. There are many reasons such as the defects in material and process impurity contamination which could cause a drop-down of the breakdown voltage. Anyway, the results have already demonstrated that the SIPOS dielectric is more suitably used in high voltage SiC devices, compared with $SiO_2$.

## 4. Conclusion

In this paper, the high voltage 4H-SiC SBD with FP termination using the SIPOS dielectric is demonstrated for the first time. The 4H-SiC SBD with specific on-resistance ($R_{sp-on}$) of 5.87 mΩ·cm$^2$ and the breakdown voltage of 1200 V has been fabricated by using an only 15-μm thick epilayer doped with $6.5\times10^{15}$ cm$^{-3}$ impurity concentration. The SIPOS has been proved to be more suitable as a dielectric layer used in FP termination of SiC power devices. The higher relative dielectric constant 10.4 prevents breakdown occurring in the dielectric layer, and ensuring the advantages of SiC demonstrated, compared with conventional $SiO_2$. Meanwhile, the trend of experimental results of breakdown voltage versus the length of the SIPOS FP termination shows a good agreement with the simulation results. The SIPOS dielectric has shown its value in the application on the SiC power SBD device and could be used in other types of SiC power devices in the future.

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