Computation of the locus crossing point location of MC circuit*

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In this paper, the crossing point property of the *i*–*v* hysteresis curve in a memristor–capacitor (MC) circuit is analyzed. First, the ideal passive memristor on the crossing point property of *i*–*v* hysteresis curve is studied. Based on the analysis, the analytical derivation with respect to the crossing point location of MC circuit is given. Then the example of MC with linear memristance-versus-charge state map is demonstrated to discuss the drift property of cross-point location, caused by the frequency and capacitance value.

Keywords: memristor, memristive system, crossing point, pinched hysteresis loop

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1. Introduction

The memristor has attracted widespread attention in the fields of the new generation of ultra-high density memory devices,[1] programmable analog circuits,[2] quantum neurons,[3] etc.[4,5] Compared with the traditional resistor–capacitor (RC) circuit, the typical memristor–capacitor (MC) circuit which is composed of a memristor and a capacitor in series has many advantages in the dynamic range, architecture, and programmable ability. These benefits make the MC circuit have a wide application prospect in programmable filters,[6,7] chaotic circuits,[8,9] etc. At present, the MC circuit has been found to have many interesting characteristics, including the charge and discharge time responses,[10] the change of the state caused by the white noise,[11] and the simple hysteretic relationship between voltage and current.[12] Typically, the Lissajous of the voltage and current in the MC circuit looks like two petals, which has a great similarity to the pinched hysteresis curve of a separate memristor. There is also a key crossing point in the locus of the MC circuit, reflecting some basic properties of the circuit.[13–17]

The main purpose of this paper is to analyze the crossing point property of the *i*–*v* hysteresis curve in the MC circuit. The remainder of this paper is organized as follows. In Section 2 we introduce some basic notions of the ideal passive memristor and analyze the crossing point location property. Based on the previous analysis, the crossing point location solution of the MC circuit is derived in Section 3. The example of an MC with linear memristance-versus-charge state map is demonstrated in Section 4, meanwhile the drift property of cross-point location, caused by the frequency and capacitance value, is discussed. Finally, conclusions are given in Section 5.

2. Crossing point of ideal passive memristor

The ideal memristor is defined by inter-relationship between the charge q and the magnetic flux φ. The memristor is defined as

$$R(q) = \mathrm{d}\varphi/\mathrm{d}q. \tag{1}$$

In addition, the passive characteristic of the memristor requires $R(q) > 0$. Clearly, the essential relationship $\varphi = \hat{\varphi}(q)$ of $\varphi \sim q$ which meets the requirements is a strictly monotonically increasing relationship. A strictly monotonically increasing relationship confirmed from the side $\varphi \sim q$ is a one-to-one relationship, which illustrates the equivalence relationship between the ideal passive charge control memristor $R(q)$ and magnetron memristor $W(\varphi)$.

Lemma 1 Under current excitation $i = I_{\max}\sin(\omega t)$, the ideal passive memristor whose resistance state has one-to-one relationship formats the pinched hysteresis curve with only one crossing point, namely the origin.

Proof The voltage–current relationship of the ideal memristor is given as follows:

$$v = R(q)i. \tag{2}$$

With the excitation of the current $i = I_{\max}\sin(\omega t)$, if the voltage and current hysteresis curve intersection exists besides the origin, it is $C(i_c, v_c)$; if it is in the first quadrant, namely in the $0 \sim T/2$ time interval, the intersection is corresponding to two times t_1 and t_2 which satisfy

$$i_c = I_{\max}\sin(\omega t_1) = I_{\max}\sin(\omega t_2), \tag{3}$$

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where $t_1 + t_2 = T/2$ and $t_1 \neq t_2$.

Also, the internal state of the memristor can be calculated by

$$q_{\tau=t} = q_{\tau=0} + \Delta q = q_{\tau=0} + \frac{I_{\max}}{\omega}(1 - \cos(\omega t)). \quad (4)$$

We have $q_{\tau=t_1} \neq q_{\tau=t_2}$, thus the resistance state picture of the memristor presents a one-to-one relationship.

So, $R(q_{\tau=t_1}) \neq R(q_{\tau=t_2})$, and $R(q_{\tau=t_1})i_c \neq R(q_{\tau=t_2})i_c$. There exists no such situation where both voltage and current values are equal. With the same idea, we can prove that there exists no intersection in the third quadrant of i–v plane.

3. Solving the locus crossing point location of the MC circuit

When connecting a passive memristor with a capacitor in series as shown in Fig. 1, the v–i relationship of such a circuit is determined by

$$v = v_1 + v_2 = R(q)\, i + \frac{q}{C}, \quad (5)$$

$$q = \int_0^t I_{\max} \sin(\omega\tau)\, \mathrm{d}\tau = \frac{1}{\omega}(1 - \cos(\omega t))\, I_{\max}. \quad (6)$$

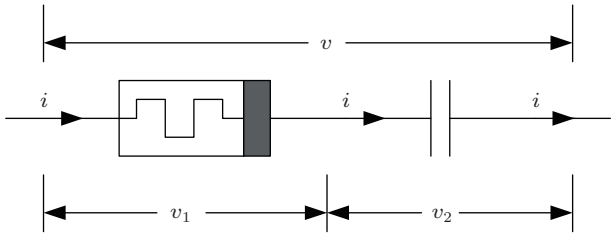


Fig. 1. MC circuit scheme. We use general definition of polarity: the terminal with black thick line denotes the negative terminal, and the other side is the positive terminal. When current flows from the positive terminal to the negative terminal, the memristor goes into the state of low resistance, *vice versa*.

Theorem 1 Let the memristor with monotonic memristance-versus-charge state map be driven by periodical current $i = I_{\max}\sin(\omega t)$, $\omega = 2\pi/T$, then the location of locus crossing point of this circuit will be able to be analytically computed by

$$\cot(\omega t) = \frac{\omega C}{2}\left[R(q(t)) - R\left(q\left(\frac{T}{2} - t\right)\right)\right]. \quad (7)$$

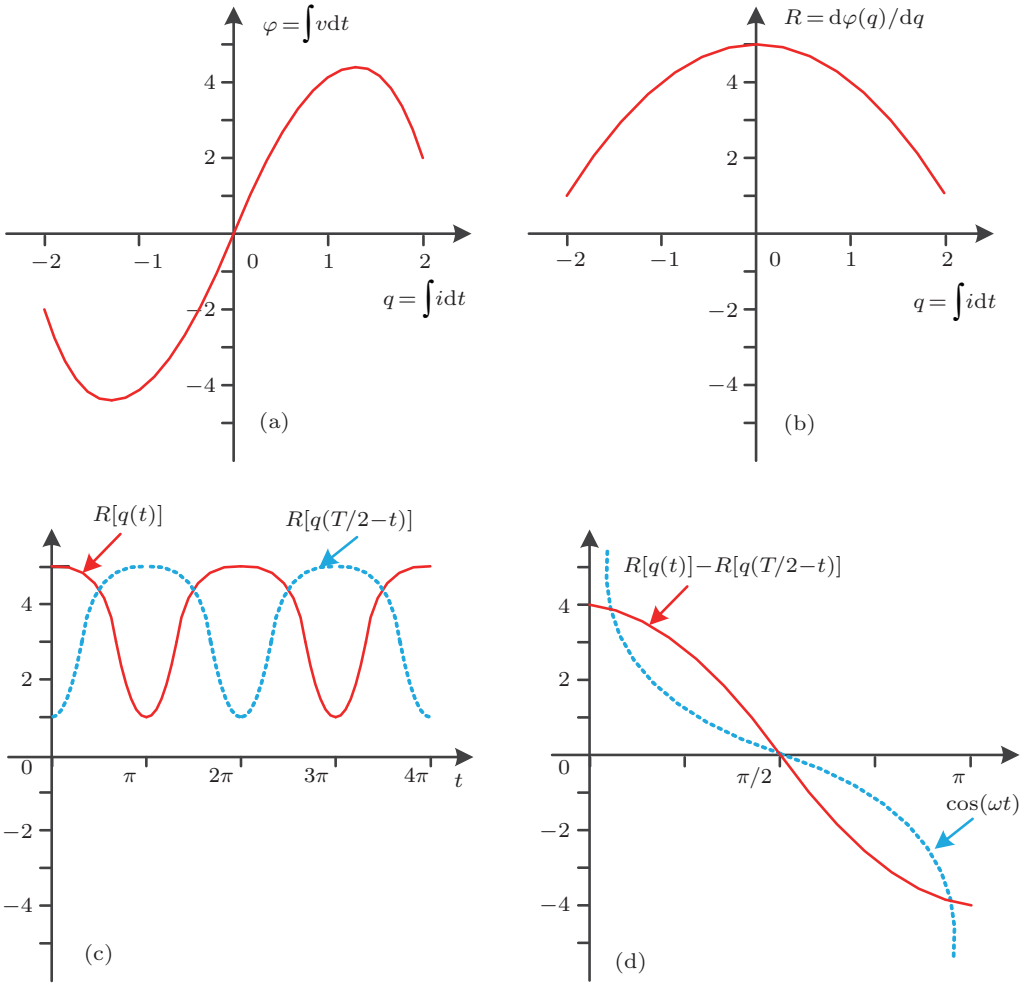


Fig. 2. (color online) Brief illustration of computing the locus crossing point location: (a) the constitutive relations of memristor; (b) R versus q map; panels (c) and (d) illustrate the solution of Eq. (7).

Proof According to the property of sinusoid, when $t \in [0, T/4)$

$$i(t) = i\left(\frac{T}{2} - t\right). \tag{8}$$

So if the crossing point lies in the first quadrant, the voltage at the crossing point should satisfy

$$v(t) = v\left(\frac{T}{2} - t\right). \tag{9}$$

Substituting Eq. (9) into Eqs. (6) and (5), we have

$$\begin{aligned} &R(q(t))\, i(t) + \frac{1}{C} q(t) \\ &= R\left(q\left(\frac{T}{2} - t\right)\right) i\left(\frac{T}{2} - t\right) + \frac{1}{C} q\left(\frac{T}{2} - t\right). \end{aligned} \tag{10}$$

After a short arrangement, we have

$$\begin{aligned} &\left[R(q(t)) - R\left(q\left(\frac{T}{2} - t\right)\right)\right] i(t) \\ &+ \frac{1}{C}\left[q(t) - q\left(\frac{T}{2} - t\right)\right] = 0, \end{aligned} \tag{11}$$

which can be further simplified into

$$\begin{aligned} &I_{\max}\left\{\left[R(q(t)) - R\left(q\left(\frac{T}{2} - t\right)\right)\right]\right. \\ &\left.\times \sin(\omega t) - \frac{2}{\omega C}\cos(\omega t)\right\} = 0. \end{aligned} \tag{12}$$

Solving the nonlinear equation (12) leads to the result (Eq. (7)). The derivation procedure is shown in Fig. 2.

4. Simulation of MC with linear memristance-versus-charge state map

Consider that the dependence of the memristance on the passing charge is given by the linear formula:

$$R(q) = kq + d, \tag{13}$$

where k is memristance changing rate proportional to the charge, and d denotes the initial memristance state. The memristance-versus-charge state map is obviously monotonic. Substituting Eq. (13) into Eq. (11) and making a short rearrangement, we have

$$\left[q(t) - q\left(\frac{T}{2} - t\right)\right]\left[ki(t) + \frac{1}{C}\right] = 0. \tag{14}$$

It follows from Eq. (14) that if the v–i locus crossing point exists during $t \in [0, T/4]$, i.e., in the first quadrant, the time solution must be $i(t) = -1/kC$. Meanwhile, the voltage applied to this circuit is

$$v = R(q)\, i + \frac{q}{C} = -\frac{kq + d}{kC} + \frac{q}{C} = -\frac{d}{kC}. \tag{15}$$

It is easy to see that the location of v–i locus crossing point is independent of frequency, but just inversely proportional to the capacitance and the memristance changing rate.

One such example is the well-known Hewlett–Packard (HP)'s linear model of memristor,[17] whose memristance can be expressed as Eq. (13), where

$$d = R_{\text{off}}, \tag{16}$$

$$k = -\frac{\mu_{\text{V}} R_{\text{on}}}{D^2}\left(R_{\text{off}} - R_{\text{on}}\right). \tag{17}$$

Here, R_{on} and R_{off} are the minimum and maximum values of the memristance, D denotes the thickness of memristor, and μ_{V} is the average ion mobility. The simulation results are given in Fig. 3. The memristor is excited by a source of harmonic current $i = I_{\max}\sin(2\pi f t)$, whose amplitude $I_{\max}$ is 1 mA. The memristor parameters are $R_{\text{on}} = 100\ \Omega$, $R_{\text{off}} = 12560\ \Omega$, and $D = 10$ nm. Figure 3(a) describes the influence of the working frequency f on the HP's linear model of memristor with the average ion mobility μ_{V}= 1×10^{-14} $\text{m}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$. It can be seen that with the increase of working frequency, the i–v hysteresis curve becomes contractive. From this figure, it can be obtained that the location of v–i locus crossing point of this memristor is independent of frequency.

Figure 3(b) provides the influence of the working frequency f on MC circuit. The capacitance value is set to be 0.2 μF and the average ion mobility μ_{V} is 1×10^{-14} $\text{m}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$. It can be seen from this figure that with the increase of working frequency, the i–v hysteresis curve also becomes contractive and the locations of v–i locus crossing point with different working frequencies are the same. From this simulation and Eq. (15), it can be concluded that the location of v–i locus crossing point of the MC circuit is also independent of frequency.

Figure 3(c) shows the influence of the capacitance value on the MC circuit in the case that the working frequency f is set to be 400 kHz and the average ion mobility μ_{V} is 1×10^{-14} $\text{m}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$. It can be seen from this figure that with the increase of capacitance value, the location of v–i locus crossing point is close to the original point. When the capacitor value tends to infinity, the MC circuit can be reduced to the memristor in Fig. 3(a). From this simulation and Eq. (15), it can be concluded that the location of v–i locus crossing point of the MC circuit is inversely proportional to capacitance.

Figure 3(d) exhibits the influence of the average ion mobility on the MC circuit with the working frequency f = 400 kHz and capacitance value $C = 0.2$ μF. It can be seen from this figure that with the increase of the average ion mobility, the location of v–i locus crossing point is away from the original point. When the average ion mobility is equal to zero, the MC circuit can be reduced to the RC circuit, whose i–v hysteresis curve has no crossing point.

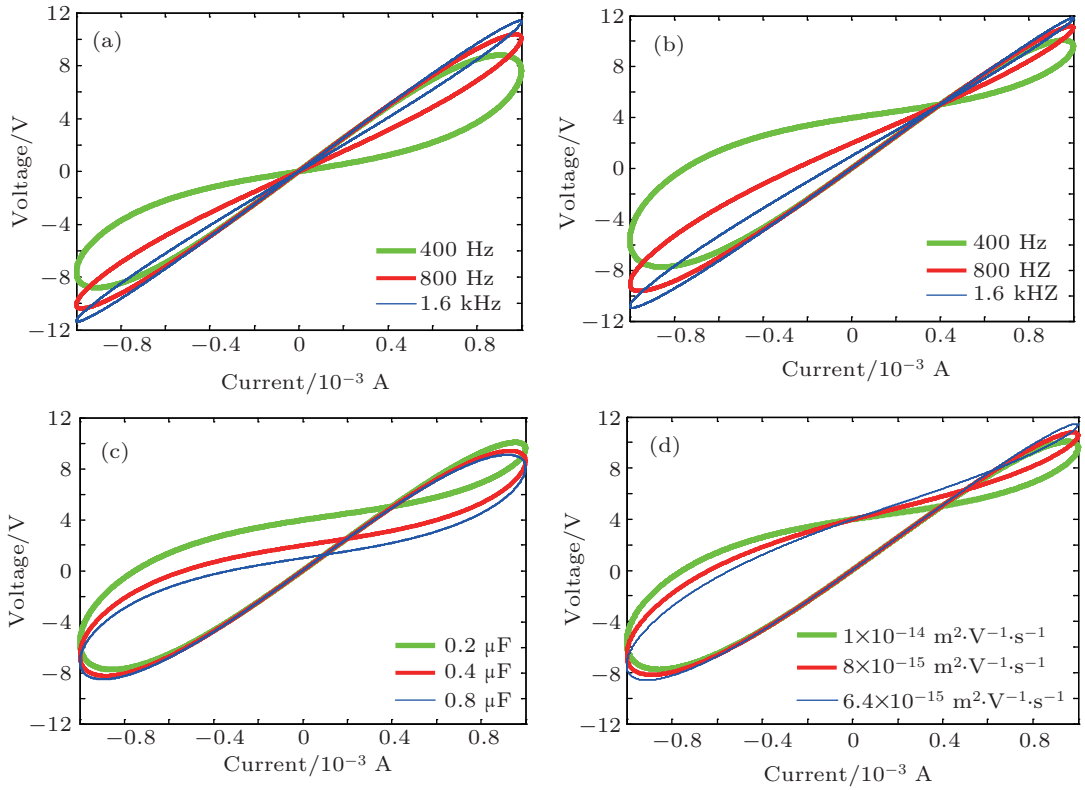


Fig. 3. (color online) Simulations of MC with the HP's linear model of memristor, showing the influences of the working frequency f on (a) HP's linear model of memristor, and (b) MC circuit; influences of (c) the capacitance value and (d) the average ion mobility on MC circuit.

5. Conclusions

The crossing point property of the ideal passive memristor is a noticeable point used to describe the voltage current characteristic of the circuit system with memristor. Based on the analysis, the analytical derivation with respect to the crossing point location of MC circuit is methodologically given. Then the MC circuit with HP's linear model of memristor[17] is demonstrated as an example of the MC circuit with linear memristance-versus-charge state map. From the simulation result and Eq. (15), the drift property of cross-point location, caused by the frequency and capacitance value, shows that the location of v–i locus crossing point is independent of frequency, but just inversely proportional to the capacitance and the memristance changing rate.

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