Frequency and voltage-dependent electrical and dielectric properties of Al/Co-doped PVA/p-Si structures at room temperature

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In order to investigate of cobalt-doped interfacial polyvinyl alcohol (PVA) layer and interface trap (D_{it}) effects, Al/p-Si Schottky barrier diodes (SBDs) are fabricated, and their electrical and dielectric properties are investigated at room temperature. The forward and reverse admittance measurements are carried out in the frequency and voltage ranges of 30 kHz–300 kHz and −5 V–6 V, respectively. C–V or ε'–V plots exhibit two distinct peaks corresponding to inversion and accumulation regions. The first peak is attributed to the existence of D_{it}, the other to the series resistance (R_s), and interfacial layer. Both the real and imaginary parts of dielectric constant (ε' and ε'') and electric modulus (M' and M''), loss tangent ($\tan\delta$), and AC electrical conductivity (σ_{ac}) are investigated, each as a function of frequency and applied bias voltage. Each of the M' versus V and M'' versus V plots shows a peak and the magnitude of peak increases with the increasing of frequency. Especially due to the D_{it} and interfacial PVA layer, both capacitance (C) and conductance (G/w) values are strongly affected, which consequently contributes to deviation from both the electrical and dielectric properties of Al/Co-doped PVA/p-Si (MPS) type SBD. In addition, the voltage-dependent profile of D_{it} is obtained from the low–high frequency capacitance (C_{LF}–C_{HF}) method.

Keywords: Al/Co-PVA/p-Si (MPS), electrical and dielectric properties, AC electrical conductivity, frequency and voltage dependence

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1. Introduction

Recently, considerable attention has been paid to the fabrication and electrical characterizations of organic semiconductor devices, such as metal–semiconductor (MS)- and metal–insulator/polymer–semiconductor (MIS or MPS)-type Schottky barrier diode (SBD).[1–8] There are many reports of conjugated conducting polymer-based devices being used in applications in the electronics industry.[9–22] Among them, polyvinyl alcohol (PVA) has the most excellent film forming, emulsifying, and adhesive properties with low melting point for the fully hydrolyzed and partially hydrolyzed grades. Although it is also a good insulating material with low conductivity, its conductivity can be increased by doping some metals, such as nickel (Ni), and zinc (Zn), cobalt (Co). Therefore, a metal-doped PVA material can be used as an interfacial layer between metal and semiconductor to prevent the interdiffusion between metal and semiconductor.[15–18,23]

The performances of MS, MIS, MPS, and similar devices are considerably influenced by the fabrication processes, structural and external effects. The performance of these devices is dependent on various parameters, such as interfacial layer and its inhomogeneity, surface charges, doping concentration of acceptor or donor atoms, interface traps or dislocations (D_{it}) localized at M/S interface, series resistance of device (R_s) and the shape of barrier formation at M/S interface.[24,25] When localized interface traps and an interfacial layer exist at the M/S interface, the device behavior is different from that in the ideal case. Therefore, the interface trap capacitance or excess capacitance depends strongly on the frequency and applied voltage, thus the C–V and G/ω–V characteristics are considerably affected.[26–35] For these reasons, the investigations of both electrical and dielectric properties dependent on voltage and frequency are important. On the other hand, although the electrical conductivity of pure PVA is poor, it can be improved by being doped with suitable dopant material, such as metal ions (Zn, Co, Ni, Cu, Fe). When a polymer is doped with these metals in various quantities and forms, their incorporation within a polymeric system can be expected to enhance the conductivity of the polymer. As is well known, when C–V and G/ω–V measurements are carried out only at one frequency and applied bias voltage, they cannot obtain enough information about the conductivity mechanism. However, when these measurements are performed at various frequencies and in a wide range of applied bias voltages, they can supply much information about both electrical and dielectric properties.

Therefore, in our study, Al/Co-doped PVA/p-Si (MPS)-type SBDs are fabricated and their electrical and dielectric properties are investigated with the following two aims: to investigate the variations of dielectric constant (ε'), dielectric loss (ε''), loss tangent ($\tan\delta$), AC electrical conductivity (σ_{ac}),

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and real and imaginary parts of electric modulus (M' and M'') each as a function of voltage and frequency; and, to obtain the voltage-dependent profiles of interface traps (D_{it}) and series resistance (R_s) and their effects on the electrical and dielectric properties. For these aims, forward and reverse bias C–V and G/ω–V characteristics are studied over the frequency and voltage ranges of 30 kHz–300 kHz and −5 V to 6 V, respectively, using an HP-4192A impedance analyzer at room temperature.

2. Experimental procedures

The Al/p-Si Schottky barrier diode (SBD) with a thin interfacial Co-doped PVA layer was fabricated on a p-type (bor doped) single crystal Si wafer with (111) float zone, 350-μm thickness, 0.04-Ω·cm resistivity. The semiconductor wafer first was cleaned in a mix of a peroxide–ammoniac solution and then in $H_2O + HCl$ solution for 10 min. The Si wafer was thoroughly rinsed in de-ionized water with 18-MΩ·cm resistivity in the ultrasonic bath for 15 min and then high purity Au (99.999%) with ∼ 2000 Å was thermally evaporated onto the back side of the Si at about 10^{-6} Torr (1 Torr = 1.33322×10^2 Pa). To provide a low resistivity Ohmic contact, the Si wafer was also annealed at 450 °C for 5 min in a dry nitrogen (N_2) atmosphere. Co-doped thin polyvinyl alcohol (PVA) film was fabricated on the p-type Si by an electrospinning method. A 0.5-g cobalt acetate was mixed with 1-g PVA. After vigorous stirring for 2 h at 50 °C, a viscous solution of codoped PVA acetates was obtained.

Using a peristaltic syringe pump, the precursor solution was delivered to a metal needle syringe (10 ml) with an inner diameter of 0.9 mm at a constant flow rate of 0.02 ml/h. The needle was connected to a high voltage power supply and positioned vertically on a clamp. A piece of flat aluminum foil was placed 15 cm below the tip of the needle to collect the nanofibers. By applying a high bias voltage (20 kV) on the needle, a fluid jet was ejected from the tip. The value of the interfacial Co-doped PVA was estimated to be 54.5 Å from the interfacial polymer layer capacitance. After the electrospinning process, rectifier contacts with 1 mm in diameter and 1500-Å thick high purity Au was deposited on the PVA surface through a metal shadow mask in a high vacuum system at 10^{-6} Torr.

The C–V and G/ω–V measurements were carried out in a frequency range of 30 kHz–300 kHz at room temperature by using an HP 4192A LF impedance analyzer between −5 V and 6 V DC voltages in steps of 50 mV. At the same time, a small AC signal of 40 mV_{p-p} was applied to the sample in order to meet the requirement. All of these measurements were carried out with the help of a microcomputer through an IEEE-488 AC/DC converter card in a shielded environment to avoid any external noise or illumination.

3. Results and discussion

3.1. Electrical characterization

Voltage-dependent C and G/ω each as a function of frequency are given in Figs. 1(a) and 1(b), respectively. As can be seen in Fig. 1(a), C–V plot for each frequency presents two peaks which are corresponding to the inversion and accumulation region due to the continuous distribution of D_{it} at M/S interface near the energy band gap of Si and R_s of device, respectively Contrary to C–V plots, the G/ω–V plots each show a nearly U-shape behavior for each frequency. As the frequency decreases, the interface charges at traps can easily follow the external an AC signal and thus cause the C and G/ω values to increase. Such a behavior can be explained in terms of the charge storage ($C = Q/V$). In this way, these charges can increase the C and G/ω values. On the other hand, it is believed that the injection of charges involves a process of hopping to localized interface traps/states, but the detailed physical mechanism of an injection is not well understood yet.

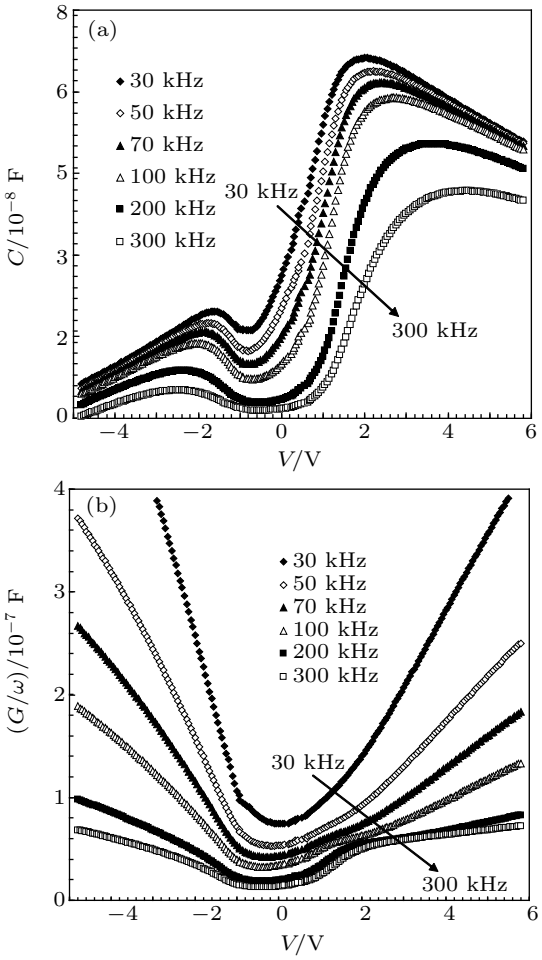


Fig. 1. Variation of (a) capacitance (C) and (b) conductance (G/ω) with voltage for MPS-type SBD at the room temperature for different frequencies.

In order to clearly see this contrast, the C–V and G/ω–V plots for 100 kHz are shown together in Fig. 2. It is clear that, in the inversion and accumulation regions, the minimum of the C value corresponds to the maximum of the conductance.

This contrast in C and G/ω values shows that the material displays an inductive behavior in the inversion and depletion regions.[28]

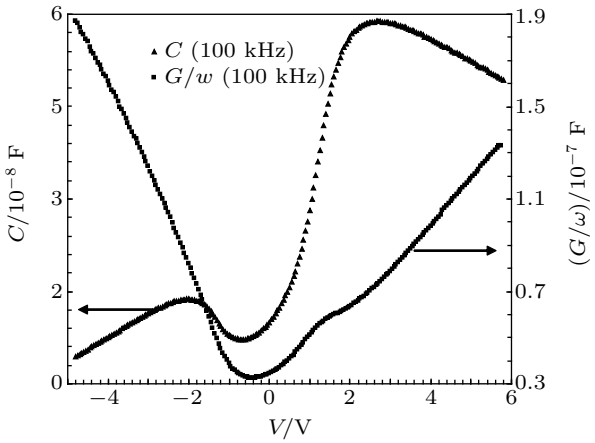


Fig. 2. Variations of capacitance (C) and conductance (G/ω) of the MPS-type SBD at the room temperature with voltage for 100-kHz frequency.

It should be pointed out that the value of R_s is as important as D_{it}, which influences both electrical and dielectric properties of device. Therefore, the voltage-dependent resistivity (R_i) profile is obtained by using the C and G/ω data using admittance method developed by Nicollian and Brews.[24] This method can determine the value of R_i in the whole measured range of device. According to this method, the real value of R_i at sufficiently high frequencies and in a strong accumulation region corresponds to the real value of R_s for MPS diode and can be obtained from the measured C_{ma} and G_{ma} values, as follows:[24]

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2}, \tag{1}$$

where ω ($= 2\pi f$) is the angular frequency, C_{ma} and G_{ma} are the capacitance and conductance values in the strong accumulation region. In addition, the voltage-dependent R_i values are extracted from Eq. (1) for each frequency, and are given in Fig. 3. It is significant to pay special attention to R_s effect in the admittance characteristics. As shown in Fig. 3, the R–V plots give distinguishable peaks at about zero bias, which corresponds to the minima of the G/ω–V plots. It is indicated that the value of resistance is proportional to inverse conductance ($R_i = 1/G_i$). The magnitude of peak decreases with the increase of frequency. As can be seen in Fig. 3, in a sufficiently high forward bias region ($V \geq 6$ V), the real value of resistance corresponds to the R_s of structure especially at high frequencies. On the other hand, in the depletion and accumulation regions, the value of R_i is greater than the real value of R_s due to the charges in interface traps and dislocations.

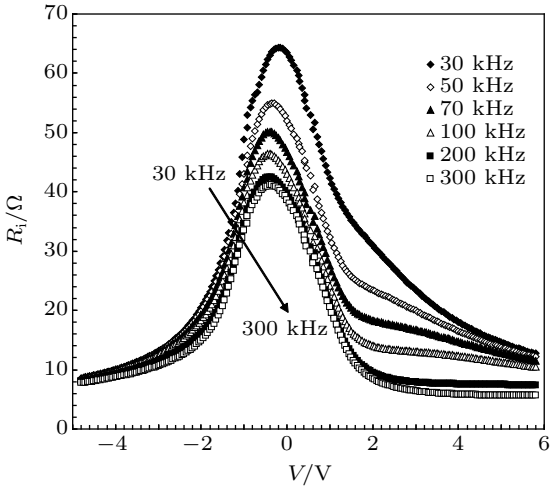


Fig. 3. Variations of the resistivity of the MPS-type SBD with applied bias voltage at room temperature for various frequencies.

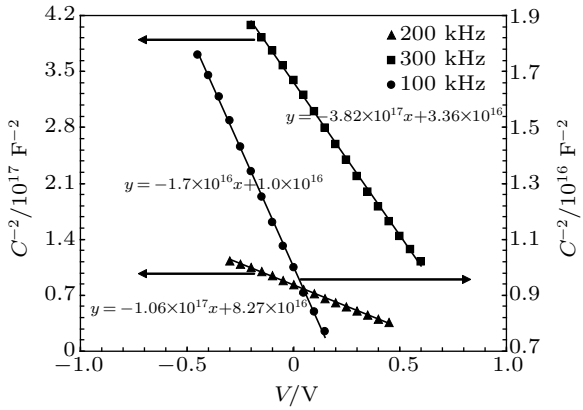


Fig. 4. The C^2–V plots of the MPS-type SBD at the room temperature for three frequencies.

The doping concentration of acceptor atoms (N_A), Fermi energy level (E_F), diffusion potential (V_d), and barrier height ($\Phi_B(C$–$V)$) are found from the reverse bias C^{-2} versus V characteristics (Fig. 4) for high frequencies (100, 200, and 300 kHz) at which the effect of charges at traps is avoided.[25] In addition, the values of R_s are obtained from the admittance method at sufficiently forward bias (6 V) for the same frequencies. The obtained values of them are given in Table 1. As shown in Table 1, while the values of E_F, V_d, and $\Phi_B(C$–$V)$ increase with the increasing of frequency, N_A and R_s decrease. These results indicate that the main diode parameters, such as N_A, E_F, V_d, $\Phi_B(C$–$V)$, and R_s must be obtained at sufficiently high frequencies to eliminate the charge effect at interface traps.

Table 1. Obtained various experimental parameters for the MPS-type SBD determined from C–V data at high frequencies.

f/kHz	$N_A/10^{17}$ cm^{-3}	E_F/eV	V_d/eV	Φ_B/eV	R_s (at 6 V)/Ω
100	7.23	0.074	0.61	0.68	10.51
200	1.15	0.120	0.80	0.92	7.36
300	0.32	0.152	0.90	1,05	5.62

There are several methods in the literature to obtain the voltage/energy density distribution profile of D_{it}.[24,25,32]

However, the high–low frequency capacitance (C_{HF}–C_{LF}) method is more suitable for obtaining the D_{it}–V profile. The advantage of this method comes from the fact that it permits the determination of many properties of the interface layer, the semiconductor substrate, and interface easily. In addition, this method requires only two C–V plots. According to this method, the D_{it}–V plots can be extracted from its capacitance contribution to the measured experimental C–V plot. In the equivalent circuits of MIS, MOS, and MPS devices, the interfacial layer capacitance C_i is connected in series with the parallel combination of the interface state capacitance C_{ss} and the space charge capacitance C_{sc}. The value of C_{it} can be determined by subtracting the space charge capacitance C_{sc} (extracted from the measured high frequency capacitance C_{HF}) from the C_{sc} in parallel with the C_{ss} (extracted from the measured low frequency capacitance C_{LF}) and is given as

$$C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_i}\right]^{-1} - C_{sc}. \tag{2}$$

As is well known, at high frequencies, D_{it} cannot respond to the AC excitation, so they do not contribute to the total capacitance directly, but stretch out of the C–V curve occurs. Therefore, the equivalent capacitance is the series connection of C_i and C_{sc} and is given as

$$\frac{1}{C_{HF}} = \frac{1}{C_i} + \frac{1}{C_{sc}}. \tag{3}$$

Thus, by combining Eqs. (2) and (3), the interface state density D_{it} is calculated from

$$qAD_{it} = C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_i}\right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_i}\right]^{-1}. \tag{4}$$

This calculation is performed numerically from the flat band to strong accumulation, and to strong inversion. The voltage-dependent profile of D_{it} is also obtained from the low–high frequency capacitance (C_{LF}–C_{HF}) method by using low frequency (1 kHz) and high frequency (300 kHz). It is believed that at sufficiently low frequencies, the charges in traps cannot follow the external AC signal, which is contrary to the scenario at high frequencies. The plots of low–high frequency capacitance versus voltage are given in Fig. 5 and the obtained voltage-dependent profile of D_{it} is given in Fig. 6. It is clear that the plot of D_{it} versus V presents a peak at about 1 V, which corresponds to the depletion region. The mean value of D_{it} is found to be 2.5×10^{13} ($eV^{-1} \cdot cm^{-2}$). Such a peak behavior of D_{it} versus V plot can be attributed to a particular density distribution of interface traps between metal and semiconductor.

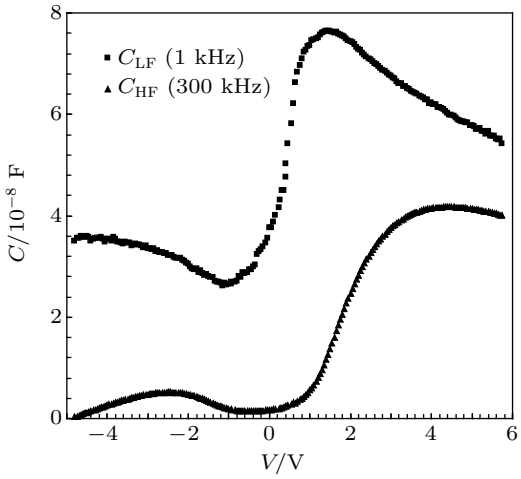


Fig. 5. Measured high–low frequency capacitance (C_{LF}–C_{HF}) plots of the MPS-type SBD at room temperature.

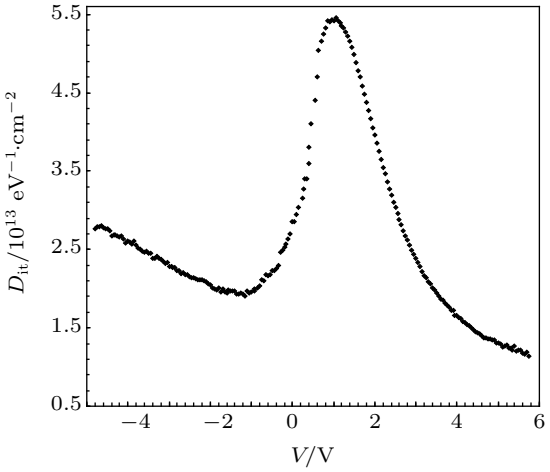


Fig. 6. Energy distribution profile of the D_{it} obtained from high–low frequency capacitance method for the MPS-type SBD at room temperature.

3.2. Dielectric properties and AC conductivity

The values of real and imaginary parts of dielectric constants (ε' and ε''), loss tangent ($\tan\delta$), AC-conductivity (σ_{ac}), and the real and imaginary parts of electric modulus (M' and M'') of the used interfacial polymer layer (Co-doped PVA) that is located at M/S interface are obtained from the voltage-dependent C and G measurements using the following expressions, respectively:[36,37]

$$\varepsilon^* = \varepsilon' - j\varepsilon'' = Cd/A\varepsilon_o - j\,(Gd/\omega A\varepsilon_o), \tag{5}$$

$$\tan\delta = \varepsilon''/\varepsilon', \tag{6}$$

$$\sigma_{ac} = \omega\varepsilon_o\varepsilon'\tan\delta, \tag{7}$$

$$M^* = \frac{1}{\varepsilon^*} = M' + jM'' = \frac{\varepsilon'}{\varepsilon'^2 + \varepsilon''^2} + j\left(\frac{\varepsilon''}{\varepsilon'^2 + \varepsilon''^2}\right), \tag{8}$$

where ω, d, ε, and A are the angular frequency, the thickness of the PVA, permittivity of the free space ($\varepsilon = 8.85 \times 10^{-14}$ F·cm^{-1}), and the rectifier contact area, respectively. Both the obtained dielectric properties and electric modulus values each as a function of applied bias voltage and

frequency can supply much information about conductivity mechanism and relaxation process for a specific electronic application.[36,37] The voltage dependences of ε', ε'', and $\tan\delta$ profiles are obtained using Eqs. (2) and (3), and are given in Figs. 7(a)–7(c), respectively. As can be seen in these figures, the values of ε', ε'', and $\tan\delta$ are strongly dependent on both frequency and applied bias voltage.

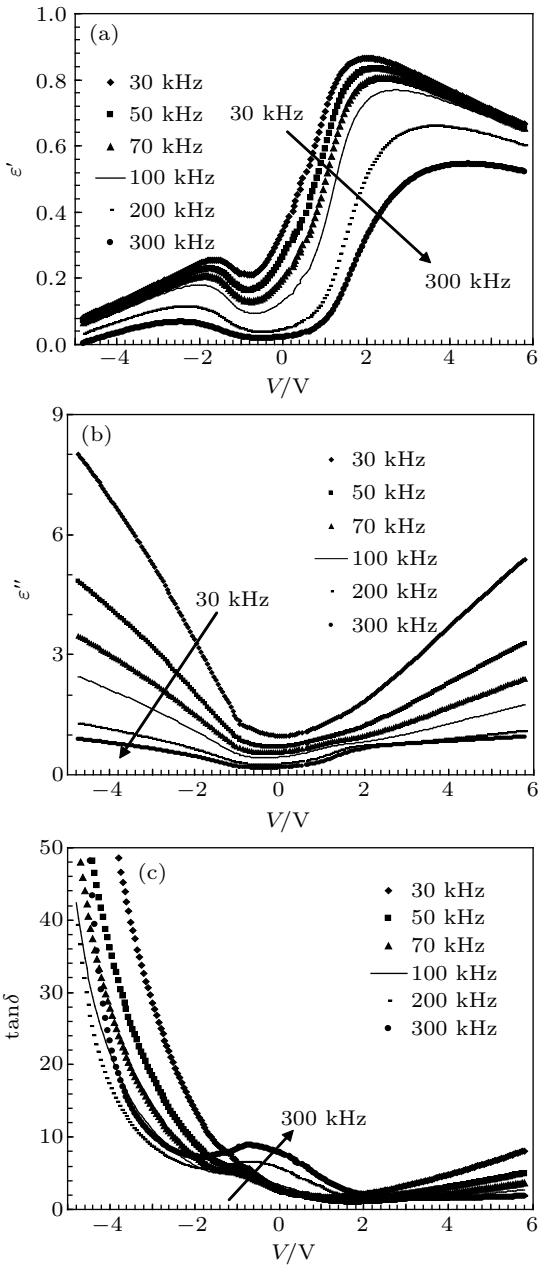


Fig. 7. Voltage dependence of the (a) ε', (b) ε'', and (c) $\tan\delta$ at various frequencies for the MPS-type SBDs at the room temperature.

As can be seen in these figures, the profiles of ε', ε'', and $\tan\delta$ versus V are found to be similar to the plots of C–V and G/ω–V due to the same reasons. These behaviors can be attributed to the interfacial effect within bulk of the sample, interfacial polymer layer, interface trap, surface polarization, and electrode effect.[37,38]

The σ_{ac}–V plot is also obtained from the conductivity data and is given in Fig. 8. As shown in this figure, the voltage-dependent value of σ_{ac} as a function of frequency indicates similar results. The increase in σ_{ac} with frequency conductivity is accompanied by an increase of the eddy current, which in turn increases the $\tan\delta$ due to the gradual decrease in series resistance with the increasing frequency.[39] Similar results are observed in Refs. [40] and [41], where the values of σ_{ac} are found to be almost independent of voltage at high frequencies.

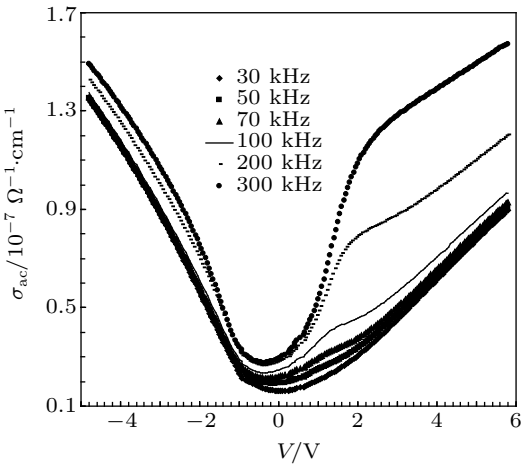


Fig. 8. Variations of the AC electrical conductivity (σ_{ac}) with applied bias voltage for the MPS-type SBDs at room temperature for different frequencies.

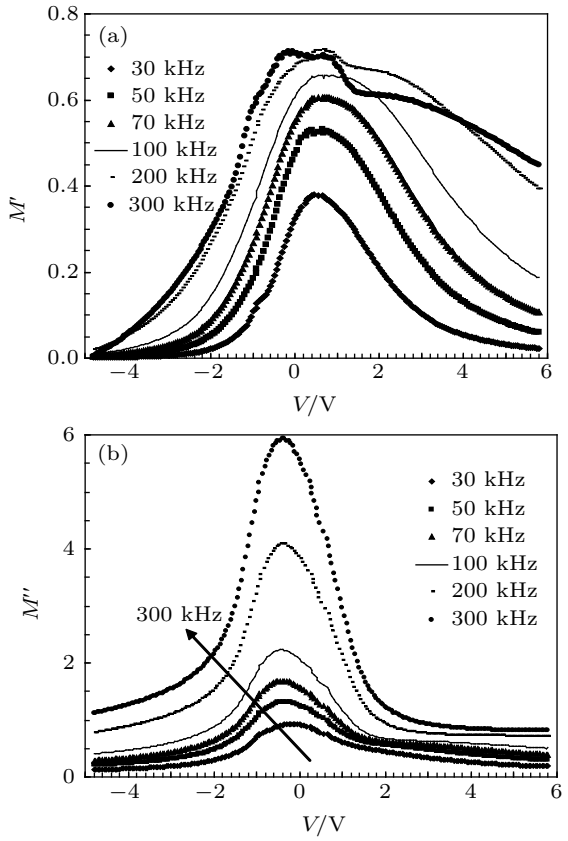


Fig. 9. Plots of (a) real part M' and (b) imaginary part M'' of electric modulus M^* versus voltage over a measured frequency range of 30 kHz–300 kHz for the MPS-type SBD at room temperature.

M'–V and M''–V plots are also obtained by using ε' and ε'' data for various frequencies and given in Figs. 9(a) and 9(b), respectively. Each of these plots exhibits a peak. The peak magnitude increases with the increasing of frequency and its position shifts toward negative bias voltage slightly. Similar results have been reported in Refs. [11], [15], [42], and [43]. The features of these plots are attributed to the relaxation polarization in doped polymers and charges in traps. In polymer composite films, the existence of charges in traps gives rise to interfacial polarization. Therefore, it is believed that the dielectric relaxation process in the doped polymer is not a pure process.[15]

4. Conclusions

Both the frequency and voltage dependences of electrical and dielectric properties of Al/Co-PVA/p-Si type SBDs are investigated in wide frequency and voltage ranges at room temperature. The main electrical parameters, such as N_A, E_F, V_d, $\Phi_B(C$–$V)$, and R_s, are obtained at sufficiently high frequencies to eliminate the charges in interface traps. In addition, the main dielectric properties, such as ε', ε'', $\tan\delta$, σ_{ac}, M', and M'' values, are also obtained, each as a function of frequency, by using admittance measurements that include frequency-dependent capacitance and conductance values in the frequency and voltage ranges of 30 kHz–300 kHz and −5 V–6 V. All of these parameters are found to be strongly dependent on frequency and applied bias voltage in the inversion, depletion, and accumulation regions. However, these changes in inversion and depletion region are attributed to the existence of D_{it}, but in the accumulation region they are attributed to the R_s and interfacial PVA layer. The two peak behaviors in ε'–V plots can be especially attributed to a particular distribution of D_{it}, R_s, and interfacial polarization. In addition, the plots of M' and M'' versus V each show a distinct peak and its magnitude of peak increases with the increasing of frequency. These results show that the interface trap capacitance (C_{it}), R_s, and the interfacial PVA layer strongly affect the C–V and G/ω–V data, and consequently contribute to a deviation from both the electrical and dielectric properties of Al/Co-doped PVA/p-Si (MPS) type SBD. In addition, the voltage-dependent profile of D_{it} is obtained from the high frequency capacitance $(C_{LF}$–$C_{HF})$ method and it shows a peak at about 1 V. As a result, the values of electrical, dielectric, and electric modulus are all found to be considerably high at low frequency compared with at high frequency. These behaviors may happen because of interfacial effects within the bulk of the sample, the interfacial polymer layer, the interface trap, the surface or interfacial polarization, or because of the electrode effect.

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